

Rostir, Inc.: The Fabrication of Ultra High Value Chip Resistors & Business Plan Development

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Abstract— The concept of this project was comprised of a proof of concept design with an additional focus on entrepreneurship. To define clearly, this project included the selection of a device to fabricate, where a commercial market opportunity existed, using semiconductor technologies while simultaneously developing a business plan marketed towards further funding. This project required complete design of the Ultra High Value Chip Resistor as well as a process design for fabrication of the resistors. Gigaohm resistance values were achieved and varied with a range between 60-160Gohms, with an average of 99.5 Gigaohms, the expected value was 86.6 Gigaohms. Some results may have been skewed by noise and extremely small current levels. Additionally, the devices were subjected to high intensity light and heat, both of which can generate carriers and decrease the resistance values. The devices were shown to have VCR of 5000ppm/°V and TCR of 6250/°C

Index Terms— Chip Resistors, Gigaohm, Semiconductor Technologies.

I. INTRODUCTION

The concept of this project was comprised of a proof of concept design with an additional focus on entrepreneurship. To define clearly, this project included the selection of a device and process, where a commercial market opportunity existed, using semiconductor technologies. The motivation of this project came from student requests and career goals along with the flexibility and experiences of the Microelectronic Engineering faculty. As the first project of its kind in various business development resources, methodologies, and ideas were explored that would enable Rostir the project to transition to an operating business.

The devices selected for project were Ultra High Value Chip Resistors based off of currently manufactured Surface Mounded Devices (SMDs) that existed in a niche market, ease of manufacture, and potential advantages offered by using Semiconductor Technology.

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Currently most Ultra High Value Chip Resistors are manufactured using a Ceramic or Silicon substrate where a ceramic paste is spread across the substrate and is then patterned using an electron beam writer.¹ Each chip is written, one by one, and throughput limitations can occur when devices designs are more complicated. Additionally, this technology requires multiple designs for different value chips. Tolerances and repeatability tend to be a limiting factor when compared to semiconductor technology.

Ultra High Value chip resistors currently reside in a niche market with specific applications. Currently these devices are used in high input impedance quartz amplifiers, low temperature sensing applications, and testing devices.

II. Entrepreneurial Methodologies

A business plan encompassing all aspects of business: marketing, financial, and industry analysis has been written in its organic form, representing the ongoing changes inherent with writing and developing a new business. A formal abbreviated plan was also developed and submitted to the RIT Undergraduate Business Plan Competition in 2006 in conjunction with Stephen Parshall. The business plan emphasis is on technology leverage in to the SMD market by translating one mature technology in a constantly changing industry (Semiconductor) into another industry (SMD Passives) offering novelty and performance increase in comparison to that industry's particular mature technology (SMD Passive). The business plan also includes integration steps with the Microelectronic Engineering department and the Microelectronic Student Association.

In order to provide adequate background for similar future projects certain classes offered at RIT should be taken, including, Entrepreneurship, Managing Innovation and Technology, and any entry level finance class. These classes provide the knowledge necessary to write a complete and adequate business plan as well as provide a consulting opportunity for a business to full work out any inconsistencies or offer suggestions on how to develop the strategy relating to business development.

III. Chip Design/Process Design

A new chip design was employed to achieve the large resistance values desired based on empirical evidence on experiments using the Varian implant tool.ⁱⁱ An initial design was conceived, however due to limitation of simulation tools, could not be relied on, as will be explored later. The device chips were designed using Mentor Graphics IC Station based on five common chip resistor sizes founded in industry. This enables Rostir to enter the SMD passives market with limited learning curve for consumers.

$$R = \rho \left(\frac{L}{W * t} \right) \quad (1)$$

$$\frac{\rho}{t} = R_s \quad (2)$$

$$R = R_s \left(\frac{L}{W} \right) \quad (3)$$

Equation 1-3 Resistance as a function of Rs & resistivity

Equation 1- 3 describe that resistance is based off of the length, width and thickness of the resistive material. In order to achieve the same resistance for each different sized chip resistor, the active area for each device was designed to be the same. This also enabled a cost saving measure by requiring only one mask step to define the active area instead using multiple mask designs which would have been used for various implantation steps. Sheet resistance, Rs, plays a crucial role in determine the outcome of the resistance value of the chip resistor. As the chip design was manufactured to have 1724 squares a required sheet resistance of 68 MegaOhm was necessary to have a resistance value acceptable for this projects proof of concept design. The chip design included 99 devices per die and roughly 3,564 devices per 6inch wafer.

The chip layout included three levels, an active level, which defines the resistor value, a metal level, which defines the resistor size, and contact cut level. Although the lithography tool being used has fine alignment capabilities, the device tolerances were large enough to only use the pre-alignment feature on the Canon FPA 2000il and the auto-global alignment feature. Additionally, no test structures were designed on the chip. The mask was written by the SMFL mask-house using a MEBESIII electron beam mask printer. The respective chip resistor sizes are as follows:

Chip Sizes
1.27mm x 0.635mm
1.27mm x 1.016mm
1.27mm x 1.905mm
1.27mm x 2.54mm
1.27mm x 3.81mm

Table 2 - Chosen Common Chip Resistor Designs ⁱⁱⁱ

The mask was designed with λ = 1μm and metal overlay error equal to λ = 10μm. In order to accommodate for isolation

between devices and dicing of the wafer, a 200μm buffer was included around each device.

Simulation work was done using Design Architect's ATHENA to provide expected process parameters, however the process provided erroneous results due to the inability of the program to calculate low doping levels in to polysilicon.

IV. Fabrication & Platform Design

This project required the complete design of Ultra High Value Chip Resistors as well as a process design for fabrication of the resistors. The process developed was based around the SMFL toolset capabilities at RIT and prior knowledge from other chip resistors fabricated at RIT. The resistors were fabricated in the SMFL using three mask levels. The layout was designed using Mentor Graphics IC station and the masks fabricated using the SMFL mask house MEBESIII. The basic process flow included use of a coat/develop track, lithography exposure tool, furnace system, LPCVD, PECVD, Ion Implanter, Wet Chemistry Bench, Dry Etch, and Metal Sputtering System.

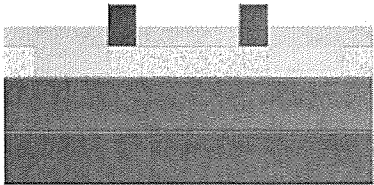


Figure 1 - Cross Section of Final Product

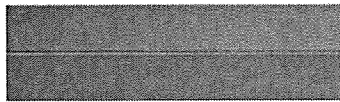
The SMFL toolset capabilities provided two platforms for fabricating the chip resistors on either 100mm or 150mm wafers. A cost analysis which considered further R*D costs, proof of concept costs, and full scale production, showed that 150mm platform would provide better cost per device per run than the 100mm platform.^{iv}

Fabrication

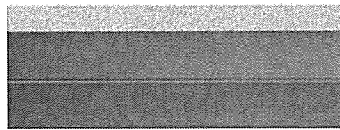
A new process flow was developed to fabrication the high value chip resistors which utilized the following select process steps: isolation between wafer and resistor material using a wet thermal oxide, B11 doped polysilicon (the resistor material), TEOS isolation to protect the resistor from the environment, contact cut lithography, and metallization. Many decisions during fabrication were focused towards implementation into a full scale manufacturing process where throughput and functionality were a major concerns.

Step I, II, III: Isolation & Resistor Formation

I Grow 20,000Å Isolation Oxide
530 minutes @ 1100°C



II LPCVD Deposit .5µm Poly



Implant Dose = 3E13 ions/cm² B11
Energy = 40KeV
Current = 1.5 E-6 Amps

III Bruce Furnace: Thermal Activation

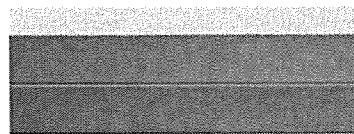


Figure 2 - First three process steps

- Wafer Selection
- Grow 2µm Isolation Wet ox @ 1100 °C
- LPCVD Poly .5µm
- Implant Dopant
- Step I, II, III (Figure 2)

A total of ten wafers were selected for this proof of concept run, where five wafers were device wafers and the other five used as test/device wafers. An insulating oxide was grown using a Bruce furnace for 530 minutes at 1100°C to target the 2µm thickness. The 2µm thickness was desirable to achieve a high voltage rating, where the voltage rating is the maximum voltage a device can operate safely. The voltage rating is defined by the isolation between the substrate material and the resistor material. The thermally grown oxide provides a good quality limiting the amount of voids, defects, oxide charges, or other impurities that can cause arcing as higher voltages are applied. Additionally, the Voltage rating can be defined by the breakdown voltage of the isolation material, where the insulation material, oxide, breakdowns causing the device to fail indefinitely. With a desired voltage rating of 2000 Volts, superior to direct competitors, it was determined that 2µm thickness isolation would be needed via Equation 4 where thermal oxide has breakdown voltage of 10Mv/cm.

$$1000 \frac{MV}{m} = 2000V, 2E^{-6}m = 2\mu m$$

Equation 4 - Calculation of isolation thickness based off of field strength

The actual resultant thickness grown was 19300Å negligibly affecting the suspected voltage rating down to 1930 Volts.

Next a polysilicon layer was deposited using the ASM 6" LPCVD with a target of .5µm. A deposition time of 90.9 minutes was selected based off of a previous tool deposition rate of 55Å/min. The flow rate of Silane was set 100 sccm with the recipe temperature set point to 600 °C. A test wafer was used to determine the polysilicon thickness, which was found to be roughly .7µm, overshooting the target value. This thickness difference had no impact on limiting the devices from achieving intended process specifications, as the implant step had not yet been done. The thickness of the polysilicon layer does inversely affect sheet resistance via Equation I, thus requiring more stringent guidelines for manufacturing runs.

To create a functioning device with a specific value the polysilicon was implanted with B11 at a Dose of 3E13 ions/cm with a current of 14µA, and energy of 40KeV which provided a throughput of 65 seconds per wafer. The introduction of B11 impurity enables the proper amount of current to flow when a voltage is applied. Careful consideration to the amount of dose was necessary since the relationship between resistivity and dose is not linear.

Ultimately a dose was found and sheet resistance was measured using the a four point probe connected to a multimeter. Originally a CDE Resistivity-mapper was to be used, however such high resistance values could not be registered by the device. The sheet resistance was defined by

the following equation, $\frac{V}{I} \frac{\pi}{\ln 2}$.

B11 was selected as the dopant material since it provides an ohmic contact between for the probes to measure sheet resistance, as compared to the phosphorus species P31. To activate the dopant a thermal process was done for 30 minutes and sheet resistance measurements were made resulting in roughly 68megaohms/square.

Step IV: Creation of Active Region

Level I Lithography: Active Define
Etch Poly LAM 490



Figure 3 - Steps IV

- Lithography Level I
- Polysilicon Dry Etch
- Ash PR & RCA Clean Standard

The active area for the chip resistors was defined by level lithography, which defined the large contact pads and mor

intricate serpentine structure of the resistor. A new stepper job was created for this process which called for an exposure dose of $160\text{mJ}/\text{cm}^2$ and a focus offset of $.24\mu\text{m}$. no alignment was necessary for this step. The program created 36 die to be exposed, with portions extending beyond the wafer surface. Each die contained eleven rows and nine columns of chip resistors, resulting in roughly 3,564 devices per wafer. The polysilicon was then etched using the a LAM 490 using endpoint detection, test wafer with a polysilicon over oxide film stack was first used to verify endpoint detection was functioning properly by performing a BOE wet etch in a similar method used to determine wet etch rates.

Step V: Isolation & Contact Cuts

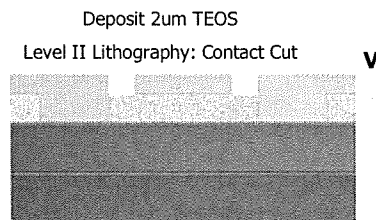


Figure 4 - TEOS & Contact Cuts

- TEOS
- Lithography Level II
- Contact Cut Etch
- AS PR & RCA Clean Special HF Dip

A $2\mu\text{m}$ thick TEOS layer was then deposited using a AME P5000 PECVD and verified using a blank test wafer. The TEOS film was chosen over Nitride due to suspected film stresses that might have resulted in film cracking and ultimately failure of devices. This film stack layer provides external environmental protection for the doped polysilicon resistor. Following this deposition level II lithography was completed, by aligning to the Canon i-line TVPA marks and using it's AGA (Automatic Global Alignment). More precise alignment technologies available on the Canon were not used due to the large features, which ultimately would have had limited improvement on the final product and increased throughput times. A contact cut etch was performed using BOE for 12minutes , the etch rate was $1706\text{ Angstroms}/\text{min}$.

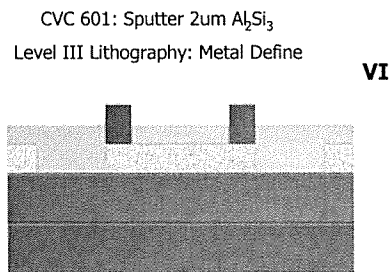


Figure 5 - Metallization & Final Device

- Sputter Metal: Aluminum
- Lithography Level II: Define Resistor Sizes
- Metal Etch: HF Phosphoric Acid
- Ash PR

An Aluminum film was deposited using a CVC 602 in which roughly $1.9\mu\text{m}$ was deposited using 2000 Watts of power at 4mtorr for 53minutes. Ultimately Aluminum will not be the film of choice, however, for testing purposes which prove the ability to achieve Gigaohm values of resistance; aluminum was the least expensive and most readily available target.

Level III lithography required a thicker photo-resist to be coated to ensure greater adhesion and greater protection for the metal etch process. Additionally, a different develop recipe was used in which had a longer develop time and higher hardbake temperature than the previous lithography coat/develop processes. The metal was then etched in a Hot Phosphoric Acid bath at a temperature of 80C for roughly 7 minutes and was verified by measuring oxide thickness in non-active areas.

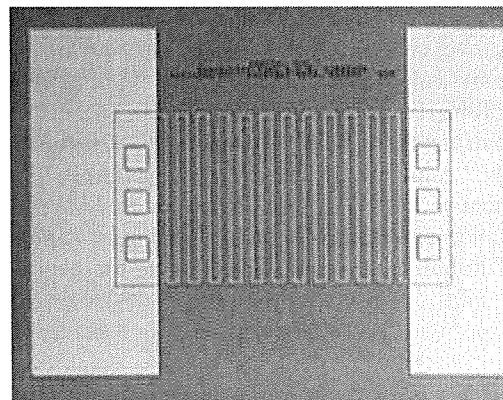


Figure 6 - Chip Resistor at end of fabrication

V. Testing Methods & Results

Step VI: Metallization

Testing was completed in the testing lab in the Microelectronics Building #17 using a HP4145A Semiconductor Parameter Analyzer connected to a computer running Interactive Characterization Software (ICS).

In order to evaluate the devices properly a labeling convention was created using the following format:
SizeRow#Column#Device#, example 650R1C1D1,

corresponds to a 650um device found in Row 1, Column 1 and is Device 1 on the chip. Device numbers correspond to how many of same size chips exist on the wafer when read from left to right and the flat of the wafer oriented down.

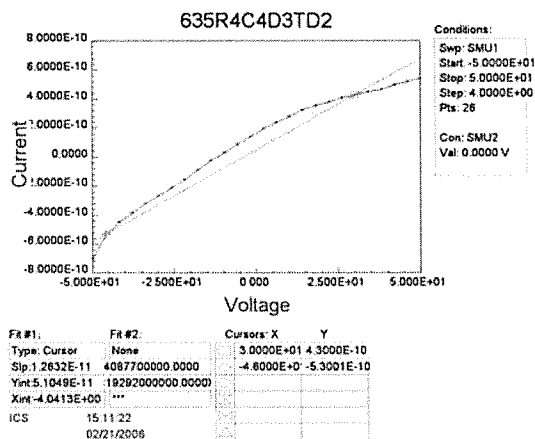
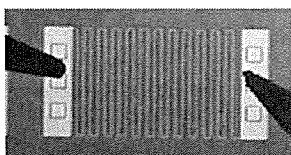


Figure 7 - 635um I-V Characteristic, 76.2 Gigaohm



Picture 1 - 635 um Device

Figure 7 and Picture 1 depict the first I-V characteristic of the devices fabricated. The result was successful, achieving 76.2 ohms. The curve is mostly linear, with a slight roll when voltage was first applied. Figure 8 is a comparison between all the devices tested, all achieving Gigaohms results with a range between 60 to 160 Gigaohms with an average of 99.5 Gigaohms, over shooting the expectation of 86.6 Gigaohms. The range and values of the chip resistors are suspect to the accuracy of the testing method, which in this case may need further refinement due to the effect of any EMF around the testing area. Additionally, it was determined from the range of values that sorting of the chip resistors based on a specific range of values and tolerances would need to be implemented in to the distribution process. The reasoning for this is to maintain quality and profit margin, i.e.: A device with a 100 Gigaohm spec with 20% tolerances sells for less than a device with 5% tolerances.

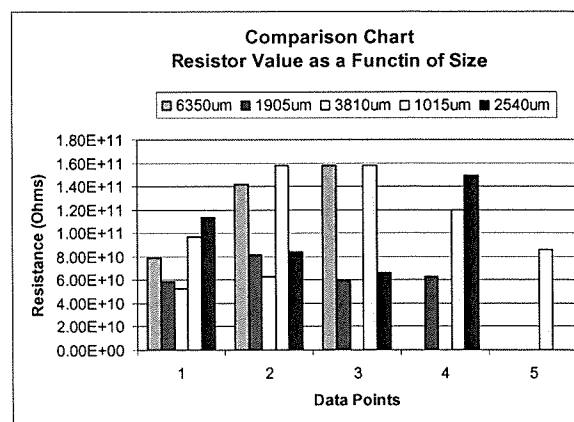


Figure 8 - Comparison Chart of Resistor Values

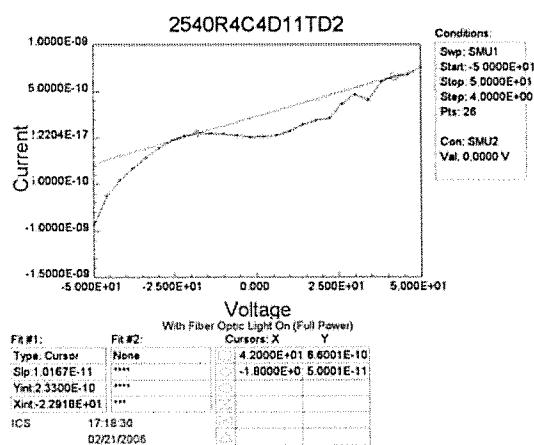


Figure 9 - Light Exposed devices, 84.5 Gigaohm

Devices were also exposed to light in order to test how short lived light generated carriers affect the resistance of the devices. It is known that Boron has high absorptive qualities of energy, thus the devices were tested to see how light generated carriers would affect the resistance of the devices.^v It is shown in Figure 9 that Gigaohm resistances are still obtained, however the I-V characteristic is not quite linear. This could be due to the testing method and/or the effect the carriers having on the devices. To be sure, Figure 10 compares the same device resistance values measured when exposed to light and when not exposed to light. According to the graph the resistances seem to vary from run to run, suggesting that the test method must be changed and inconclusive results on whether light does actually affect the resistances. Lastly, this characterization or quality control measure may not be necessary in a manufacturing setting considering the devices will be soldered contact side down, with the back side of the wafer acting as a light barrier for the resistors.

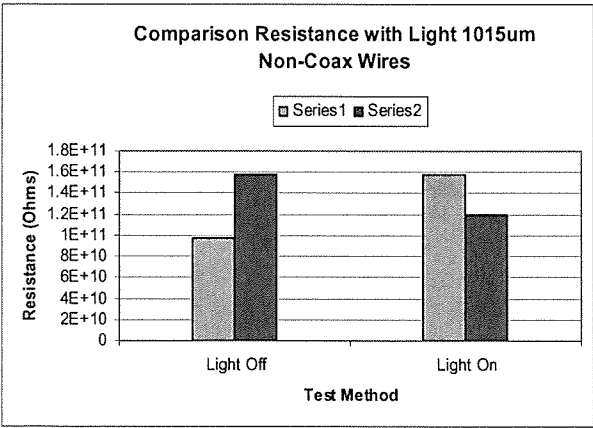


Figure 10 - Light Exposed/Unexposed for same devices

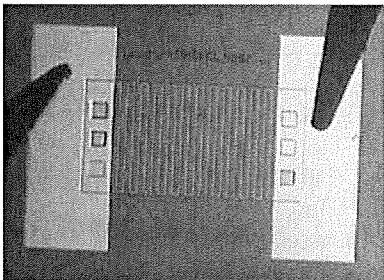


Figure 11 - Unfilled Trenches, process issues

A specific process issue was found through testing, where certain devices did not have completely filled contact cuts, resulting in noisy and non-linear I-V characteristics, see Figure 11. This device would not pass the QC of Rostir, Inc. The device was found on the edge of the wafer and the issue was not prevalent across other die.

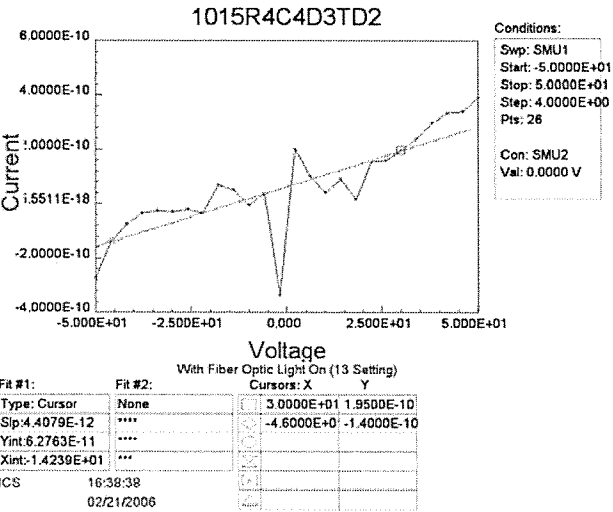


Figure 12 - Noise Issues

Most testing issues devices regard noise due to the small current levels where any stray EMF or vibration affected the testing results, see Figure 12. To address this issue an Insulated box and Coaxial wires and probes were used, see Figure 13. This setup allowed for a more robust testing

process and build confidence in to the testing model. Figure 14 depicts the I-V Characteristic post using insulated test setup, there was no noise from this test, however it still shows a rolling initial resistance.

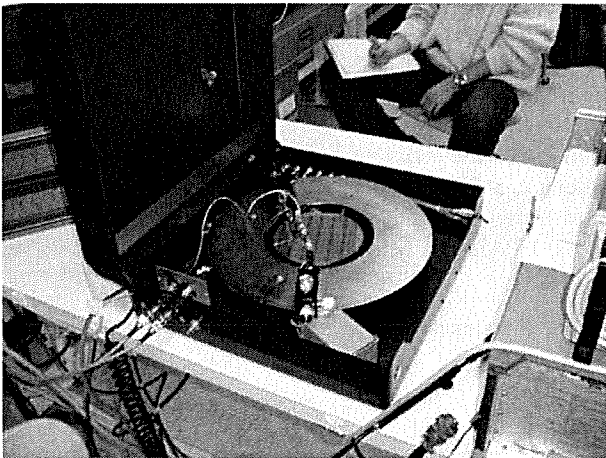


Figure 13 - Image of Insulated box and Coax Probe station

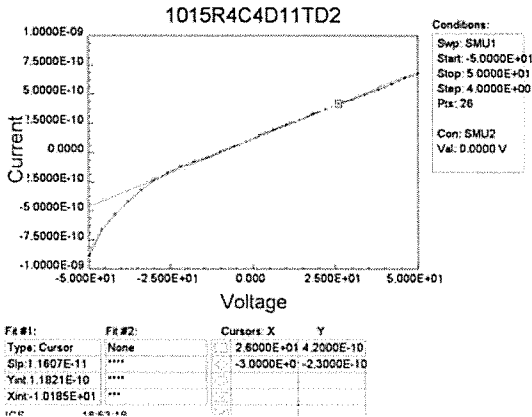


Figure 14 - Insulated Probes provided less noisy results

In order to address the rolling resistances, which were thought to occur due to the metal/poly interface issues or parasitic capacitances. Figure 15 depicts the basic concept of where the parasitic capacitances exist for the devices. It is known that $R_{semi} \ll R_{giga}$, given that R_{semi} is on the order of ohm, therefore is though to have a negligible effect on the resultant value of the chip resistor. The parasitic capacitance, however, does seem to play a role in the resultant I-V characteristic due to the MOS capacitor like structure of these chip resistors, especially since the chip size is defined by the metal contact pads, creating a large MOS capacitor like structure.

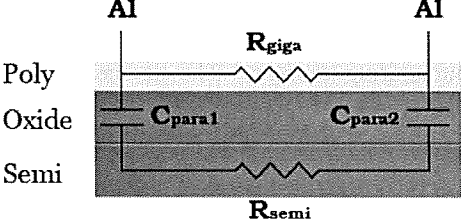


Figure 15 - Basic concept of parasitic capacitances

$$\frac{1}{C_{\text{parasitic}}} = \frac{1}{C_{\text{para1}}} + \frac{1}{C_{\text{para2}}} \quad (5)$$

$$R_{\text{Semi}} \ll R_{\text{Giga}} \quad (6)$$

Equation 5-6 - Parasitic Capacitance and Resistances

Figure 16 shows the value of parasitic capacitances and their range in the across different frequencies. A suspected the large device, 3820um, had a large capacitance than the 2540um across all frequencies. These tests were completed using the HP45275A Multi Frequency LCA Meter.

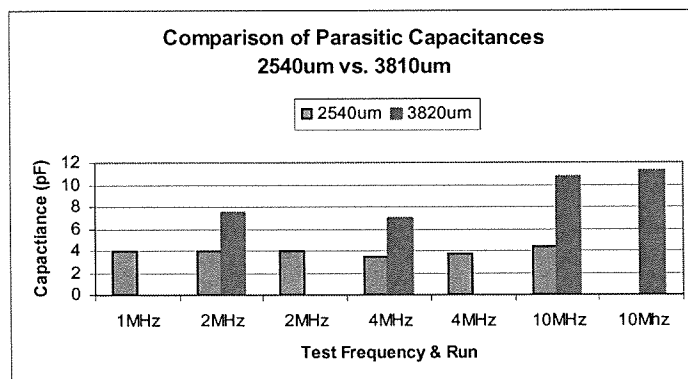


Figure 16 - Comparison of Parasitic Capacitances

The final tests for characterizing the chip resistors included Temperature Coefficient of Resistance (TCR), Voltage Coefficient of Resistance (VCR), and Voltage breakdown. It was found that the TCR of the devices was higher than competitors at a value of 6250ppm/°C to 20 to 2000ppm/°C.^{vi} The VCR of the devices were found to be 5000ppm/V which is inline with competitors which ranged from 3000 to 6000ppm/V.^{vii} Finally the Voltage Rating was tested for 200 V and passed, however in theory the device should be able to withstand 2000V, 1900V for fabricated devices, however no high voltage supply was available.

VI. CONCLUSION

This project investigated the design and fabrication of Ultra-High Value Chip Resistors with a focus on entrepreneurship. Gigaohm values were achieved with an average value of 99.6 Gigaohms. Further funding would be required to fully characterize the Implant process, which would allow Rostir to develop custom valued chips, as well as develop a more robust manufacturing process. The devices were shown to have a TCR higher than competitors, a VCR in line with competitors, and a Voltage rating superior to many competitors. In all, the testing method required evaluate the chip resistors must be re-addressed and implemented for large scale testing. Lastly, integration in the Microelectronic Student Association as a student run business could be implemented and help fund and provide experience for RIT students, in general.

VI. Acknowledgements

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Biography of Researcher:

Jonathan was Co-Founder and a cabinet member (Vice-President/President) of the Collegiate Entrepreneur's Society (CESR) from 2002-2004 where he networked extensively within RIT and outside RIT to help provide resources for the entire student body seeking to learn about entrepreneurship or to start and develop their own businesses. Jonathan also worked with COB faculty and RIT administrators on the RIT Student Incubator and RIT Undergraduate Business Plan Competition which he subsequently won in 2004 with partner Kyle Scholz. Jonathan was also a founding member of CoFu Inc., a software technology firm, in late 2002 with Kyle, which operated in the RIT Student in 2004. Jonathan has also worked for Micron Semiconductor, a Biomedical Device firm Diapulse, and Boston Scientific, a market leader in the development of less invasive biomedical products.