

Workfunction Tuning of Molybdenum Gate by Nitrogen Incorporation (May 2006)

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Abstract—Due to the aggressive scaling of CMOS devices, it is necessary to provide a metal gate solution to replace the conventional process known as a self-aligned poly-silicon gate. Molybdenum (Mo) possesses several properties that make it attractive as a CMOS gate electrode material. In addition, Mo has been identified as a candidate for “single-metal / dual-workfunction” technology, with the ability to tune the workfunction by the introduction of nitrogen. In this study, the correlation between workfunction of the Mo gate and the incorporation of nitrogen was investigated. The flat-band voltage shift was extracted from the obtained C-V Characteristic curves. Both reactive sputtering and ion implantation methods provided a negative shift in the C-V characteristics. The observed shift was greater for the ion implantation methods. These results indicate that a Mo-gate process with incorporation of nitrogen is a good candidate for replacing the self-aligned poly-silicon gate process.

Index Terms—Molybdenum, Dual-workfunction, single metal gate, nitrogen implantation

I. INTRODUCTION

THE requirements for faster, smaller, and inexpensive electronics in this high technology world are mainly the driving forces for increasing the packing density and enhancing the speed of microelectronic devices. The primary technique used to fulfill these demands is scaling of devices. To allow further scaling and improve the transistor performance, it is necessary to bring new materials into the transistor arrangement for upcoming CMOS devices. The scaling is carried out by following certain rules or principles to reduce the transistor design without reducing its performance. In spite of following these rules, problems will arise in time.

The scaling requirements for upcoming CMOS generations are generally directed by the International Technology Roadmap for Semiconductors (ITRS). Every other year, the ITRS identifies the technological confrontations and necessities. In ITRS, the scaling factors generally fall within two main application classes – high performance and low

power [consumption]. For high performance model, the main aim is to maximize the performance (speed) of devices. Generally aggressive scaling is used to achieve this goal. For low power model, the main aim is to minimize the chip power consumption. The 2005 ITRS predicts that the polysilicon gate electrode will be replaced with alternative materials by 2008 [1]. The reason for this prediction is that the scaling of channel length and gate oxide thickness in a conventional transistor heightens the problems of high gate resistivity, polysilicon gate depletion effect (thus reducing drive current), high gate tunneling leakage current, and boron penetration into the channel region. Thus, the incorporation of a metal gate technology will be necessary for future CMOS devices.

To choose alternative CMOS gate electrode materials, several aspects must be addressed:

1. *CMOS process compatibility* (such as thermal stability of material during high temperature annealing steps / etching).
2. *Influence on gate dielectric reliability*
3. *Compatibility with advanced technology in future* such as use of high-k gate dielectric materials. Since ultra thin SiO₂ gate oxide has presented reliability concerns, use of high-k dielectric materials has been the focus of many recent papers [2].
4. *Appropriate gate work functions*. In order to keep good short channel performance and working threshold voltage, it is important that the gate work functions of the n-FETS and p-FETS are close to those of n⁺ and p⁺ doped poly-Si for bulk-Si CMOS devices.

It is not a simple task to introduce new materials into the complex and well established conventional fabrication. For successful implementation, newly formed metal gate technology should be compatible with standard CMOS processing with respect to process integration as well as thermally and chemically stable. In addition, process which develops uniform damage-free deposition and etching, and selective etching process to prevent layer and mask resources will be necessary.

Several material techniques and process incorporation methods for achieving multiple gate work functions (and thus replacing poly-Si gate process) have been investigated up to date [2]. These include: use of single metal gate, use of dual metal gate, and use of fully silicided doped poly-Si. Out of these material techniques and process incorporation methods for achieving multiple gate work functions, a process using single metal gate has the simplest process requirement. Use of

single metal gate step process, however, need to be carefully considered. That is the working set of work functions is needed in order to replace polysilicon gate electrode process to metal gate process. In CMOS transistors, p- or n-type doped polysilicon is used. The work function generally comes out to be 5.2 eV for p-type and 4.1 eV for n-type [3]. To achieve the favorable performance of the transistors, it is required to have correct work functions of metal gate.

II. MOLYBDENUM METAL GATE

Among several candidates, Molybdenum was chosen to be a possible candidate to be used in a single-metal dual gate work function technology provided that an adequate and stable work function shift can be obtained. Molybdenum is the possible candidate for metal gate process for several reasons. Molybdenum has characteristic of having a high melting point of $\sim 2610^\circ\text{C}$ and low coefficient of thermal expansion of $5 \times 10^{-6} / ^\circ\text{C}$ at 20°C . The thermal processing processes generally performed in a CMOS fabrication processes can be endured by this characteristic held by Molybdenum. In addition, Molybdenum gate provides significant reduction in gate resistance as compared to doped polysilicon gate. This is due to Molybdenum being one of the most conductive refractory metals. Molybdenum possesses high stability in contact with SiO_2 at high temperature [6]. Thin films of Molybdenum with (110) crystallographic texture have been shown to exhibit work function close to 5 eV on several candidate dielectrics (hi-k dielectric). These properties endure the thermal budget used throughout the conventional CMOS processes.

For single metal process, it is impossible to find a metal that possesses two different work functions; molybdenum is no exception. Therefore, several methods need to be investigated for incorporating Molybdenum metal gates to conventional CMOS technology. In this study, the correlation between the work function of Molybdenum and incorporation of Nitrogen was investigated. The methods used to incorporate nitrogen were ion implantation and reactive sputter deposition.

Reactive sputter deposition of Mo with the introduction of nitrogen in the ambient results in the deposition of Mo_xN_y (a stoichiometric molybdenum nitride is MoN). The nitrogen gas flow (ratio to argon) was varied in order to investigate the influence on the gate workfunction. While this technique would not enable a dual workfunction material, it was used as an initial test of the chemical influence of nitrogen, avoiding the influence structural changes induced by ion implantation. Ion implantation of nitrogen into deposited Mo was also performed, followed by high temperature annealing. Using X-ray diffraction (XRD), previous work has shown that significant amorphization occurs during the implantation, and recrystallization happens during subsequent high temperature annealing steps. In addition, considerable segregation of the nitrogen at the Mo/SiO_2 interface could result from the nitrogen implantation and the high-temperature annealing process. Either of these events may be the mechanism responsible for inducing a workfunction shift [4].

III. PROCESS / FABRICATION

A. Treatment Combinations

In this study, Mo capacitors were fabricated with different treatment combinations, as shown in Table 1 and Table 2.

TABLE I
TREATMENT COMBINATION USED FOR THE NITROGEN
REACTIVE SPUTTERING PROCESS

#	N Gas Flow	Ar Gas Flow	Nitrogen %
1	0 sccm	21.6 sccm	0 %
2	2 sccm	18 sccm	10 %
3	3.8 sccm	15.12 sccm	20 %
4	7 sccm	10.51 sccm	40 %

TABLE II
TREATMENT COMBINATION USED FOR THE NITROGEN
IMPLANTATION PROCESS

#	Implant Dose (cm^{-2})	Anneal Temp ($^\circ\text{C}$)
1	1.00×10^{15}	No Anneal
2	5.00×10^{15}	No Anneal
3	1.00×10^{16}	No Anneal
4	1.00×10^{15}	600
5	5.00×10^{15}	600
6	1.00×10^{16}	600
7	1.00×10^{15}	700
8	5.00×10^{15}	700
9	1.00×10^{16}	700
10	1.00×10^{15}	800
11	5.00×10^{15}	800
12	1.00×10^{16}	800

B. Process Flow

The major process steps included sheet resistance measurement, thermal gate oxide growth (500Å), Mo deposition with and without reactive sputtering, nitrogen implantation (half of the wafer), LPCVD low temperature oxide (LTO), high-temperature thermal annealing, aluminum evaporation (quarter of the wafer), lithography (capacitor gate definition), etch and sinter. A C-V characteristic curve was extracted for each process. Fig. 1. shows the location of different metal gates within the wafer. Different metals were configured this way so that pure Mo gates and aluminum gates could be used to create reference capacitance-voltage (C-V) characteristics.

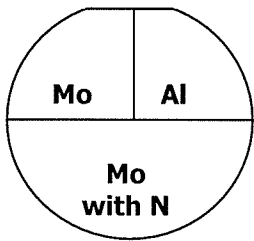


Fig. 1. The location of different metal gates within each wafer. Mo = molybdenum / Al = aluminum

1) *Molybdenum Deposition*: PE 2400A RF sputtering tool was used to deposit 1500 Å of Molybdenum. For reactive sputtering, the nitrogen gas flow (ratio to argon) was varied. Base pressure, depositing pressure, power, and time was held consistent to make sure that only factor influencing the flat-band voltage shift is due to the nitrogen gas flow. For the nitrogen implantation process, nitrogen implantation energy and anneal temperature was varied. Everything except for those two factors were held consistent to make sure that only they were influencing the flat-band voltage.

2) *Nitrogen Implantation*: implant energy of 80 keV and implant species of ¹⁴N⁺ was used during the nitrogen implantation. Fig. 2. shows the linear SRIM model for nitrogen ion in Molybdenum with implant energy of 80 keV. With this nitrogen implant energy, it was assumed that nitrogen will be mostly implanted in the middle of molybdenum metal, thus not causing any implant damage on dielectric material and/or silicon.

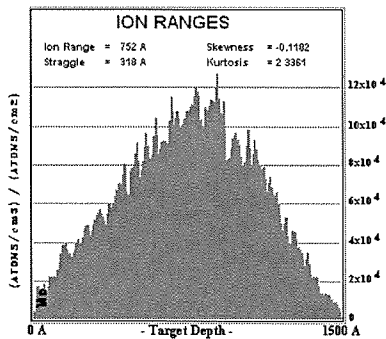


Fig. 2. The linear SRIM model analysis for nitrogen ion in Molybdenum with implant energy of 80 keV. Molybdenum thickness of 1500Å was used for this analysis. The peak ion concentration was occurred at 752Å which was close to the middle of the molybdenum metal.

3) *LPCVD low temperature oxide (LTO) Deposition*: Mo oxidizes in high temperature oxygen ambient, due to a poor quality of Mo fabricated in our laboratory. Mo oxidizes even in a sintering recipe (no oxygen ambient / low temperature recipe). LTO was needed to be used as the protecting layer. Fig. 3. shows the picture of molybdenum wafer with LTO on the half of the wafer. This wafer was first deposited with 1500Å of Mo then was put in Bruce furnace (annealed in

600C° for 15 minutes). Left half of the wafer was protected with 500Å of LTO, whereas right half of the wafer was not protected. The side with LTO was not oxidized and conductive, but the side without LTO was partially oxidized and exhibited the less conductive surface. Several tests were made (shown in TABLE III) with different temperature and LTO thickness to choose the proper LTO thickness to protect Mo surface.

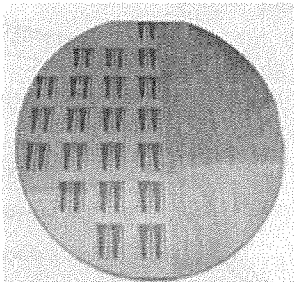


Fig. 3. The picture of molybdenum wafer after the annealing step (600C°). The left side was protected with 500Å of LTO, whereas the right side was not protected. The left side stayed conductive, but the right half was oxidized.

TABLE III
OXIDATION INVESTIGATION:
DIFFERENT LTO THICKNESS / DIFFERENT TEMPERATURE

#	LTO Thickness	Recipe / Temperature
1	500A	Sinter / 425C°
2	500A	Anneal / 600C°
3	500A	Anneal / 800C°
4	1000A	Anneal / 800C°

From this investigation, it was found that 1000Å of LTO was a good protection for the sintering and 600C°/800C° annealing step.

IV. RESULTS/ANALYSIS

The sheet resistance of twelve different wafers were measured and shown in TABLE IV. Sheet resistance of wafers were made sure to be consistent, since difference in these values can shift the C-V curves itself. As shown in TABLE IV, sheet resistance of twelve different wafers came out to be really close with values of 97 to 105 ohms/square.

TABLE IV
RESMAP SHEET RESISTIVITY MEASUREMENTS

#	RS (ohms/square)
1	102.7
2	104.0
3	100.9
4	100.8
5	97.89
6	98.34
7	100.7
8	103.2
9	103.4
10	100.5
11	100.5
12	97.11

Fig. 4. shows the Capacitance-Voltage (C-V) characteristic curves for the nitrogen reactive sputtering process. Increasing in nitrogen flow appears to give negative shift to the CV curve. A lateral shift is consistent with a workfunction change. This could also be due to interface charge differences.

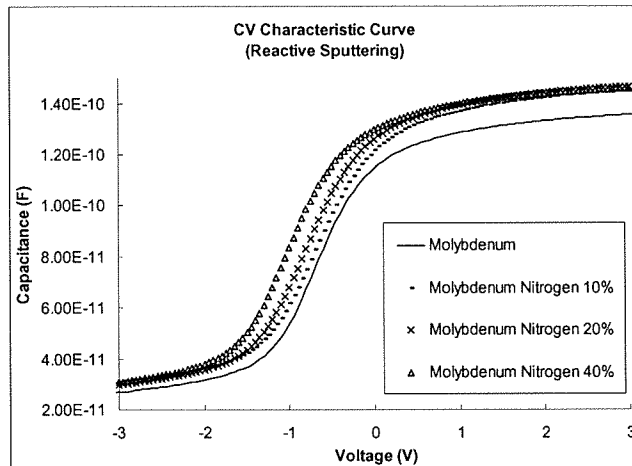


Fig. 4. Capacitance-Voltage characteristic curves for the nitrogen reactive sputtering process.

Using Fig. 4, the flat-band voltage shift was extracted and shown in TABLE V and Fig. 5. Increasing the nitrogen flow gave larger negative flat-band voltage shift.

TABLE V
V_{FB} SHIFT FOR REACTIVE SPUTTERING PROCESS

Nitrogen %	V _{fb} Shift
10%	- 0.05 V
20%	- 0.15 V
40%	- 0.35 V

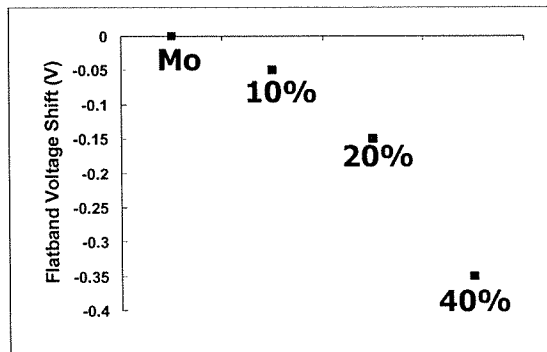


Fig. 5. V_{FB} shift for the reactive sputtering process. Increasing the nitrogen flow gives larger negative flat-band voltage shift.

Fig. 6. shows the Capacitance-Voltage (C-V) characteristic curves for the nitrogen implantation process. The certain implant/anneal treatment combinations resulted in degraded C-V characteristics. The C-V curves shown in Fig. 6. are representative characteristics for several treatment combination that actually exhibited the C-V response.

Distortion (broader slope) as nitrogen dose increases supports increased levels of interface traps. In addition, the influence of temperature was confounded with the nitrogen dose. It was very unusual that the other treatment combinations exhibited failure, yet these three measurable treatment combinations involved the three different nitrogen doses investigated – and each one at a different temperature. This indicates a strong interaction effect that is not understood.

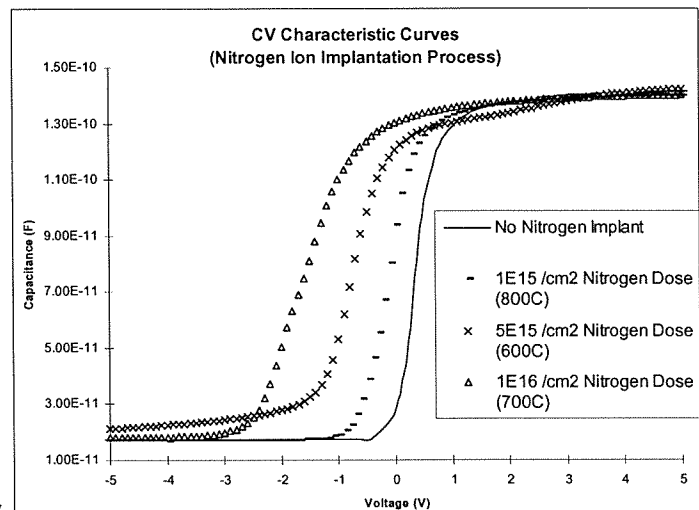


Fig. 6. Capacitance-Voltage characteristic curves for the nitrogen implantation process.

Using Fig. 6, the flat-band voltage shift was extracted and shown in TABLE V and Fig. 7. Increasing the nitrogen dose gave larger negative flat-band voltage shift.

TABLE VI
V_{FB} SHIFT FOR NITROGEN IMPLANTATION PROCESS

Nitrogen Dose	V _{fb} Shift
1X10 ¹⁵ cm ⁻²	- 0.6 V
5X10 ¹⁵ cm ⁻²	- 1.05 V
1X10 ¹⁶ cm ⁻²	- 2.0 V

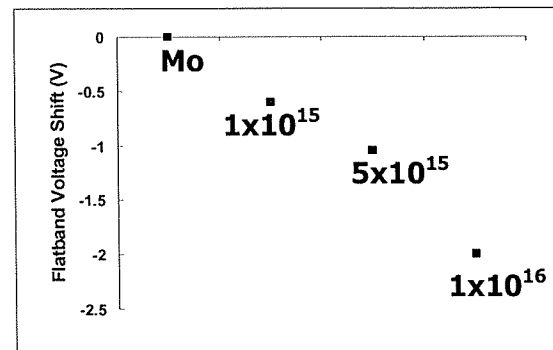


Fig. 7. V_{FB} shift for the nitrogen implantation process. Increasing the nitrogen dose gives larger negative flat-band voltage shift.

Fig. 8. shows the log scale SRIM model for nitrogen ion in Mo at 80 keV. This analysis was done to find out why for several treatment combinations, C-V curves came out to be

degraded. It was found that the implant damage on SiO₂ was actually severe with value of 1×10^{19} atoms/cm³. This could have caused oxide charge and/or interface damage from implantation step and degraded several C-V curves.

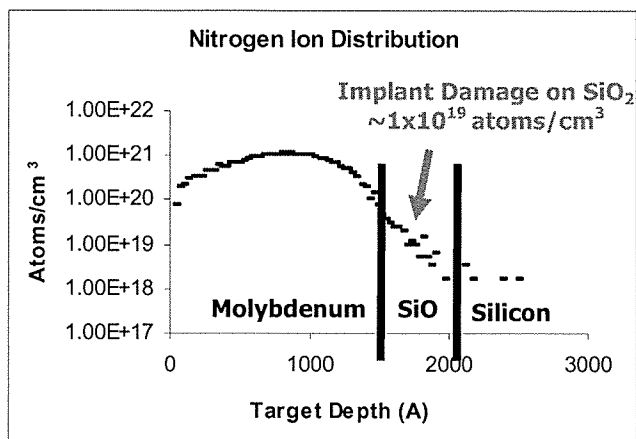


Fig. 8. The log scale SRIM model for nitrogen ion in Molybdenum. Implant damage on SiO₂ was found out to be in the range of 1×10^{19} atoms/cm³

V. CONCLUSION

A. Both reactive sputtering and ion implantation methods provided negative shifts in CV curves (either by more nitrogen gas flow or dose). Shift was greater for the ion implantation methods. For the reactive sputtering method, -0.05 to -0.35V V_{FB} shift was observed to be dependent on the % nitrogen in the ambient. A lateral shift is consistent with a workfunction change. For the nitrogen implantation process, large V_{FB} shift (-0.6 to -2.0V) was observed. However, severe implantation dose might have caused interface damage. Interface trapped charge could be held responsible for a large portion of the threshold shifting observed.

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