Fabrication and Test Characterization of Organic Poly(3,3''' dialkylquaterthiophene) (PQT-12) Transistors

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Abstract—**Organic thin film transistors (OTFTs) are fabricated as bottom gate, top contact devices unlike conventional integrated circuits. Transistors of various dimensions with a top organic polymer layer that acts as a semiconductor known as poly(3,3''' dialkylquaterthiophene) (PQT-12) have been fabricated and electrically tested. Two processes have been designed prior to spin coating the PQT polymer: a) four heavily doped boron wafers using the back of the wafer as a gate with aluminum and chrome source/drain metal options and b) five moderately doped boron wafers with molybdenum or chrome gates with aluminum or molybdenum source/drains. The devices fabricated on the heavily doped boron wafers performed unfavorably compared to the devices fabricated with metal gates. The threshold voltages (V_T) for the devices that exhibited device transfer characteristics were extrapolated approximately -8.5 to -9.0 V. The devices with wafer gates show that Al as a source/drain metal exhibited high gate leakage where V_T occurs between -12.0 V to -25.0 V.**

I. Introduction

Recently, much attention has been focused on applications of organic thin film transistors as they can be used as low-cost alternatives to amorphous silicon technologies for printed electronics [1]. For large-area devices and low-cost microelectronic applications where high computer powers or switching speeds are not needed, silicon IC technologies become unnecessary and expensive. Plastic ICs composed of organic transistors can potentially be manufactured at low cost by solution processes such as coating, stamping, printing, etc [2]. Fabricating ICs via jet printing is particularly efficient and environmentally friendly as it is a direct-write process, and is suitable to the productive reel-to-reel manufacturing procedures [2]. Organic transistors are also well-suited with flexible substrates, thus allowing fabrication of compact, lightweight, flexible, and efficient micro-electronic products.

Organic thin-film transistors (OTFTs) fabricated using solution-deposition techniques (e.g. spin-coating, screen printing, inkjet printing) may also be attractive for low-end electronic devices (e.g. radio frequency identification tags) where the high cost of packaging silicon circuits becomes restrictive. For important useful applications, these OTFTs need to provide field-effect transistor (FET) mobilities close to that of amorphous silicon [3]. This will require establishment of proper molecular order in the semiconductors to achieve high mobilities [4,5], since charge-carrier transport in organic semiconductors is dominated by hopping [6], and disordered materials are not efficient charge-transporting media.

The simplicity of OTFT designs make them cost effective thus allowing less demanding fabrication steps. It is necessary for OTFTs to possess proper molecular ordering that enables their charge carrier transport [7]. PQT-12 (Figure 1. (a)) polymer cast in dichloro-benzene gives rise to a three-dimensional (3D) lamellar stacking network (Figure 1. (b)) [8]. This special preparation allows PQT-12 to act as a semi-conductor that exhibits charge transport capabilities. Prior to applying a PQT-12 layer, a priming layer known as Octyltrichlorosilane, 8 (OTS-8), facilitates the adhesion of the polymer and promotes its lamellar stacking order (Figure 2).

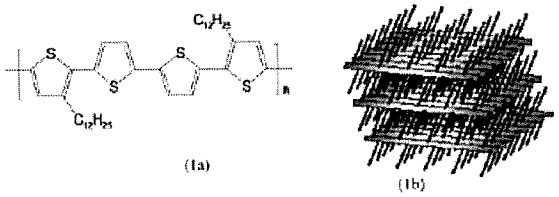


Figure 1. PQT molecular structure shown as a) a 2-D structure and b) 3-D rod-shaped lamellar stacking structure. [8]

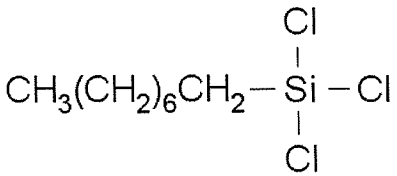


Figure 2. Chemical formula of Octyltrichlorosilane (OTS-8)

II. Process

A designed experiment consisting of nine devices wafers has been implemented in this study. Five moderately doped boron (p) wafers (5 – 25 Ω·cm) with cross sections shown in Fig. 2 have been processed with the following layers: an oxide foundation, a patterned chrome or molybdenum metal gate, a LTO gate, an aluminum or molybdenum source and drain, an OTS-8 priming layer, and a PQT-12 polymer layer.

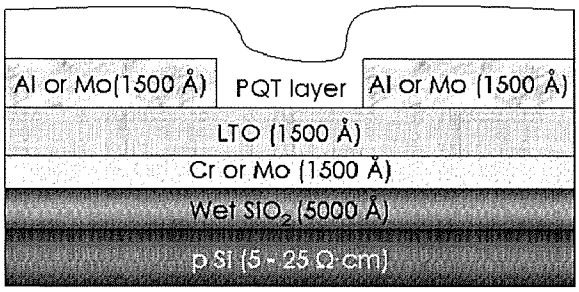


Figure 2. Cross section schematic of five moderately doped p-type wafers

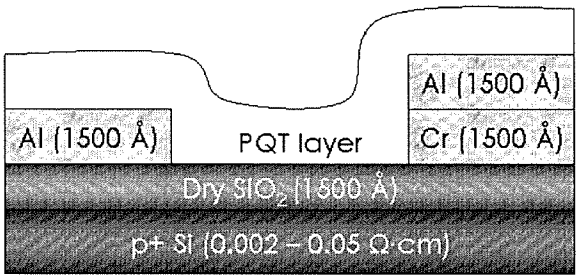


Figure 3. Cross section schematic of four heavily doped p-type wafers

Four heavily doped boron (p+) wafers (0.002 – 0.05 Ω·cm) using silicon as the gate with cross sections show in Figure 3 have also been processed with the following layers: a dry oxide gate, a chrome/ aluminum source and drain, an OTS-8 priming layer, and a PQT-12 polymer layer. The thicknesses of each processed layer are also shown in Figures 2 and 3.

The four heavily doped boron wafers were fabricated with two commonly used metals in the semiconductor industry (aluminum and chrome) that act as the source/drain of the device. The purpose of this design is to test the performance of this type of device in comparison to devices with only one source/drain metal (aluminum). This approach may demonstrate asymmetric source/drain operation due to different metal-semiconductor contact behavior.

The five moderately doped p-wafers have chrome or molybdenum gates, which are two commonly used gate metals in TFT technology. Aluminum was not chosen as a gate material as various studies have indicated that its surface topography tends to be rougher than chrome or molybdenum making it a poor interface for a bottom gate layer. In order to avoid a high temperature oxidation step, a layer of LTO has been deposited as the gate dielectric and a conventional source/drain metal was patterned.

Prior to coating all wafers with PQT-12, an OTS-8 priming layer has been applied in order to enhance adhesion of the polymer and promote its lamellar stacking order. Each wafer was submersed in 0.1 M OTS-8 in Toluene for 20 minutes at 60°C, rinsed in isopropanol for five minutes, and air dried from the method discussed in [9]. PQT-12 was then spin coated at 300 rpm for 60 seconds on each wafer. The wafers were then treated with a vacuum oven annealing step at 145°C for 30 minutes. Figure 4 is an example of an Atomic Force Microscopy (AFM) image taken of a PQT-12 polymer after being annealed at 145°C for 30 minutes and cooled to 25°C for two hours [3].

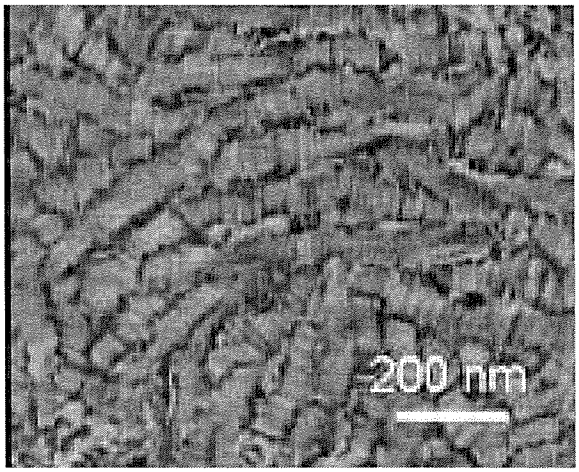
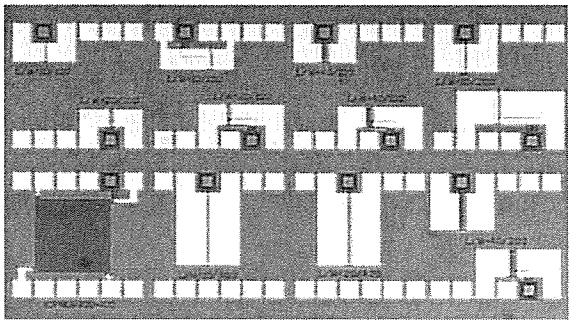


Figure 4. Atomic force microscopy (AFM) image of PQT-12 films on OTS-8 treated SiO_2 surfaces annealed at 145°C for 30 minutes and cooled to 25°C over a period of 2 hours. [3]

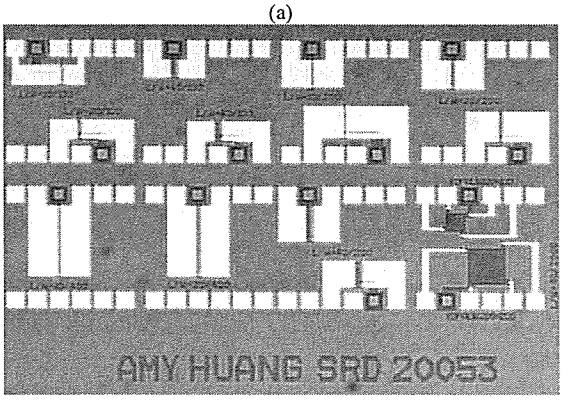
III. Results and Analysis

Transistors of various dimensions (L x W) ranging from 20 x 100 μm^2 to 100 x 3000 μm^2 and Van der Pauw structures that determine the sheet conductance have been fabricated and tested. Figure 5 (a) through (c) are screen captures of the devices taken under a 20x Leitz microscope.

The device dimensions that have been studied for comparison during electrical testing were 10 x 400 μm^2, 20 x 2000 μm^2, and 40 x 2000 μm^2. The smaller devices have proved to be more difficult to manually probe with conclusive results.



(a)



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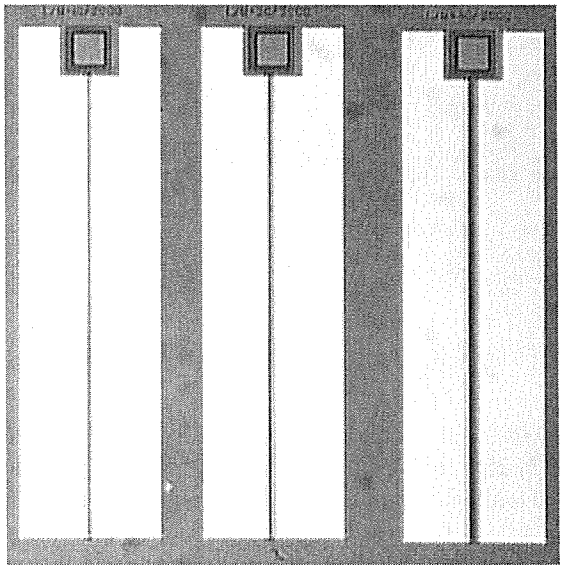
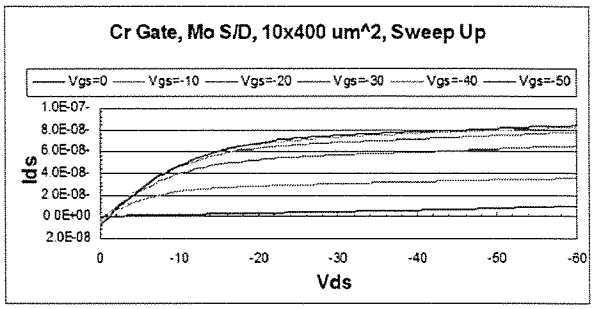


(c)

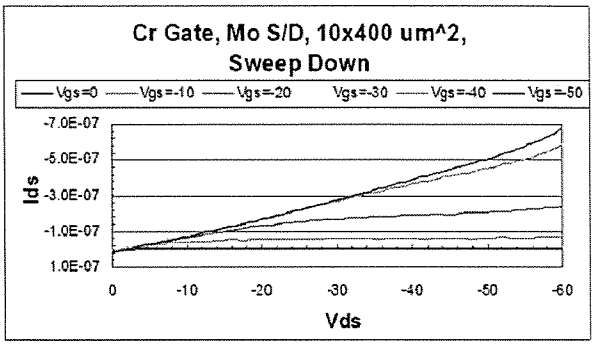
Figure 5. Screen captures of (a) 10 x 100 μm² to 40 x 200 μm² with Van der Pauw 400 x 400 μm², (b) same structures with Van der Pauw 100 x 100 μm² and 200 x 200 μm², and (c) 10 x 2000 μm², 20 x 2000 μm², and 40 x 2000 μm².

Every device tested has exhibited PMOS behavior. The heavily doped p-type wafers demonstrated noisy electrical behavior due to the back side of the wafer acting as the gate (not shown). The gate being present everywhere caused noise during testing and the integrity of the device was sacrificed. The effect of having two different source/drain metals on charge carrier transport could not be tested.

The family of curves data in Figure 6 (a) and (b) demonstrate that the sweeping direction of drain-source potential (V_{DS}) causes a strange behavior in device operation. Figure 6 (c) shows that V_T is extrapolated to be -8.52 V due to the device being relatively large in comparison to conventional ICs.



(a)



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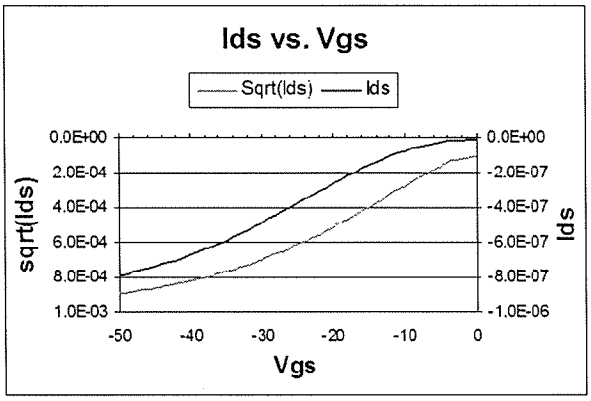
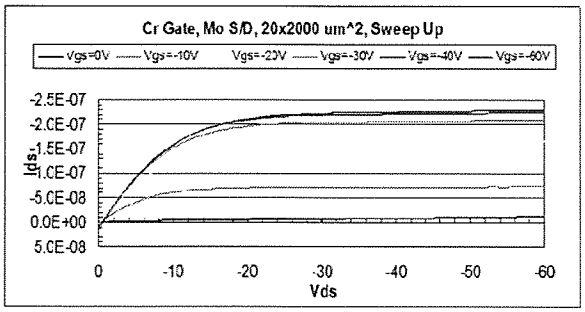


(c)

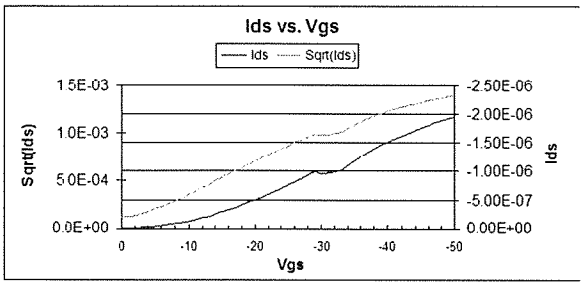
Figure 6. Electrical data of (a) family of curves sweeping V_{DS} from 0 to -60 V on a chrome gate, molybdenum S/D device with 10 x 400 μm², (b) family of curves sweeping V_{DS} from -60 to 0 V on the same device, and (c) I_{DS} vs. V_{GS} curve with a V_T of -8.52 V.

Chrome and molybdenum gate contacts have been compared for 20 x 2000 μm² devices in Figure 7 (a) through (d). There is no notable difference between using either type of metal, though the molybdenum gate carries greater current than chrome for the same device (Figure 7 (a) and (c)). In both I_{DS} vs. V_{DS} curves, a dip in current exists between -30 to -35 V shown in Figure 7 (b) and (d). This is possibly due to

contact interface issues or polymer shelf life degradation.



(a)



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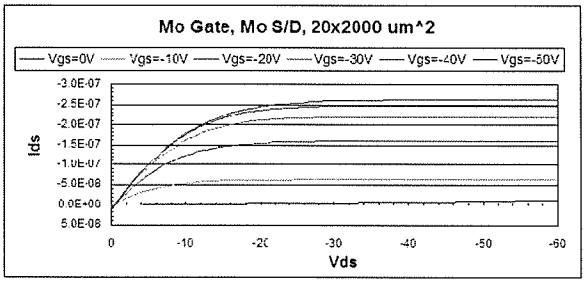

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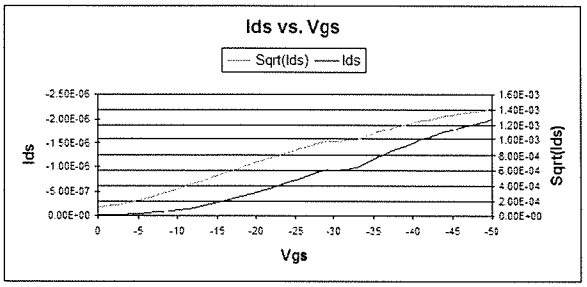
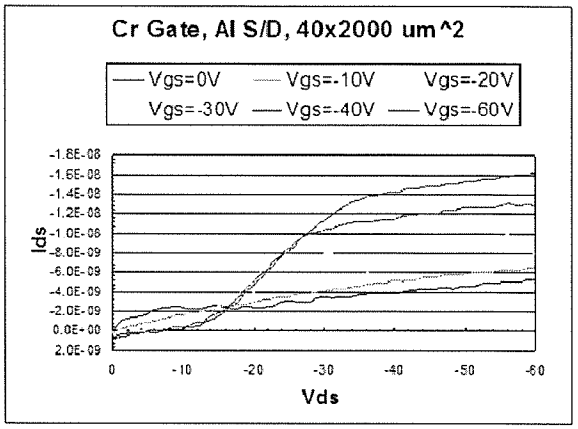


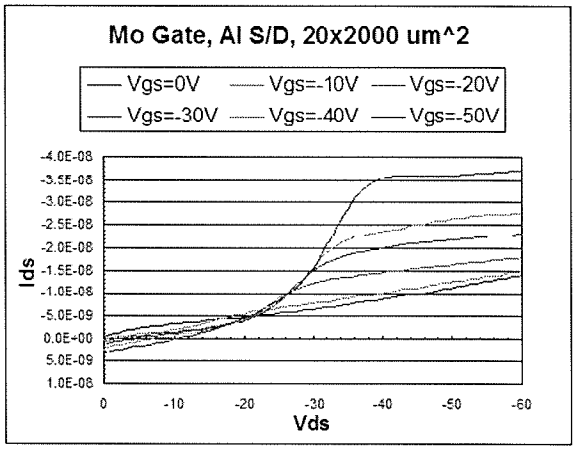
(d)

Figure 7. Electrical data of (a) 20 x 2000 μm^2 chrome gate, molybdenum source/ drain device, and (b) its I_{DS} vs. V_{GS} curve, (c) 20 x 2000 μm^2 molybdenum gate with molybdenum source/drain device, and (d) its I_{DS} vs. V_{GS} curve.

Figure 8 (a) through (c) all exhibit high gate leakage where device operation occurs late where V_T is typically between -12 to -25 V depending on the dimensions of the device. All three devices use aluminum as their source/drain metal. This recurring behavior supports the conjecture that molybdenum is a superior source/drain metal as well as a superior gate metal compared to aluminum for organic PQT-12 transistors.



(a)



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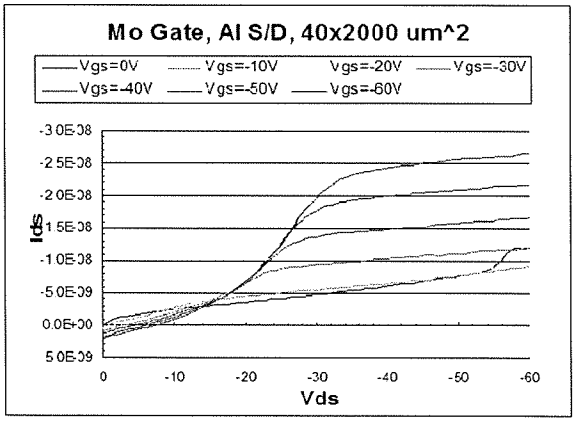

(c)

Figure 8. Family of curves data for (a) 40 x 2000 μm^2 chrome gate with aluminum source/drain, (b) 20 x 2000 μm^2 molybdenum gate with aluminum source/drain, and (c) 40 x 2000 μm^2 molybdenum gate with aluminum source/drain.

Testing conditions such as lighting, integration time (short, medium, long) and V_{DS} sweep direction (high to low or low to high in magnitude) may have an effect on the device transfer characteristics. The light turned on minimized noise in test data, which

indicates that PQT-12 polymers are photoactive. Optimal family of curves data were captured using medium integration times, the microscope and ambient light on, and sweeping V_{DS} from low to high (0 to -60 V).

IV. Conclusions

Transistors and test structures of various dimensions have been designed on a four-quadrant mask and PQT-12 devices have been successfully fabricated and tested. Electrical data for the heavily doped p-type wafers exhibited noise due to the back side of the wafer acting as the device contact. The electrical data show that 10 x 400 μm^2 moderately doped p-type wafer devices have a V_T of -8.52 V. Compared to chrome gates, molybdenum gates generate higher current. The electrical behavior of devices also demonstrated that molybdenum is a superior source/drain metal compared to aluminum. Devices with aluminum source/drains exhibited high gate leakage and poor turn on potentials between -12 to -35 V. Optimal testing conditions include using medium integration times, the microscope and ambient light on, and sweeping V_{DS} from low to high (0 to -60 V). The dynamic hystereses of PQT-12 polymer as a semiconductor data require further investigation to explain its behavior.

References

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