Formation of Self-Aligned Shallow Junction MOSFET Source/Drains by Proximity Rapid Thermal Diffusion

Scott W. Kenny

Abstract— The creation of short-channel length MOSFET's requires shallow junctions and thin gate dielectrics to maintain long channel behavior. The focus of this paper is the creation of shallow source/drain junctions by Proximity Diffusion with Rapid Thermal Processing (RTP). PMOS devices were fabricated using Borofilm 100 Spin on Dopant with temperatures of 950° and 1000° for 10 and 20 seconds ramped at 30 degrees per second. The source and drain regions are defined by the patterned polysilicon gate, which is also doped during this process. A 100 Å gate oxide is used, incorporating nitrogen to reduce boron diffusion through the gate. The devices were tested and working transistors were found down to 0.6 micron mask defined gate lengths. The threshold voltage for these devices was found to be -3.1 Volts. Samples sent out for analysis by Secondary Ion Mass Spectrometry (SIMS) to profile the boron diffusion. The approximate junction depth was found to be between 30 and 40 Å for the sample ran at 950° C for 10 seconds

***Index Terms*—Proximity diffusion, Rapid Thermal Processing (RTP), shallow junctions, device scaling**

I. Introduction

The demands of the semiconductor industry push device sizes ever smaller. To continue the trends of the past 40 years materials and processing obstacles will have to be overcome. The creation of short-channel length MOSFET's requires shallow junctions and thin gate dielectrics to maintain long channel behavior

Power supply voltages and electric fields do not scale nicely with device dimensions. Some potential problems with smaller dimensions are hot carrier injection, punchthrough breakdown between source and drain, gate oxide breakdown, and other short channel effects. Brews et al. took this up and developed an empirical relation for a minimum channel length to maintain long channel behavior, Eq. (1). [1]

$$L_{\min} = A[x_j t_{ox}(w_x + w_d)^2]^{1/3} \quad (1)$$

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$$w_d = \sqrt{2}L_B[\beta(V_{DS} + V_{bi} + V_{BS})]^{1/2} \quad (2)$$

L_{min} is the minimum channel length required, A is a proportionality factor, x_j is the junction depth, t_{ox} is oxide thickness, and $(w_s + w_d)$ is the sum of source and drain depletion depths, as described by equation (2):

$$L_B = \sqrt{\frac{\epsilon_s}{\beta q N_A}} \quad (3)$$

where the bulk Debye length is shown is equation (3) and $\beta = (kT/q)^{-1}$. V_{DS} is the drain-source voltage, V_{bi} is the build in voltage, and V_{BS} is the body to source bias.

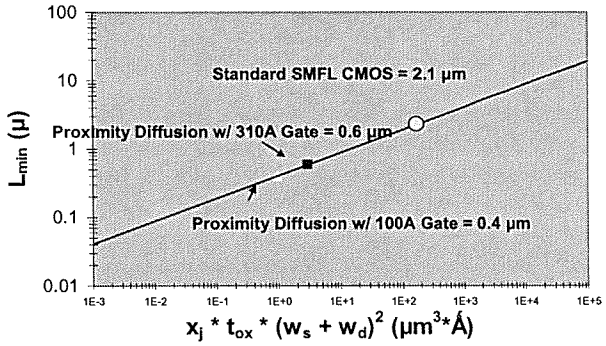

Fig. 1 This figure shows the relationship between junction depth, gate dielectric thickness, doping levels and the minimum channel length to maintain long-channel behavior. The standard SMFL CMOS process is shown (2.1 microns) and the process used in this project (0.4 microns). [1]

Traditionally, doping has been performed by ion implantation. The formation of shallow, highly doped junctions requires a low thermal budget and large dose. Ion implantation induces damage in the implanted substrate that requires a separate annealing step to repair this damage as well as activate the dopants. Proximity diffusion performed with rapid thermal annealing produces little damage to the substrate and eliminates the need for a separate thermal annealing step. The resulting dopant profile is both highly

doped and shallow due to the limited thermal budget and lack of transient diffusion.

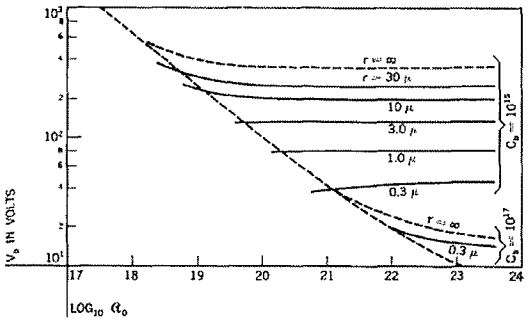

Fig. 2 Figuring showing relationship between a shallow junction depths and small radius of curvature and decreasing junction breakdown voltage. [2]

Fig. 2 shows the reduction in junction breakdown voltage as a function of shallower junction depths. This is due to the resulting electric field from the decreased radius of curvature.

II. Proximity Diffusion

Proximity uses inert disk, such as a wafer in this case, with a deposited SOD layer. The source wafer is prepared by coating Borofilm 100 ramped to 3000 RPM. It is then baked at 200°C for 20 minutes in an air ambient.

The device wafer is HF dipped to remove any native oxide, and placed in an AG 610A Rapid Thermal Processor separated from the source wafer by 300 micron silicon carbide spacers. This setup is shown in fig. 3.

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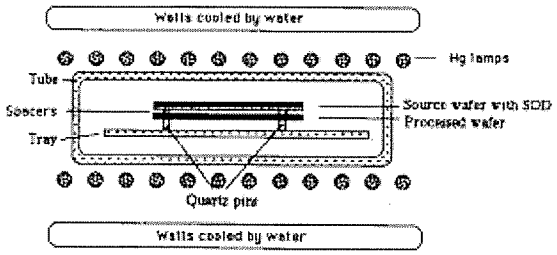


Fig. 3 An illustration of proximity diffusion being performed in an RTP system. [3]

The temperature is then ramped at 30° C per second up to the soak temperature. As the wafers are heated the Boron in the SOD layer diffuses out of the source wafer and is absorbed onto the device wafer by gas phase transport. A small surface reaction occurs resulting in a thin oxide. The Boron then diffuses into the device wafer.

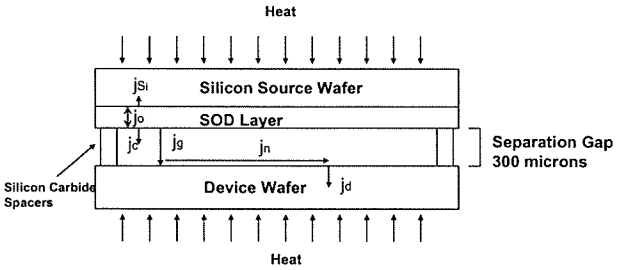
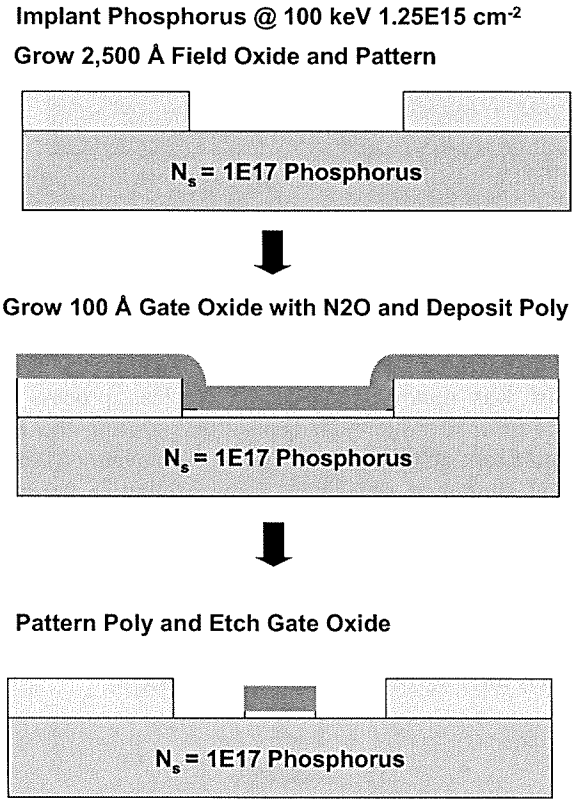


Fig. 4 A zoomed in view of the proximity diffusion process. The various dopant fluxes are labeled. [3]

III. Device Fabrication

The process flow is shown in fig. 5. The n-well doping is ion implanted to a surface concentration of $1x10^{17}$ cm^{-3}. A field oxide is grown and patterned. The 100 Å gate oxide incorporated nitrogen to limit boron diffusion through the gate into the channel. Polysilicon is deposited and patterned. The proximity diffusion process is done forming the source/drain regions as well as doping the poly gate. Finally, a TEOS ILD is deposited, contact cuts etched, and aluminum sputtered.



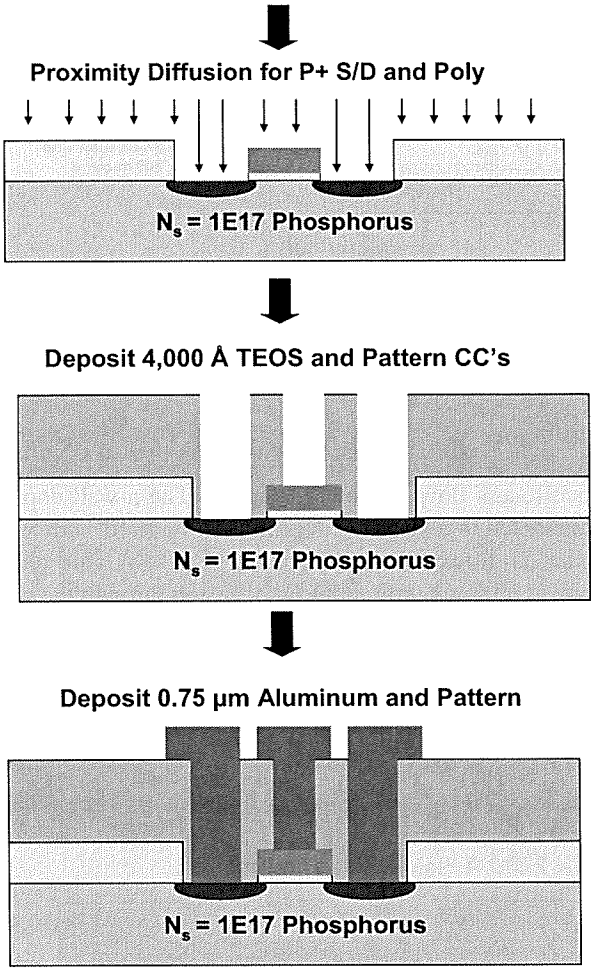


Fig. 5 Illustration of the PMOS transistor fabrication process.

One major processing issue was encountered. After performing the proximity diffusion process, 4,000 Å of TEOS was deposited to serve as an ILD. The contact cuts were wet etched in buffered oxide etch with surfactants. The photoresist was removed and an RCA clean process was performed prior to Aluminum deposition. During the RCA clean, significant amounts of TEOS was removed. After the subsequent aluminum deposition, some peeling of the metal occurred. The most likely explanation is the proximity diffusion process left a very thin layer of Borosilicates causing the adhesion problems for the TEOS and peeling under stress. The metal adhesion problem was due to the underlying TEOS. The proposed solution is to perform an RCA clean immediately after the proximity diffusion process.

IV. Results

The devices were tested and working transistors were found down to 0.6 micron mask defined gate lengths. Since the processing was done using g-line lithography the resolution of small gate lengths is limited.

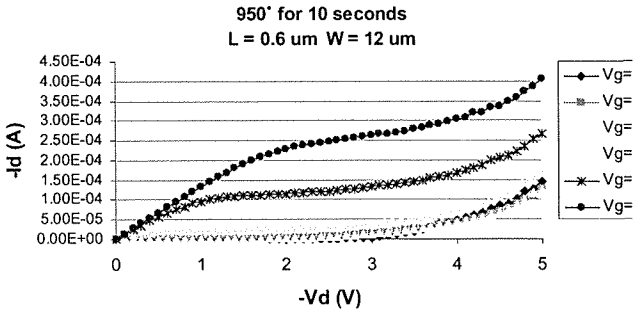


Fig. 6 Id vs. Vd Family of curves for different gate voltages, 0.6 micron device with a 10 second diffusion at 950 degrees.

The threshold voltage for these devices was found to be -3.1 Volts. A threshold voltage adjustment implant could be performed in the future if needed. It was also determined that the drain/source junction breakdown voltage matched the theoretically expected values for ultra-shallow junctions with a small radius of curvature.

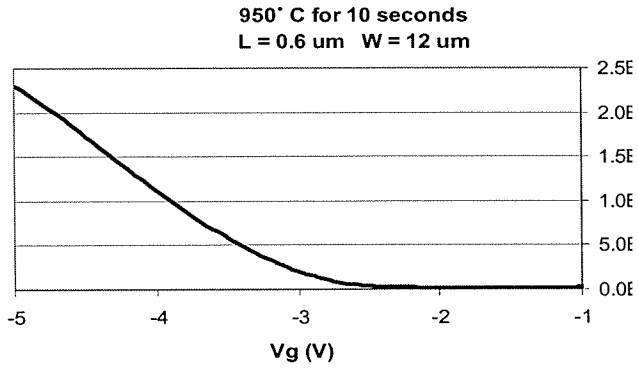


Fig. 7 Id vs. Vg characteristics for a 0.6 micron gate length PMOS transistor. The threshold voltage is extracted and found to be -3.1 Volts.

The SIMS analysis in Fig. 8 shows a very high surface concentration with a junction depth of 30 to 40 Å. The measurement had a higher than normal concentration threshold.

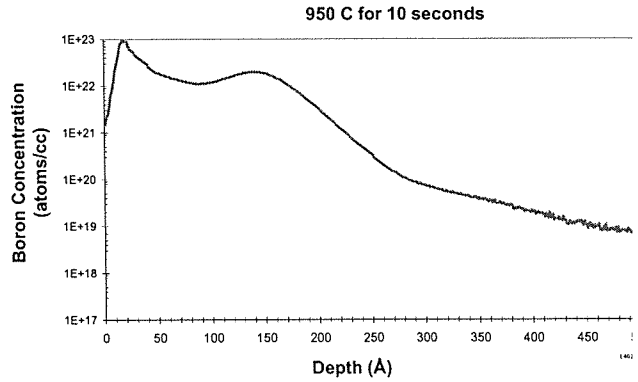


Fig. 8 SIMS analysis results showing the boron dopant profile.

V. Conclusions

This was the first attempt at proximity rapid thermal diffusion for patterned wafers here at RIT. The process produced good working sub-micron PMOS devices down to 0.6 microns. This work provides a base for further research work on scaled devices.

Acknowledgments

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References

[1] J. R. Brews, W. Fichtner, E.H. Nicollian, and S.M. Sze, "Generalized Guide for MOSFET Miniaturization," *IEEE Electron Dev. Letters*, vol. EDL-1, No. 1, Jan. 1980, pp. 2-4.

[2] D. P. Kennedy, and R. R. O'Brien, "Avalanche Breakdown Calculations for a Planar p-n Junction," *IBM Journal*, May 1966, pp. 213-219.

[3] W. Zagozdzon-Wosik, P.B.Brabiec, and G.Lux, "Fabrication of Submicron Junctions-Proximity Rapid Thermal Diffusion of Phosphorus, Boron, and Arsenic," *IEEE Trans. On Electron Dev.*, vol. 41, No. 12, Dec. 1994, pp. 2281-2290.

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