Junction Integrity for Low Temperature Dopant Activation in Silicon

Geoff E. Watson

Abstract—**Detailed within this paper is investigation of using low temperature processes to activate dopant in silicon. Parameters studied include breakdown voltage, turn-on voltage, leakage current, and ideality factor. Strong correlation was seen between the temperature of activation and both the ideality factor and leakage current. Breakdown voltage seemed constant except for the highest temperature processing. Turn-on voltage seemed to change for boron activation, but not for phosphorus activation**

Index Terms—**Doping, electrical activation, semiconductor process modeling, low temperature processing.**

I. Introduction

Intrinsic silicon as a semiconductor lacks the conductivity to allow for circuits to operate. This is corrected by the addition of dopants that increase the conductivity. Dopants are divided into two subgroups: p-type and n-type. The n-type dopants, such as Phosphorus or Arsenic, when electrically activated in the silicon provide extra electrons which allow the silicon to conduct electricity. The p-type dopants, such as Boron or Gallium, remove electrons when activated and the resulting "hole" allows the conduction of electricity as well.

However, in order for the dopants to become electrically activated, the silicon must undergo a thermal process. In the case of thin film transistors where silicon is found connected to an insulating glass, there are material constraints that must be considered. For example, Corning Incorporated produces a glass that has many desirable characteristics for thin film transistors. The negative qualities of this glass, however, include its low temperature strain point of approximately 660°C. While this is seemingly a high temperature, a comparison with the activation processing temperatures around 900°C to 1100°C shows that the glass would be raised far above its strain point causing irreparable damage to the glass.

Having devised a method of activating the dopant at a temperature of 600°C, there are still concerns as to how this affects the electrical devices. This study attempted to characterize the effects of lowering the temperature for dopant activation as it relates to several different characteristics found in diodes.

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II. Theory

A. Low Temperature Activation

In order for the dopant atom to become electrically activated, it must be substituted in to the silicon lattice in place of a silicon atom. Normal anneal processes do this by increasing the temperature of the activation step. The use of the higher temperatures in the case of the specified Corning Inc. glass is impossible as it would damage the glass by raising the temperature over the strain point.

An alternative to raising the temperature of the process requires a look into why the elevated temperature was thought necessary. In modern processing, silicon atoms must be substituted for dopant atoms. This substitution requires energy. One way to provide this energy is by elevating the temperature. This temperature increase provides energy for the silicon to leave the lattice site wherein the dopant atom is placed. The temperature increase, therefore, is only required to remove the silicon atom from the lattice site and place the dopant atom in that same site.

The alternative processing is to destroy the silicon lattice before attempting the activation. This amorphization of the lattice allows the temperature increase to be used to rebuild the lattice using whatever atoms are nearby. After ion implanting the dose of dopant atoms, the concentration allows the energy from the temperature to activate the dopant atoms while simply rebuilding the lattice. The temperature required for this is much lower than the standard processing requiring only 600°C to activate the dopant.

B. Amorphizing the Lattice

As it happens, the implanting of dopant atoms creates an amount of implant damage which is amorphization of the silicon. For phosphorus implantation, the atoms being implanted have enough mass to create a large amount of amorphization. They are said to self-amorphize the lattice.

However, boron atoms, because of their small mass, when implanted create very little damage to the lattice. For this reason, another element must be used to create the damage desired. For ease, fluorine is used to do this damage. This is convenient because fluorine is another species of element located in the source for the boron dopant. Boron trifluoride, BF_3, is the gas used by the ion implanter to provide the boron. Simply turning a dial allows the implantation of the

fluorine as well. The fluorine has more mass which provides greater implant damage. Lastly, the fluorine does not affect the electrical properties of the implanted silicon making it an ideal choice.

III. Experimental Procedure

A. Diode Creation

To begin this processing, both p-type and n-type wafers were acquired. The resistivity of the p-type wafers was 15 to 25 Ω-cm and the resistivity of the n-type wafers was 10 to 25 Ω-cm. The wafers began with an RCA clean using the standard RIT RCA clean process. A pad oxide was then grown on the wafers in the Bruce furnace. The recipe used was Furnace Recipe 250 which targeted 500Å. Following this, well implants were performed on the Varian 350D Ion Implanter. For the n-type wafers, phosphorus was implanted at a dose of $5.5x10^{12}$ cm^{-2} at an energy of 100 keV. For the p-type wafers, boron was implanted at a dose of $6.0x10^{12}$ cm^{-2} at an energy of 55 keV. A diffusion step was performed for the well drive and a field oxide was grown using Furnace Recipe 112. The field oxide target was 5000 Å.

Level 1 lithography was then performed. Two die on each wafer were shot with the NWELL RIT BJT mask to set alignment marks. The rest of the die were shot with the BASE RIT BJT mask. Defaults were used for all of the exposure parameters. To remove the oxide from the patterned areas, a 12 minute etch was performed in 10:1 buffered oxide etch. This was followed by a deionized water rinse for 5 minutes. The resist was stripped using a solvent strip and an RCA clean was performed to remove any residual organics. Furnace Recipe 311 was then used to grow 1000 Å of oxide to be used as an implant mask.

The backside of the wafers were implanted to improve the contact between the aluminum. N-type wafers were implanted with phosphorus at a dose of $1x10^{15}$ cm^{-2} with an energy of 92 keV. P-type wafers were implanted with boron at a dose of $4x10^{15}$ with an energy of 34 keV. Furnace Recipe 272 was used to anneal the backside implants. The frontside of the wafers were then implanted to create the active area. For the n-type wafers, fluorine was first implanted at a dose of $3x10^{15}$ cm^{-2} with an energy of 75 keV to amorphize the surface. Boron was then implanted at a dose of $4x10^{15}$ cm^{-2}. For the p-type wafers, phosphorus was implanted at a dose of $4x10^{15}$ with an energy of 92 keV.

The experimental split was performed at the frontside anneal. The processing conditions can be found in Figure 1. The recipes used were Furnace Recipes 273 through 279. Contact cut lithography was then performed using the CONTACT CUT RIT BJT mask and all the default parameters for exposure. The contact cut etch was performed in the same 10:1 buffered oxide etch for 2.25 minutes. A 5 minute deionized water rinse followed. The resist was stripped with a solvent strip chemistry again. An RCA clean was then performed to remove residual organics followed by a 30 second HF dip in 50:1 HF acid to remove any native oxide.

N-type Wafers	P-type Wafers
600C 1 hr	600oC 1 hr
600oC 2 hr	600oC 2 hr
700oC 1 hr	700oC 1 hr
800oC 1 hr	800oC 1 hr
900oC 1 hr	900oC 1 hr
1000oC 30 min	1000oC 30 min
1100oC 10 min	1100oC 10 min

Figure 1: Treatment Combinations

Aluminum was evaporated on the frontside of the wafers at a target thickness of 7500 Å. Base pressure for the evaporation was 4 with an energy of 92 keV.

The experimental split was performed at the frontside anneal. The processing conditions can be found in Figure 1. The recipes used were Furnace Recipes 273 through 279. Contact cut lithography was then performed using the CONTACT CUT RIT BJT mask and all the default parameters for exposure. The contact cut etch was performed in the same 10:1 buffered oxide etch for 2.25 minutes. A 5 minute deionized water rinse followed. The resist was stripped with a solvent strip chemistry again. An RCA clean was then performed to remove residual organics followed by a 30 second HF dip in 50:1 HF acid to remove any native oxide.

Aluminum was evaporated on the frontside of the wafers at a target thickness of 7500 Å. Base pressure for the evaporation was $4.6x10^{-6}$ Torr. The metal was patterned using the METAL RIT BJT mask and all the default parameters for the exposure. The metal etch was performed in the wet aluminum etch chemistry using a visual endpoint detection. The etch was completed in 2 minutes. Wafers were rinsed and then inspected to ensure that the metal was completely etched. The wafers were solvent stripped and dipped in a pad etch to remove any native oxide. The pad etch dip was 10 seconds. Aluminum was then evaporated on the backside of the wafers. A sinter step was performed in the Bruce Furnace using Furnace Recipe 41. The finished diodes were taken to the test lab for analyzation.

B. Electrical Testing

Ten sites were selected on each wafer. Each site was tested with a forward bias and a reverse bias. For the n-type wafers, the forward bias was from -1 V to 2 V using 101 steps. The reverse bias for these wafers was from -30 V to 1 V using 101 steps. For the p-type wafers, the forward bias was from -2 V to 1 V using 101 steps. The reverse bias for these wafers was -1 V to 40 V using 101 steps. Current and voltage were measured and plotted. The desired parameters were extracted.

IV. Results and Analysis

A. Die-to-die Repeatability

Die to die repeatability for the n-type wafers (with activated boron) was quite impressive. Figure 2 shows a sample reverse bias curve from the n-type wafers. The chart shows very little variation from die to die. It is the same case with all of the data from the n-type wafers. The rest of these curves can be found in the appendix.

The p-type wafers (with activated phosphorus), on the other hand, showed quite a large variation from die to die. This dissimilarity can be seen in Figure 3. The leakage current in the reverse bias for the sample curve spans over orders of magnitude difference. However, the data was consistently poor for the p-type wafers regardless of activation temperature. Again, the remainder of the curves can be found in the appendix.

B. Treatment Combination Comparisons

For the comparison between the treatment combinations, the data was simply plotted on the same charts. For the n-type wafers, any of the die could have been selected because of the small variation among them. For each wafer, regardless of type, one curve was just selected showing the most desirable characteristics. For example, the curve was selected that had the lowest leakage current or the best reverse breakdown voltage. The charts can be found in the appendix.

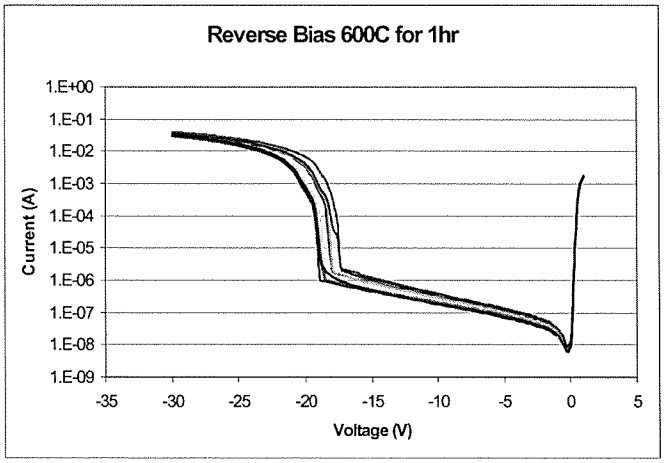


Figure 2: Reverse Bias for n-type Wafers

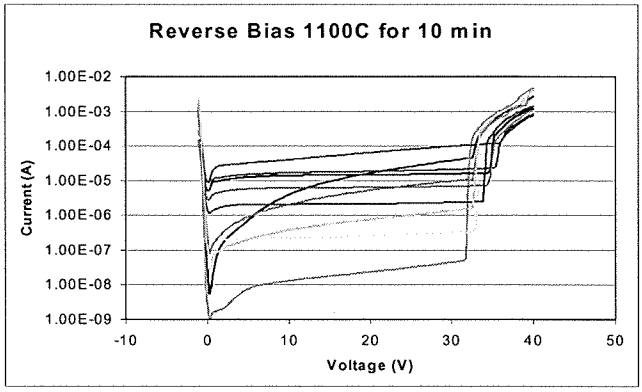


Figure 3: Reverse Bias for p-type Wafers Bias

As the devices would be operating at voltages of approximately 10 V, the leakage current extracted was done so at a reverse bias of 10 V for the p-type wafers, and -10 V for the n-type wafers. The summary tables in Figure 4 and Figure 5 show that leakage current generally worsens as the anneal temperature decreases, but the anneal time at 600°C had little impact on the leakage current.

The ideality factor showed the strongest correlation to the anneal conditions. The factor approached 1 in both wafer types. Ranging in values from 1 to 2, the ideality for low temperature anneals was closer to 2 and decreased as the temperature increased. This was expected as lowering the anneal temperature was expected to have a negative effect on the junction integrity and therefore on the ideality.

Breakdown voltages for the n-type wafers appeared to be approximately the same except for the 1100°C anneal which far exceeded the others. For the p-type wafers, the noise in the data was so great that the breakdown voltage listed is not that reliable. The turn-on voltage showed very little wafer-to-wafer variation regardless of wafer type.

n-type	Leakage current at 10V Reverse Bias	Turn-on Voltage	Breakdown Voltage	Ideality Factor
600°C 1hr	18.4 nA	0.78 V	-18.2 V	1.56
600°C 2hr	81.6 nA	0.84 V	-18.8 V	1.36
700°C 1hr	491 pA	1.05 V	-18.8 V	1.05
800°C 1hr	700 pA	1.03 V	-19.2 V	1.05
900°C 1hr	465 pA	1.01 V	-18.5 V	1.03
1000°C 30min	409 pA	1.04 V	-19.8 V	1.05
1100°C 10min	115 pA	1.05 V	-24.4 V	1.02

Figure 4: n-type Wafer Summary Data

p-type wafer	Leakage current at 10V Reverse Bias	Turn-on Voltage	Breakdown Voltage	Ideality Factor
600°C 1hr	23.5 μA	-0.85 V	27.7 V	1.78
600°C 2hr	67.3 μA	-0.80 V	31.4 V	1.54
700°C 1hr	1.89 μA	-0.80 V	29.3 V	1.38
800°C 1hr	55.7 nA	-0.85 V	28.1 V	1.25
900°C 1hr	161 nA	-1.20 V	28.1 V	1.33
1000°C 30min	14.1 nA	-0.75 V	29.3 V	1.34
1100°C 10min	219 nA	-0.85 V	32.6 V	1.03

Figure 5: p-type Wafer Summary Data

V. Conclusion

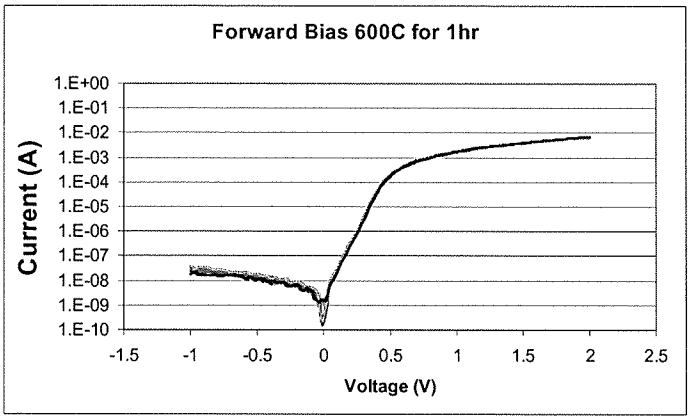
Leakage current and ideality factors are definitely negatively affected by using low temperature for the anneal step. However, the data shows that the "on" state still produces a higher current than the reverse bias "off" state. The diodes should therefore still be usable if the leakage current can be ignored.

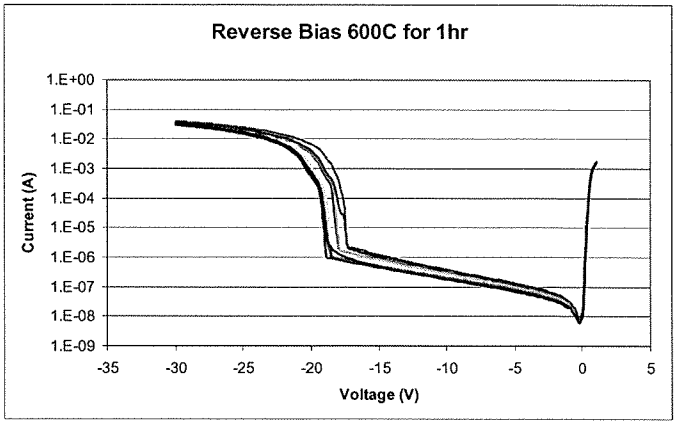
VI. Acknowledgment

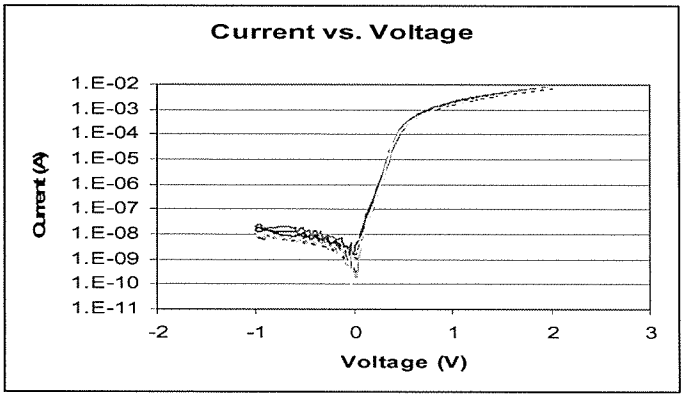
The author would like to acknowledge Dr. Hirschman for his assistance in choosing this topic.

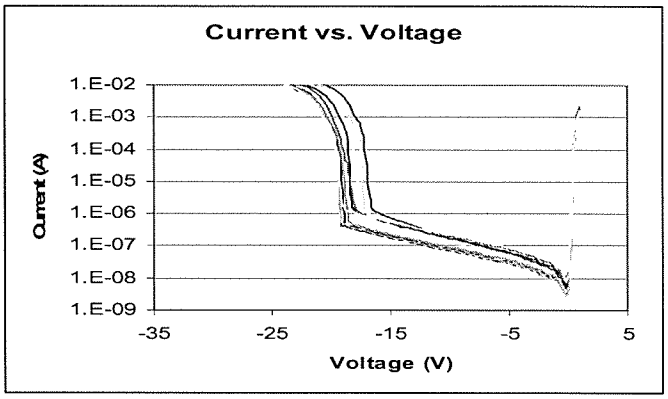
VII. Appendix

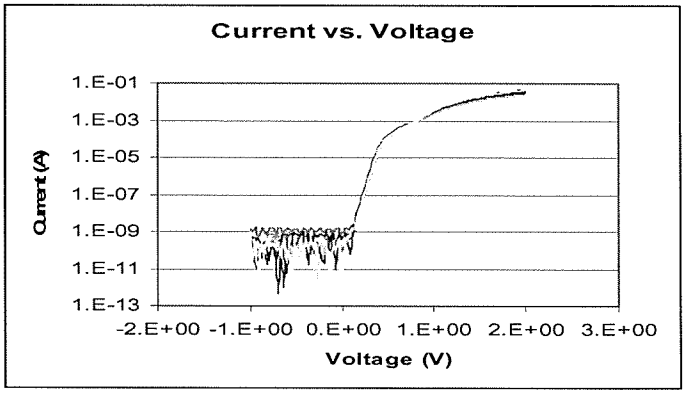
n-type wafers

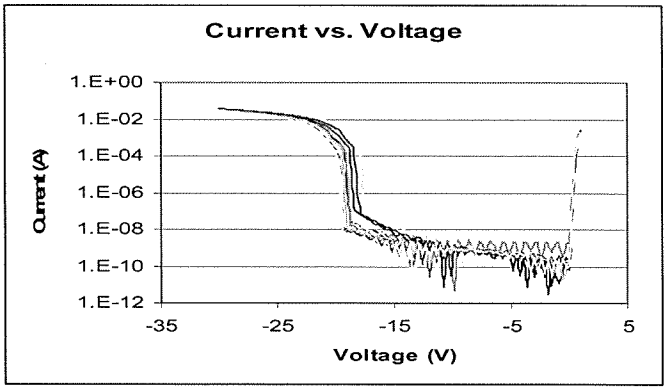


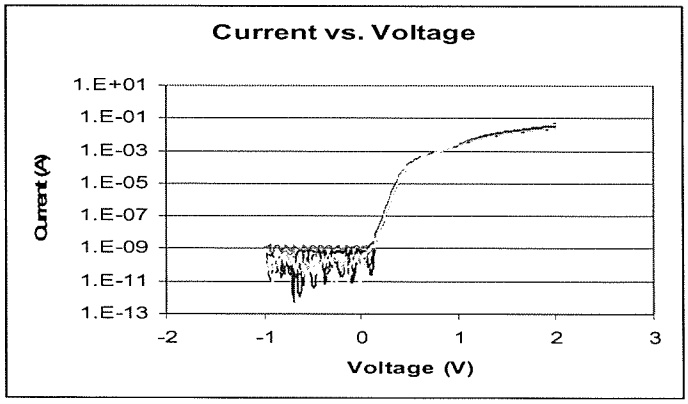


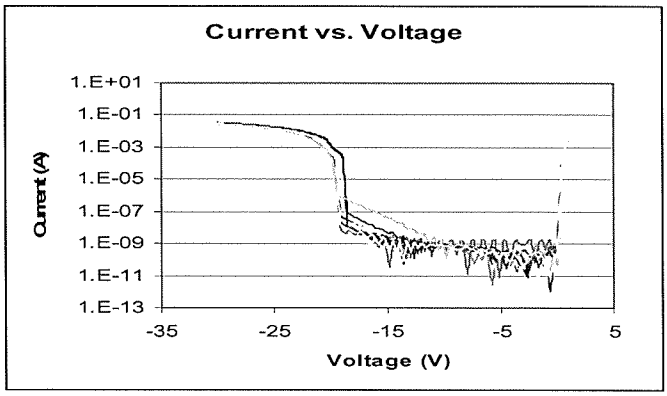


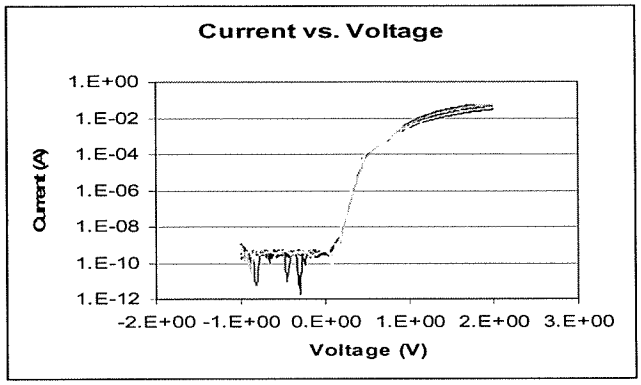








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1.E-02
1.E-04
1.E-06
1.E-08
1.E-10
1.E-12
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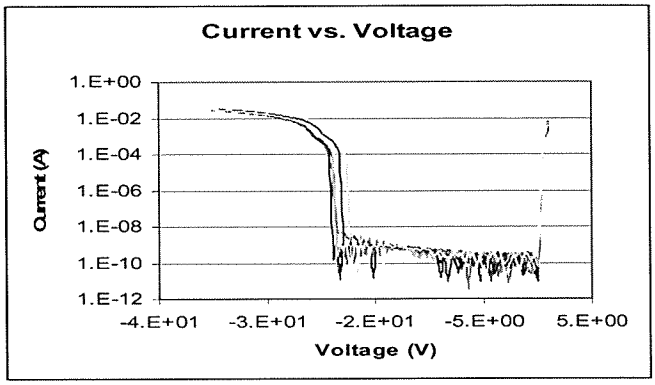
Voltage (V)


Current vs. Voltage
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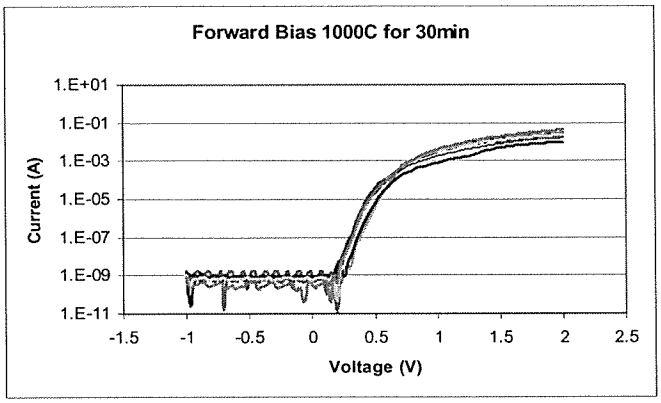
Voltage (V)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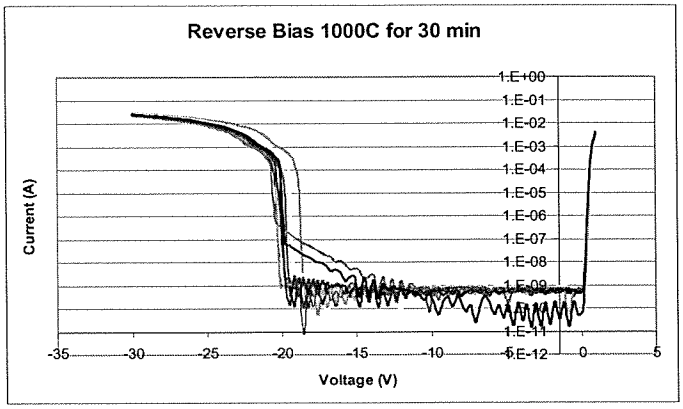
Voltage (V)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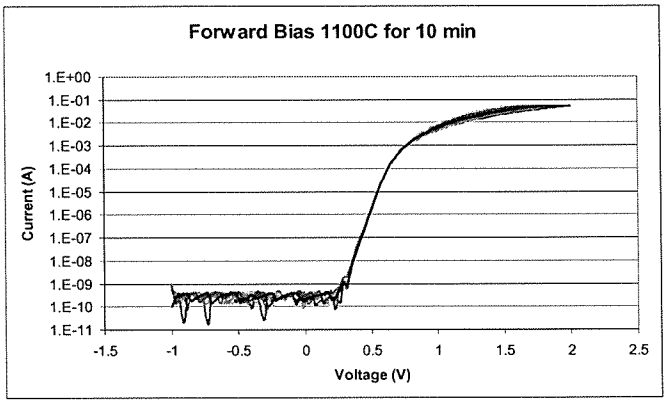
Voltage (V)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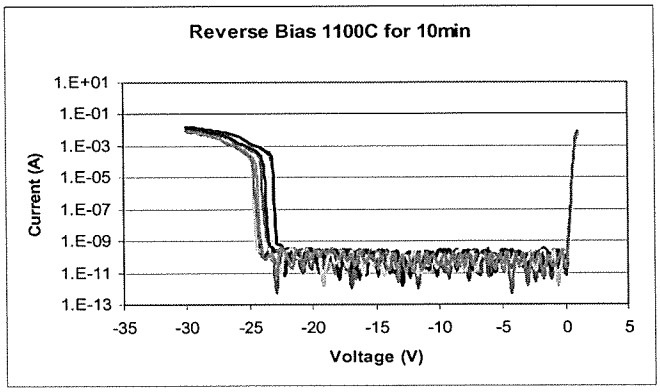
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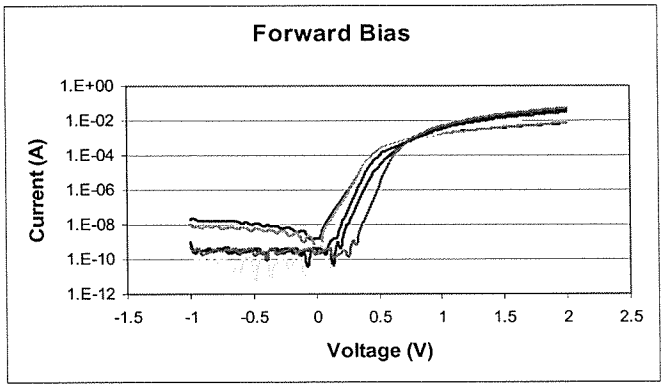
Voltage (V)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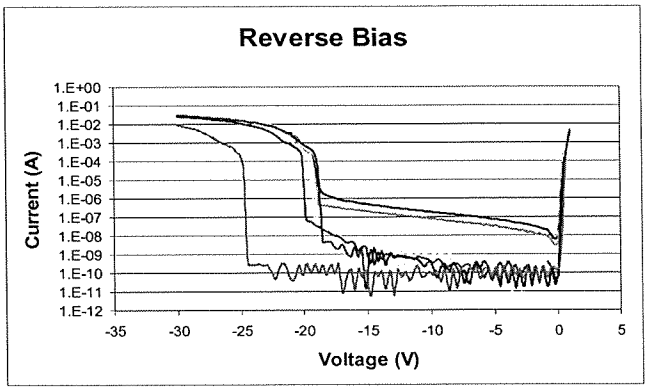
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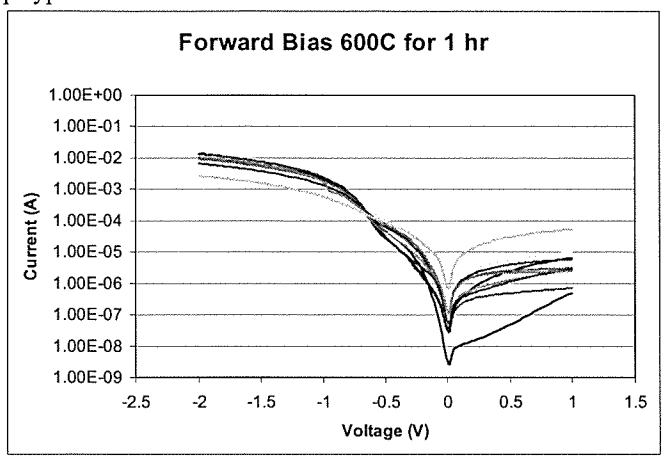
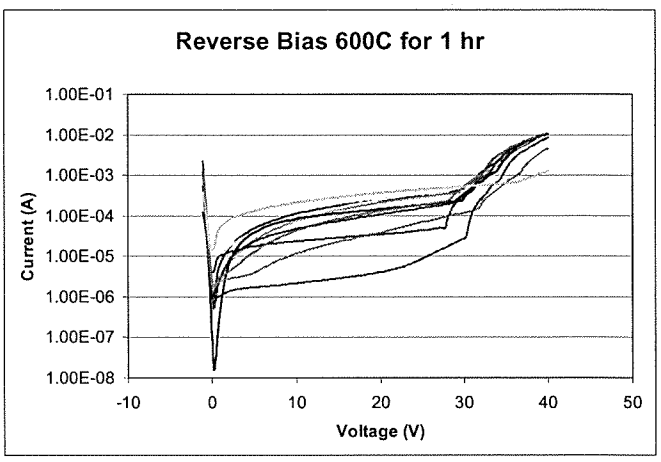
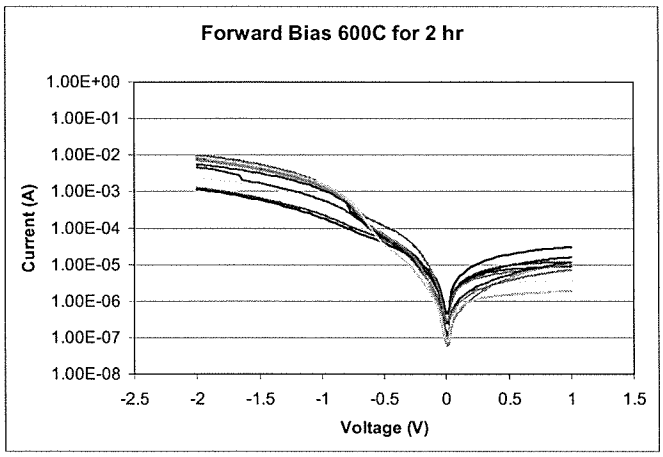
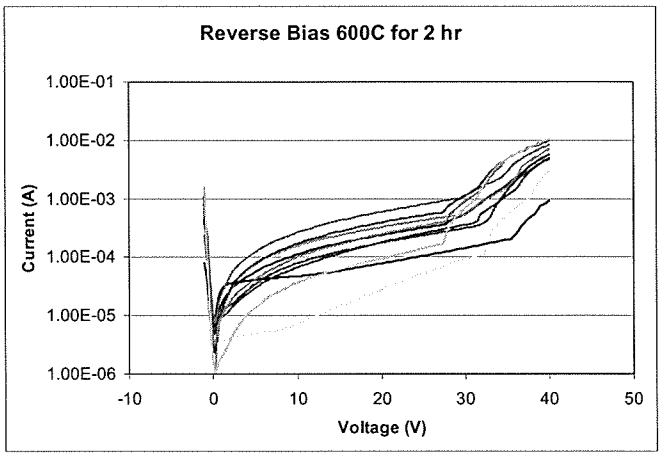
Voltage (V)

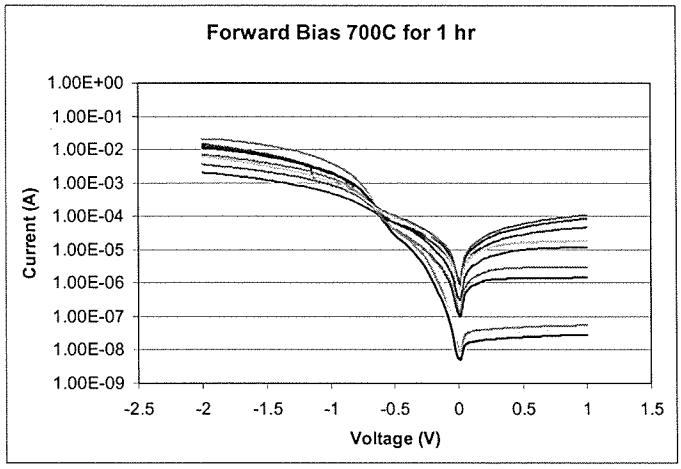
p-type wafers

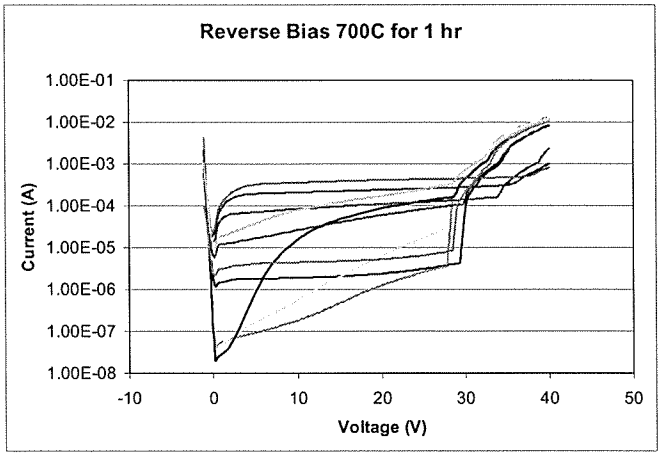


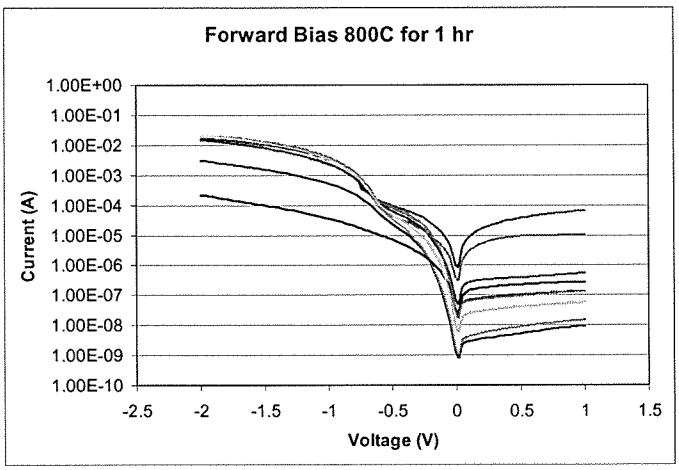








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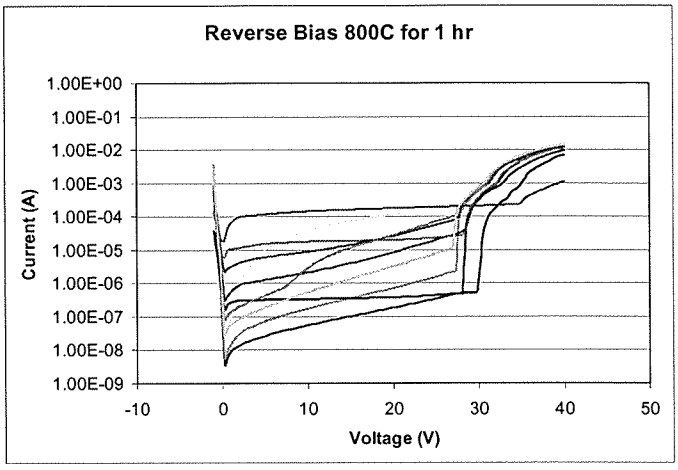
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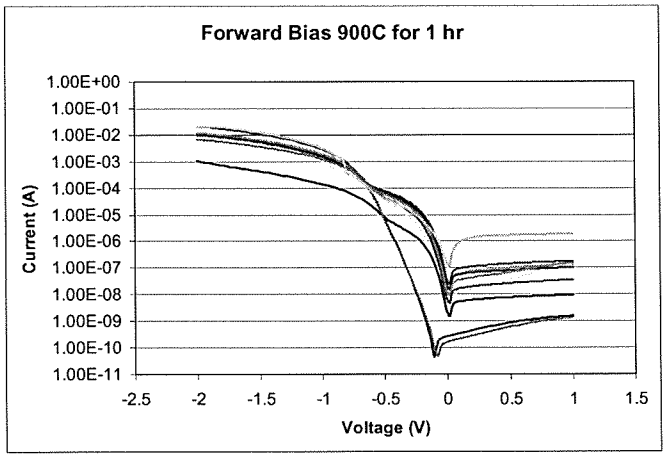
Voltage (V)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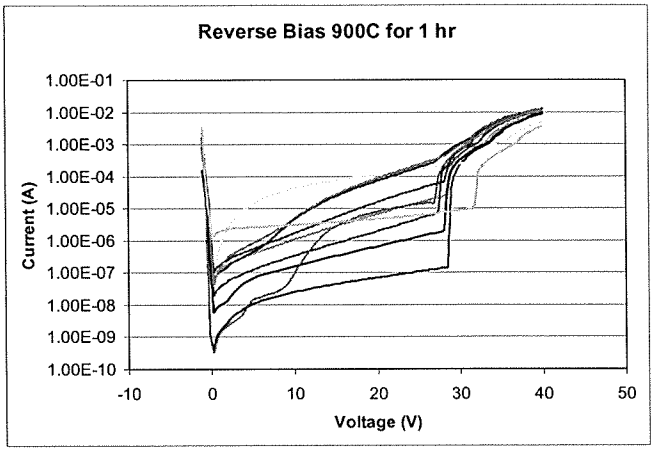
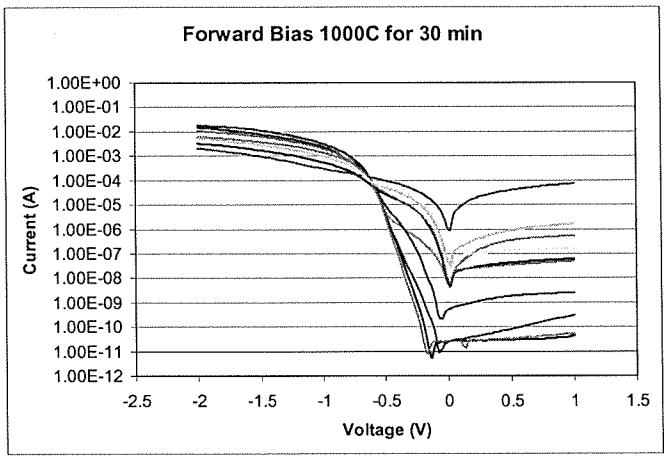
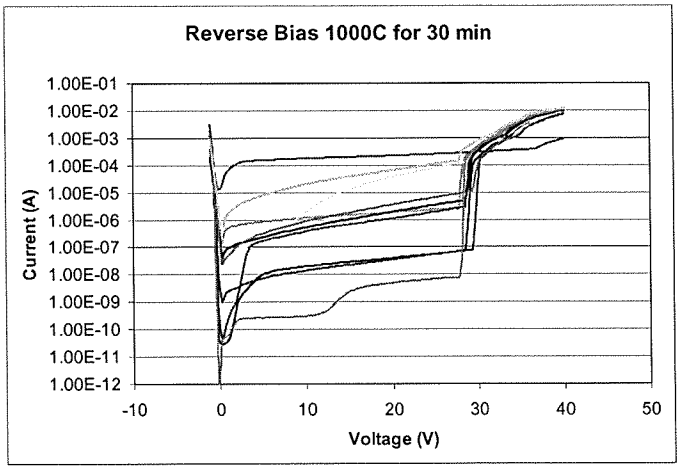
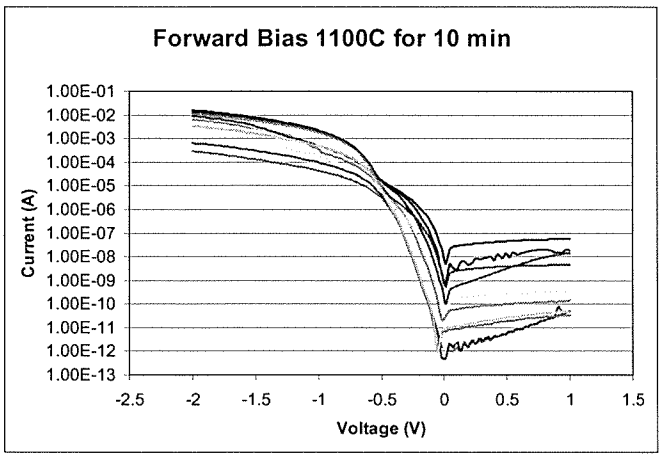
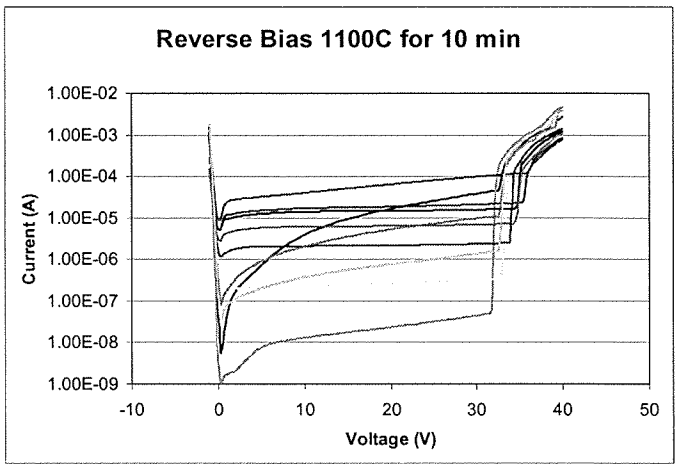
1.00E-01
1.00E-02
1.00E-03
1.00E-04
1.00E-05
1.00E-06
1.00E-07
1.00E-08
1.00E-09
1.00E-10
1.00E-11
-2.5 -2 -1.5 -1 -0.5 0 0.5 1 1.5
Voltage (V)

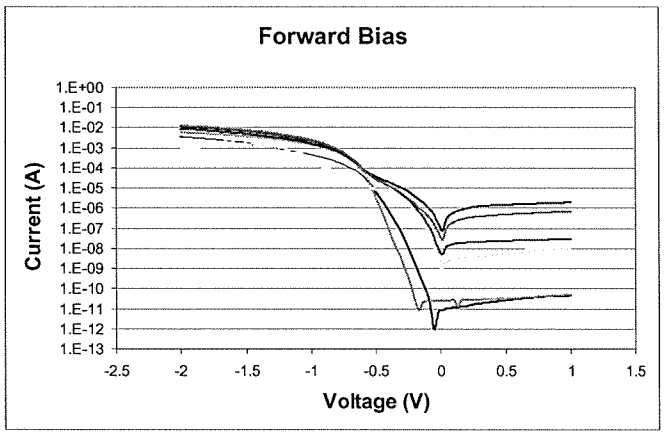

Reverse Bias 900C for 1 hr
Current (A)
1.00E-01
1.00E-02
1.00E-03
1.00E-04
1.00E-05
1.00E-06
1.00E-07
1.00E-08
1.00E-09
1.00E-10
-10 0 10 20 30 40 50
Voltage (V)

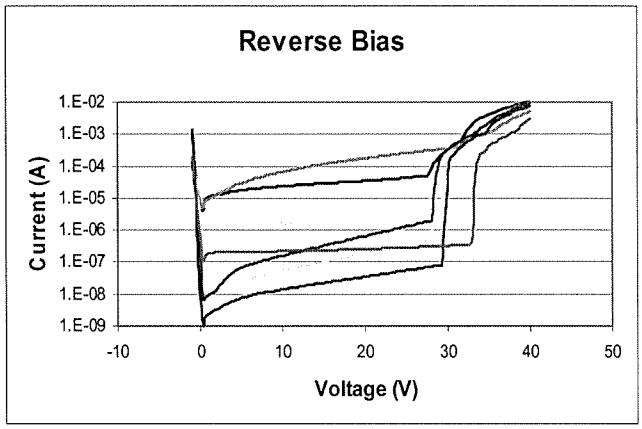

Forward Bias 1000C for 30 min
Current (A)
1.00E+00
1.00E-01
1.00E-02
1.00E-03
1.00E-04
1.00E-05
1.00E-06
1.00E-07
1.00E-08
1.00E-09
1.00E-10
1.00E-11
1.00E-12
-2.5 -2 -1.5 -1 -0.5 0 0.5 1 1.5
Voltage (V)


Reverse Bias 1000C for 30 min
Current (A)
1.00E-01
1.00E-02
1.00E-03
1.00E-04
1.00E-05
1.00E-06
1.00E-07
1.00E-08
1.00E-09
1.00E-10
1.00E-11
1.00E-12
-10 0 10 20 30 40 50
Voltage (V)


Forward Bias 1100C for 10 min
Current (A)
1.00E-01
1.00E-02
1.00E-03
1.00E-04
1.00E-05
1.00E-06
1.00E-07
1.00E-08
1.00E-09
1.00E-10
1.00E-11
1.00E-12
1.00E-13
-2.5 -2 -1.5 -1 -0.5 0 0.5 1 1.5
Voltage (V)


Reverse Bias 1100C for 10 min
Current (A)
1.00E-02
1.00E-03
1.00E-04
1.00E-05
1.00E-06
1.00E-07
1.00E-08
1.00E-09
-10 0 10 20 30 40 50
Voltage (V)


Forward Bias
Current (A)
1.E+00
1.E-01
1.E-02
1.E-03
1.E-04
1.E-05
1.E-06
1.E-07
1.E-08
1.E-09
1.E-10
1.E-11
1.E-12
1.E-13
-2.5 -2 -1.5 -1 -0.5 0 0.5 1 1.5
Voltage (V)


Reverse Bias
Current (A)
1.E-02
1.E-03
1.E-04
1.E-05
1.E-06
1.E-07
1.E-08
1.E-09
-10 0 10 20 30 40 50
Voltage (V)