

Development of a Bilayer Metallization for RIT's Existing CMOS Process

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Abstract — The design and fabrication of a two-level subtractive aluminum metal backend was completed at the Rochester Institute of Technology. Metal1-Metal2 (M1-M2) via chains were used as electrical test structures and tested operational. The optimal process uses 4000Å of LTO for an ILD, a non-heated metal2 aluminum sputter deposition, and a chlorine-based plasma for metal etch. Resistance measurements taken through via chains produced values of ~400Ω. While an ideal aluminum bar of the via chain's dimensions should have a resistance of ~100Ω, a contact resistance exists at each via throughout the chain and increases the resistance value. Capacitors were also electrically tested to determine ILD effectiveness. A 200μm x 200μm M1-ILD-M2 capacitor has a theoretical value of 3.5pF and the measured structures ranged from 3.01pF to 3.45pF. In addition to demonstrating that the first and second level metal lines could make electrical contact through via openings, testing was done to ensure electrical separation existed when needed. Metal2 lines overlapping metal1 lines were tested and measured to be electrically isolated, shown in Figures 4-6. This process has created a bilayer metallization design that allows for multilevel aluminum connections and electrical isolation where needed and can be readily implemented in RIT's present CMOS.

I. INTRODUCTION

The goal of this project was to create a bilayer aluminum that would make connections from layer to layer through vias and exhibit electrical separation when overlapping. As integrated circuit technology becomes more advanced and device sizes continue to be reduced, increased pressure is being placed on backend utilization. Metal lines serve as intermediaries to connect the underlying devices to the chip's bondpads to supply power and grounding. The use of more devices in less area requires more than a single layer of metal lines. Some of the most advanced chips have five or more metal levels to support the massive routing of current, as seen in Figure 1 [1]. The increase in the number of metal lines reduces the current load applied to each level, as well as creates more direct paths to individual structures. The goal of this project was to design and implement a reliable multilayer aluminum backend for RIT's existing CMOS process. This will allow for fabrication of more sophisticated semiconductor devices that require large amounts of power and increase the scale of connectivity in existing devices.

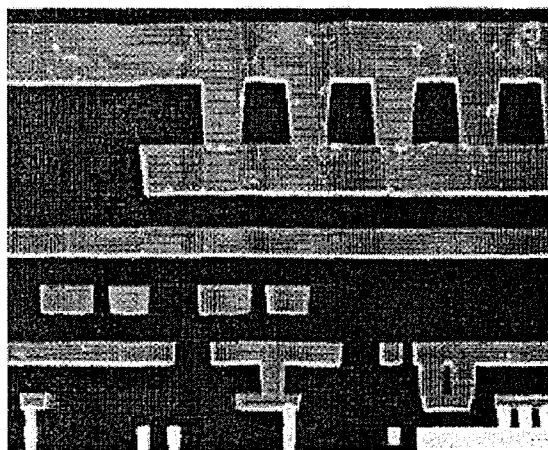


Fig. 1: SEM Cross-Section of IBM's Multilayer Metallization [1]

II. PROCESS FLOW and EXPERIMENT

The process flow used for this experiment was adapted from RIT's existing SMFL-CMOS process used in the student-run factory course. Because the goal was develop the bilayer metal for the back end, all of the steps, except one, from the front end were not needed and were not included in the processing for this project. The process step used from the front end was the n-well oxide. Eighteen total process steps are required to fabricate the two level metal structures.

First, eight bare, six-inch silicon wafers were obtained and cleaned using a wet RCA cleaning. The first step in this clean is a heated ammonium hydroxide and hydrogen peroxide mixture. The NH_4OH is a strong base and is used to remove organics from the wafers' surfaces and the H_2O_2 creates a silicon dioxide at the wafers' surfaces to keep the silicon from etching. The next step in the clean is a 10:1 hydrofluoric (HF) acid dip to remove this silicon dioxide layer. The last bath consists of hydrochloric acid and hydrogen peroxide. The HCl is a strong acid that removes metal and the H_2O_2 oxidizes the wafers' surfaces. The wafers are rinsed and dried before the thermal oxide growth.

Using a wet oxide in a Bruce thermal tube, the wafers have a thermal oxide layer grown on them

during a five hour soak in O₂ at 950°C. A 15 minute ramp up time and 30 minute ramp down time are required to heat the thermal tubes to correct temperatures and a thickness of 6500Å is targeted. Lithography is done on all wafers using a Canon FPA-2000i1 stepper, which utilizes a 365nm source wavelength, a numerical aperture of 0.52, and a degree of coherency of 0.6. The wafers are coated with 1µm of OiR620 photoresist (PR) on a SSI coating track and exposed using the "SMFL-CMOS n-well" mask. A dose of 60mJ/cm² and a focus of +0.25µm was used. They were developed on the SSI track using a TMAH developer and a post-exposure bake temperature of 120°C.

Using a 10:1 buffered oxide etch (BOE) of hydrofluoric acid, the exposed thermal oxide was etched for 15 minutes. With an established etch rate of 560 Å/minute, the oxide would need about 14 minutes to clear, but an overetch is introduced to ensure clearing non-uniform areas. The wafers have the photoresist etch mask removed using a Branson asher, which utilizes a downstream oxide-based plasma etch chemistry to remove organics. They are again RCA cleaned to remove debris and contamination from the surface before metal deposition.

The wafers are given a quick HF dip before being placed into a CVC-601 metal sputter system. This removes any native oxide that would have grown on the wafers surface from atmospheric oxygen and promotes a better adhesion between the sputtered metal and the silicon. At a base pressure of ~5.0E-6 torr, the wafers are sputtered using an 99% aluminum (Al) and 1% silicon (Si) target. The incorporation of silicon into the metal reduces the occurrence of aluminum spiking into the silicon. Argon is used as the ambient gas and a thickness of 7500Å is targeted.

All the wafers are then coated on the SSI track with a thicker layer of PR, 1.5µm for metal lithography. This helps to make it more resistive to the harsher metal etches. A focus-exposure matrix (FEM) is run at this step to establish the best lithographic conditions for the metal using the "SMFL-CMOS metal1" mask. Using 60mJ/cm² as a first dose value with a 12mJ/cm² increment and -1.0µm as a first focus value with a 0.2µm increment, the matrix is run over the 12x12 die array. The best combination is found to be 180mJ/cm² for exposure and +1.25µm for focus. All the wafers are exposed at these conditions and developed on the track using a 140°C post exposure bake to ensure proper cross-linking of the thicker resist.

The first layer of aluminum (M1) was etched using a Transene aluminum wet etch chemistry heated to 50°C. This consists of 20 parts

phosphoric acid, one part acidic acid, one part nitric acid, and one part water. One wafer was dipped in the bath in increments to establish an approximate etch rate and the remaining wafers were etched for a total of 3 minutes and 30 seconds. The time used was enough to clear the aluminum in all exposed regions, but caused some undercutting some isolated features. The photoresist was then removed using the Branson asher for a longer time because of the thicker resist. The following step was the first in which two different materials were used to find the best fit. After the M1 had been deposited and patterned, an interlayer dielectric (ILD) was needed to electrically separate the two levels of metal. Half of the wafers were deposited with a low temperature oxide (LTO) and the other half of the wafers were deposited with tetramethyl orthosilicate (TEOS). Both are oxides that have an electrical permittivity close to silicon dioxide and both films are deposited with chemical vapor deposition (CVD). The LTO is deposited in a low pressure chamber (LPCVD) and the TEOS is deposited in an Applied Materials P5000. Monitor wafers are included with each process to determine average film thicknesses.

Next, the wafers were coated with 1µm of PR and exposed using the Canon stepper and the "SMFL-CMOS via" mask. Again, an FEM was run on one wafer and the best dose was 260mJ/cm² and the best focus was +0.25µm. After development, the oxide ILD was etched using a Pad etch for the LTO and a 10:1 BOE for the TEOS. Etch rates for each material was established on a single wafer and the remaining wafers were etched accordingly with a 10% overetch. After the oxide was removed in the vias, the wafers had the photoresist removed.

At the second metal (M2) sputter, another split occurred. An attempt was made to sputter some of the wafers with aluminum while having the system's heater on. This heats the chamber to 300°C and adds enough energy to the incoming atoms to allow them to migrate on the wafer surface before finding a place to stop. Using a normal sputter, the atoms stick at the spot where they first encounter the wafer. By heating the system, it was theorized that the metal would be more conformal over step heights. Half the wafers were deposited with a normal sputter and half with a heated sputter. The metal used for M2 was 1000Å of titanium and 7500Å of aluminum. The thinner initial titanium layer acts as an adhesive between the two aluminum levels to keep them together. The Ti was sputtered at 750 watts of power and the aluminum was sputtered at the same 2000 watts as M1.

The wafers were then coated with the thicker 1.5µm of photoresist and exposed after an FEM found 160mJ/cm² and +0.5µm to be the best

combination of dose and focus. They were developed using the longer post-exposure bake time and moved to the last processing split. At M2 etch, both wet and dry etches were attempted on separate wafers to find the most anisotropic removal of aluminum possible. The wafers that were wet etched were done so in the same Transene chemistry as used for all wafers at M1 etch. The remaining wafers were dry etched using chlorine-based plasma etch in a LAM 4600 to remove the aluminum and a fluorine-based chemistry in a Drytek Quad to remove the titanium. The aluminum etch occurs at a pressure of 300mT and an electrode power of 275 watts with 60 sccm of Cl₂, 50 sccm of BCl₃, and 40 sccm of SF₆. A total of 150 seconds was needed of this etch to clear the wafer's aluminum. The titanium etch occurs at 150 mtorr and at an electrode power of 230 watts with 50 sccm of SF₆, 1 sccm of O₂, and 1 sccm of Ar. Only 60 seconds was needed to clear the Ti. After a final ashing to remove the photoresist used as the M2 etch stop, the wafers were tested and viewed in the scanning electron microscope (SEM).

Testing of the fabricated test structures was done using an HP 4145 station with a 12-pin probe system. The ICS software package collects the test data after all the pins and parameters have been setup. For capacitance testing, a C-V station was used with a heated chuck and software to acquire charge measurements. SEM work was completed on a Leo SEM.

III. RESULTS and DISCUSSION

The wafers were divided into five lots, shown in the lot matrix in Figure 2 below. Each lot was processed using the same conditions at every step except the critical steps listed.

Lot	Metal1 Etch	ILD	Metal2 dep.	Metal2 etch
A	Wet	LTO	Normal	Wet
B	Wet	LTO	Normal	Dry
C	Wet	LTO	Heated	Dry
D	Wet	TEOS	Normal	Dry
E	Wet	TEOS	Heated	Dry

Fig. 2: Project Lot Matrix

Three test structures were used during testing to gauge the electrical qualities of the bilayer metal: a 501 link via chain, M1-M2 capacitors, and M1-M2 overlays. The via chain, with links that were 6 μ m x 18 μ m, ensured that the metal could travel over the ILD step height and make electrical contact to the metal below through a 2 μ m x 2 μ m via opening. This structure can be seen in Figure 3. The second test

structure, a 200 μ m x 200 μ m capacitor, test the ILD's effectiveness in separating the metal as a dielectric, as seen in Figure 4. The last test structure, citured in Figure 5, is an SRAM cell. Since none of the front end processing had been done, the only components of the cell that were fabricated were the metall and metal2 lines. These overlapping lines were tested to ensure that the lines did not short when overlapping.

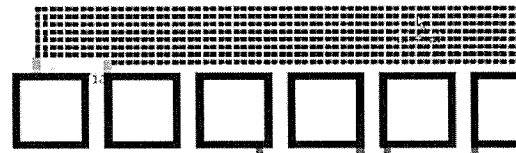


Fig. 3: M1-M2 Via Chain

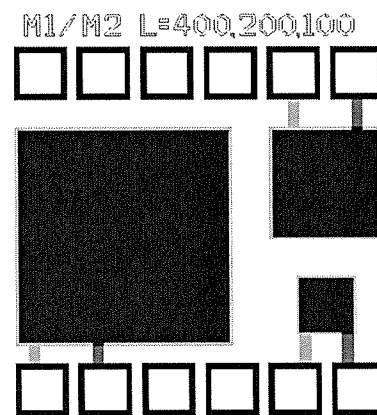


Fig. 4: M1-M2 Capacitors

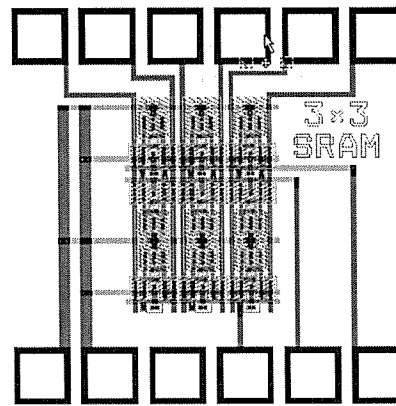


Fig. 5: 3x3 SRAM Cell

Several key challenges arose during process of the lots that played a major role in the success or failure of the test structures. The first major issue encountered was the non-uniformity of the LTO deposition. The wafers that used LTO as their ILD had been the first six-inch wafers in that dep tube in over a year. While a target thickness of 4500Å was achieved at the center of the wafer, the edge-to-edge variance was very high. The sides of the wafers

nearest to the quartz boat were the thinnest, with an average of 4000Å of LTO and the sides of the wafers nearest to the top of the boat had the thickest LTO, averaging 5000Å. This proved crucial in the via chain test structures.

The wet etch of all the wafers a M1 proved to severely undercut the metal below the photoresist. Because the wet etch chemistry is isotropic, it etches in all directions, including laterally, at the same rate. Line gratings on each die range from 0.25µm to 8µm and are used to determine the lateral etching. Using these as a metric, the wet etch undercut about 1µm of aluminum, making any feature under 2µm wide lift off the wafer. While none of the test structures used were smaller than these dimensions, it did shrink the size of the M1 links of the via chain and forced the processing steps following M1 etch to be more precise.

The first lot that used TEOS as the ILD, lot D, had the vias under etched in the BOE. A published etch rate was used instead of establishing the etch rate using a monitor wafer. This caused some of the vias to have oxide remaining in them and created opens in the via chains, as seen in Figure 6.

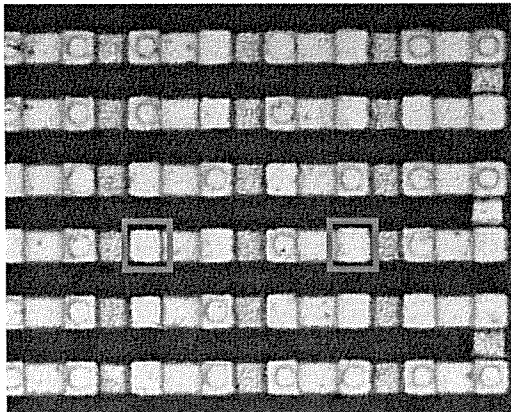


Fig. 6: Under Etch Vias

The last major processing challenge was the M2 lithography. All of the lithography steps required the Canon stepper to align the reticle to the wafer using a set of alignment marks made in the n-well oxide at the bottom of the film stack. Using a thick M2 aluminum and titanium stack, the image processor in the tool had difficulty finding and aligning to these marks. Often, the photoresist would need to be stripped off the die used for alignment and even removing the metal with a pair of tweezers in some cases. This proved to waste valuable processing time and was part of the reason for the unsuccessful via chains on lot E.

Via chains were successfully created on all the lots using LTO, but none of the TEOS lots. As

mentioned before, the non-uniform ILD had a direct effect on whether the via chains worked or not. In the thinnest areas, the via chains worked because the M2 Ti/Al did not have to travel over a very large step height. However, in the thicker ILD areas, the metal tended to break over the 5000Å step. The difference can be visible in the SEM's in Figure 7, 8 and 9. The operational via chain in Figure 7 is from a thinner LTO area, as is the tilted closer shot in Figure 8. Figure 9 shows the same 501 link chain in a thicker LTO area. One theory is that doing the M2 lithography on a highly reflective material like aluminum without a bottom anti-reflective coating (BARC) causes a high concentration of energy at the corners, which reduces the width of photoresist at that point. When the etch begins to encroach laterally, this is the first area to be undercut. Resistance measurements for the working via chains gave values varying from 400Ω to 450Ω, with the average being ~420Ω. With a theoretical value of ~100Ω existing for an aluminum bar of the same measurements, a reason for the difference could be high contact resistances at every M1-M2 contact and/or non-ideal resistivities in thin film scenarios.

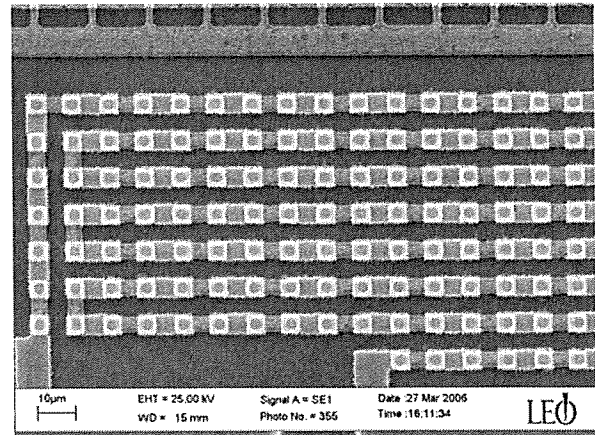


Fig. 7: SEM of Operational Via

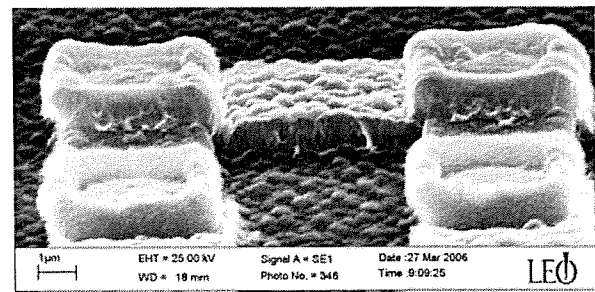


Fig. 8: Tilted SEM of Via Chain Link

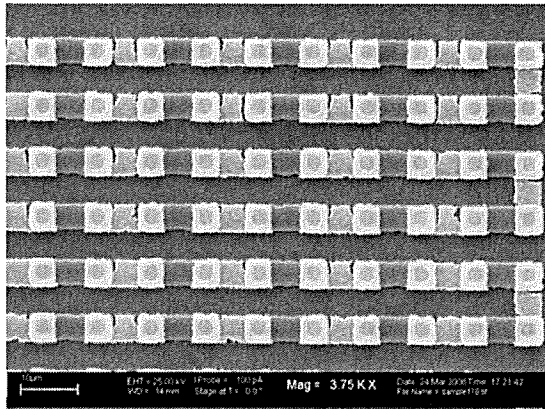


Fig. 9: Open Via Chain

The first TEOS lot, lot D, did not produce working via chains because of the under etched vias. The second TEOS lot, Lot E, had two processing issues that combined to create non-working via chains. An attempt was made to use a thicker TEOS for the final lot. Using 5000Å instead of the previous lot's 4000Å, a thicker M2 layer was needed to completely fill the taller via to make contact to the metal below. A titanium/aluminum stack totaling 1µm was used for this lot's M2. However, the metal lithography was unsuccessful after numerous attempts for the same reason it was difficult for the previous lots: location of alignment marks in n-well oxide. The thicker film made finding the fine alignment marks in the Canon stepper impossible and the lithography was completed using only pre-alignment marks as guides. This resulted in misaligned M2 lithography, but the misalignment was not enough to move the via chain photoresist off the via openings, as seen in Figure 10.

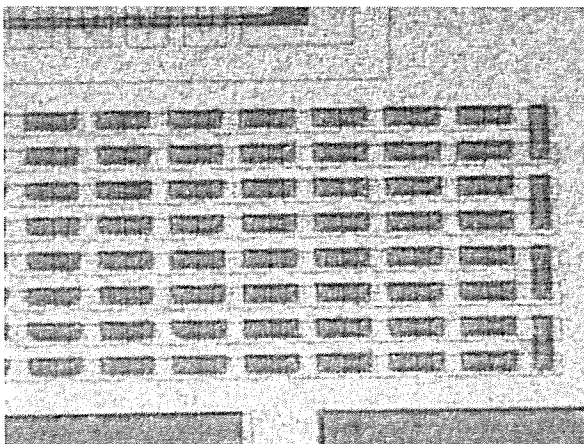


Fig. 10: Misaligned Photoresist at M2

The lot continued to the next processing step: the plasma etch of aluminum and titanium. Using a thicker metal required longer times for the

aluminum etch. Not using a thicker photoresist to coat the thicker metal, a significant amount of the metal was lost underneath the photoresist before it cleared in desired areas. If a thicker resist would have been used, the undercutting would have been minimized, as in other lots. The combination of M2 misalignment at lithography and the use of photoresist that was too thin to withstand plasma etching created open via chains across the wafers, captured in Figure 11.

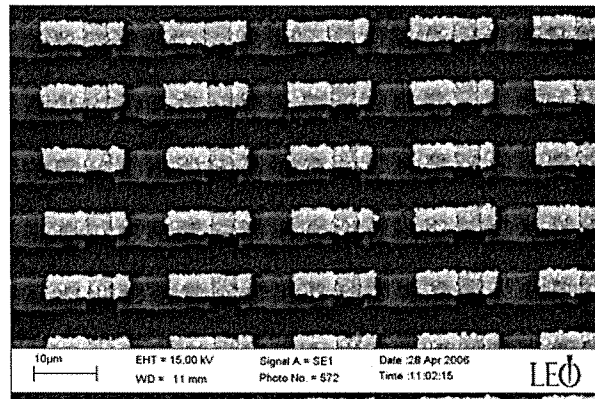


Fig. 11: Misaligned and Under Etch Via Chain

The capacitors of various sizes were tested on all lots to ensure electrical separation by placing a voltage on the underlying M1 and measuring a current at the M2 above. If any reading other than an open was measured, it meant the metal lines had created an unwanted short. For one LTO lot and one TEOS lot, actual capacitance measurements were taken on the 200µm x 200µm capacitors. Theoretical calculations offered a capacitance value of 3.5pF. The LTO capacitors averaged 3.45pF and the TEOS capacitors averaged 3.08pF. With only estimated or extracted permittivities found in publication, the values measured very close to what was predicted. These structures can be seen below in Figure 12.

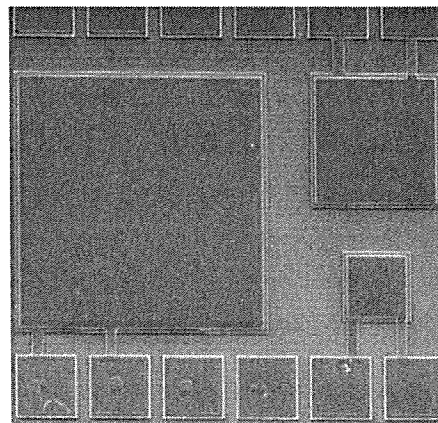


Fig. 12: M1-M2 Capacitors

The final structure tested was the SRAM cell that consisted of only overlapping M1-M2 lines. By applying a voltage to a M1 line and measuring the current of a overlapping M2 line, a determination could be made whether unwanted shorts were occurring. The SEM images in Figure 13 and Figure 14 show the M1-M2 overlays. These structures were tested on every wafer and tested as an open in most cases. One caveat to this structure is that in areas of thicker ILD or over etched metal, the lines would break and could test as an electrical open not because the overlapping lines did not short, but because the lines broke before contact. Many of the structures that tested as opens were examined in the SEM to view breaking in the lines and most did not exhibit any M2 separation over step heights.

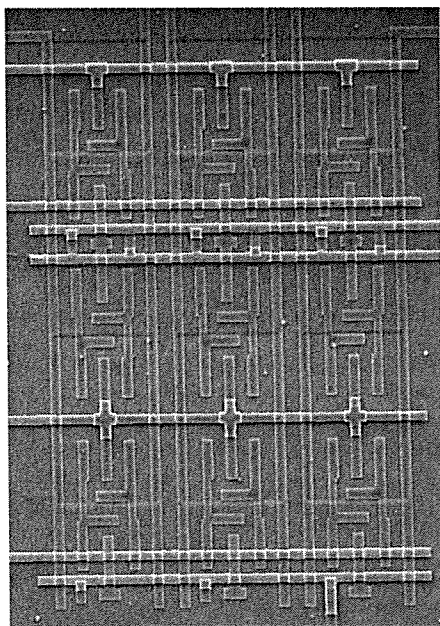


Fig. 13: M1-M2 Overlay in SRAM Cell

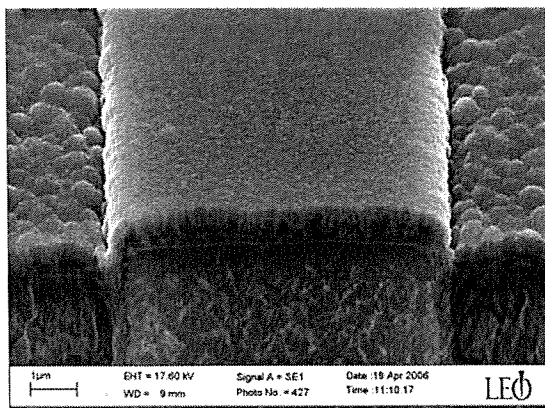


Fig. 14: M2 Line Crossing M1 Line

IV. CONCLUSIONS

A two level metal process was successfully design and fabricated at RIT's SMFL. Using subtractive aluminum at a 2µm design rule, several very stringent test structures were evaluated on five lots of varying processing to determine the best parameters to create a bilayer metallization. The optimum process utilizes 4000Å of LTO as an interlayer dielectric, an unheated metal2 sputtered deposition of 1000Å of titanium and 7500Å of aluminum, a chlorine-based plasma etch for M2 aluminum removal, and a fluorine-based plasma etch for M2 titanium removal. Key processing steps outside of the lot matrix include establishing etch rates at every etch step on monitor wafers first and running FEM's at every lithography step to determine best focus and dose for that step.

V. ACKNOWLEDGEMENTS

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VI. REFERENCES

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