Design and Manufacturing of Silicon PIN Diodes Utilizing Silicon on Insulator Technology

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Abstract—**The goal of this project was to design a process to form a PIN structure on silicon on insulator (SOI) wafers. IBIS donated the wafers for this project. Using a combination of standard and novel wafer processing techniques allowed for successful completion of the device. These techniques involved a four-layer mask process that utilized both state of the art and older tool sets. A methodology for lithographic processing of wafer pieces has been expanded upon and documented for future use.**

Testing demonstrated resistor like behavior opposed to the expected diode behavior. This result is indicative of a short through the device. The observed undercutting of the buried oxide is the most likely culprit. Undercutting would allow the surface silicon to come in contact with the bulk silicon creating an electrical path around the intrinsic region of the device.

***Index Terms*—Diode, KOH, PIN, SOI**

I. Introduction

The detection of photonic signals is critical for high-speed communication devices. A cornerstone of these systems is the PIN detector. The PIN detector is a p-n junction diode that responds to a photon stimulus with an electric current. The electric current can be amplified into a signal or measured and related to the incident intensity. Photons are detected by generating electron-hole pairs (EHP) in the intrinsic region. The built in electric field due to the reverse biased p-n junction sweeps the pairs to the contacts resulting in detectable current. Developing the processes and manufacturing techniques to produce this device will help progress the Rochester Institute of Technology towards the communications technology sector.

In the world of high-speed devices a device such as this creates the possibility of using light to transfer information instead of electrons. The detector is the link between the optical and electrical worlds. This will enable a new realm of data transfer between different systems on a single chip as well as multi-chip packages. The goal of this experiment was to develop and manufacture PIN diodes varying the total size of the device and the width of the intrinsic region. This will provide upon electrical testing correlations between size and current density and between intrinsic region width and sensitivity.

The physics behind the operation of a PIN diode are not as complicated as other alternatives. It is a three-part device involving a highly doped p region, a highly doped n region, and an intrinsic region. The most significant part is the intrinsic region. It is an area of few mobile carriers an can vary in size depending on application. This is also the section where the photons will enter. The other two sections connect to the rest of the circuit. They also allow establish the required electric field in the intrinsic region. The electric field is applied by reverse biasing the diode. The incident photons create an electron-hole pair (EHP). Since the device is biased, the EHP is swept to their respective polarity. This movement of charge from the *i*-region to the doped regions is a current. It is this current that is of most interest.

Another current that is of interest is the dark current, or off current. This is the amount of current that is always flowing through the device. Dark current exists since there are always some free carriers in the intrinsic region. Certain processing methods have been shown to increase the dark current due to plasma damage of the silicon. Dark current is background noise when trying to detect the on current. Since the on current can be very small it is important to minimize dark current.

II. Design and Manufacturing

A correlation between different current densities and physical device dimensions needed to be tested. To accomplish this PIN diodes were designed using the Mentor Graphics software suite of various sizes. Physical sizes range from one micron to one centimeter in device length with intrinsic regions ranging from one to ten microns. The intrinsic region was defined by the placement of the doped n and p regions. For electrical isolation of the devices from each other and the bulk SOI wafers were required. Mesa etching each device provided the final isolation. The doped regions were defined using a tetraethylortho silicate (TEOS) layer as a diffusion barrier. TEOS is a dielectric film that can be easily

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deposited via plasma enhanced chemical vapor deposition. This allowed fast turn-around and multi level processing in a few days.

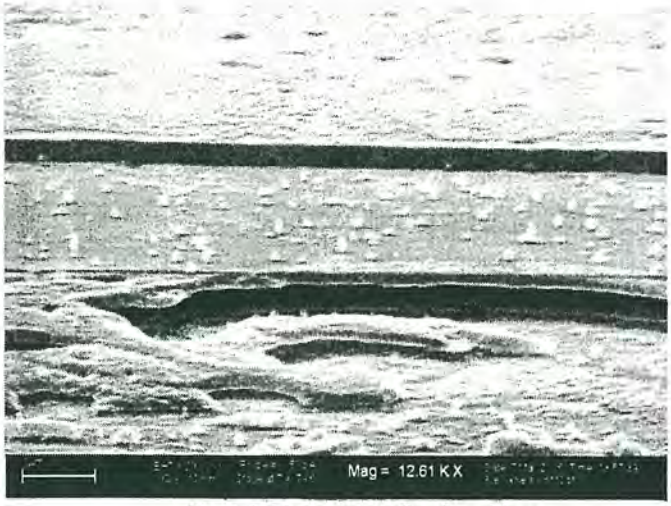

Figure 1: Undercutting of surface silicon.

The device wafer was broken into two-inch squares. This successfully kept the total cost lower, but presented its own challenges. Due to wafer handling, it is not always straightforward to process portions of wafers. Certain tools are incapable of processing pieces while others require modification. Even though the tool set was now limited, the process flow for this project was flexible enough to work. The workhorse of this project was the Karl Suss Mask Aligner. This provided the means for lithography and overlay for the mask layers. Although the tool can be run manually, it still had difficulties with pieces. The tool requires vacuum on the wafer chuck that was not being provided be a single piece of wafer. This was remedied by placing a thin sheet of aluminum under the piece on the chuck. The other necessary tools readily accepted wafer fragments. Buffered oxide etch (BOE) was used to remove the TEOS layers and potassium hydroxide (KOH) was used for the mesa etch. The main manufacturing challenges involved the manual alignment of the mask layers to each other. Future mask revisions will alleviate this problem. Another significant challenge was the KOH mesa etch. The expected etch rate differed greatly from the actual. Serious pitting was apparent as well. This pitting was determined to be a failure mechanism for the device. An etch study of the SOI wafers used in this project needs to be done prior to a second process run. It is anticipated that a dry etch will perform far superior to the KOH wet etch.

III. Results

The processing of pieces led to many challenges concerning alignment and overlay. This however was not the most significant processing issue. Upon inspection of the device in the scanning electron microscope (SEM) the reasons for the rough silicon surface after the KOH etch were revealed. In the silicon that was etched were micron size areas that had etched entirely through the surface silicon. These holes were lattice defects that occurred during the manufacturing of the SOI wafers. KOH will attack defects in silicon etching them faster than the bulk surface. This can be seen in figure 3. These pinholes exposed the underlying buried oxide. If this were known to happen, the process flow would have been

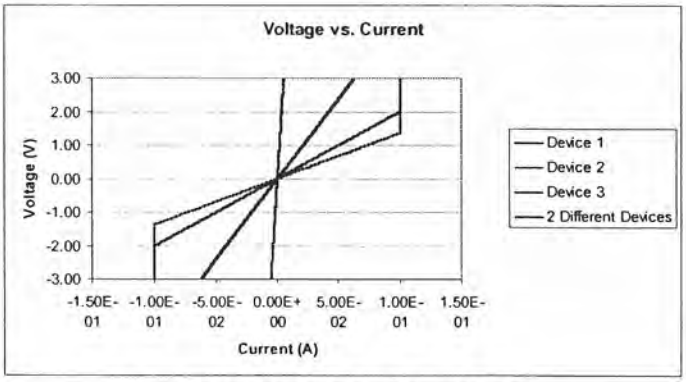

Figure 2: I-V Characteristics for tested devices.

altered to compensate. The current process flow used TEOS, which is basically the same material as the buried oxide, to mask the n and p diffusions. After each diffusion the oxide was stripped and deposited again. Since the buried oxide was exposed through the pinholes the subsequent removal of each TEOS layer removed part of the buried oxide. This eventually led to the collapse of the surface silicon layer. This collapse formed an electrical contact between the surface silicon and the bulk. This contact provided a current path around the diode. This is readily seen in the device electrical tests. Each and every device tested demonstrated a linear relationship across the test sweep as is seen in figure 2. This is indicative of a resistor. The resistor in this case is the bulk silicon beneath the device. To ensure that all the devices were shorted to each other one side of a PIN diode was tested while another diode acted as the opposite lead. Again a resistor behavior was seen. This unequivocally demonstrated all the devices were indeed shorted

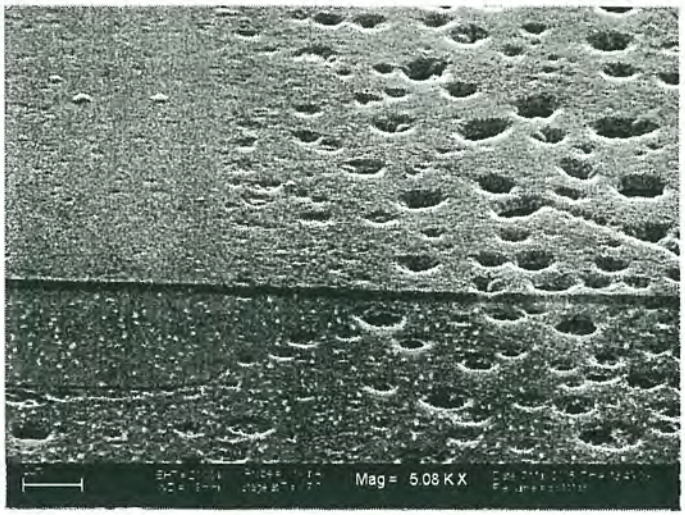

Figure 3: Pinholes etched in silicon.

IV. Conclusion

Electrical testing of the device proved that it indeed did not function as desired. This is the only negative aspect of this project. A large amount of information was learned as the project progressed. A more thorough understanding of optoelectronics as well as fabrication challenges is the ultimate goal of a project such as this. New projects will be undertaken to explore the results of this one. These projects may include further studies on the etching of SOI in KOH. Plasma processing will also be considered as an alternative. The author is optimistic that a second revision will provide functional devices as well as more data that will lead to an even better project in the future.

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References

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