Characterization of $TiSi_2$ Process And Electrical Properties

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Abstract—**The goal of this experimentation consists of the formation of $TiSi_2$ and demonstration of its electrical properties. The successful formation of a $TiSi_2$ product was be confirmed by scanning electron micrograph (SEM) images, Rutherford Backscatter Spectroscopy (RBS) data, and electrical characterization. Following an annealing heat treatment, the RBS data indicated the presence of a Si substrate, a film that compositionally appears to be $TiSi_2$, and a surface layer of TiO_2. The electrical testing indicates the presence of ohmic behavior, and the resistance is strongly dependant on the furnace annealing and rapid thermal processing (RTP) treatments.**

Index Terms—**ohmic contact, silicide, $TiSi_2$, Titanium silicide.**

I. INTRODUCTION

THIS experimentation is designed to demonstrate an improved process for the formation of $TiSi_2$ and to observe its electrical behavior. Also, in the potential formation of $TiSi_2$, there is interest in the fabrication of both the first and second phases of $TiSi_2$.

$TiSi_2$, is formed by a thermal reaction between the silicon surface and a titanium film. The titanium interacts with the silicon at a consumption rate that produces approximately 2.5nm of $TiSi_2$ for every 1nm of silicon.

The two phases of $TiSi_2$ are the C49 phase and the C54 phase. The C49 phase is the first phase in $TiSi_2$ formation and exhibits a higher resistivity value due to a lower number of grain boundaries. The C49 phase can be formed by a thermal reaction between the Titanium and the Silicon at a temperature around 650°C. The C54 phase is the second phase in the $TiSi_2$ formation. The C54 phase has a lower resistivity due to its triple-grain boundary structure and is formed by a second thermal treatment with annealing at a temperature around 900°C. Both C49 and C54 are phases of compositional $TiSi_2$, but the C54 phase has a lower sheet resistance in comparison to the C49 phase.

When evaluating materials such as barrier layers or silicides, the method of Rutherford Backscattering Spectroscopy, or RBS, is a useful metrology application. RBS is a method that sends energized ions toward a given sample and measures the energy of the returning backscattered ions. The response of the energized ions is dependent upon the mass of the target element. Ultimately, RBS can provide a quantitative analysis of thin films, layered structures, or bulk material, as well as measurements of surface defects and impurities that may have been caused by heavier metallic impurities on the Silicon substrate. The analysis of RBS is provided in a spectrum format, where the RBS spectrum is plotted as the Intensity versus the amount of energy. So the intensity is the actual counts being measured and the energy is shown as the channel number. The spectrum will plot the elements present in the sample by graphing peaks that are proportional to the element concentration. Information provided by the RBS will confirm the formation of $TiSi_2$ before additional work is completed and electrical testing is performed.

This work is part of capstone design project for a B.S. degree in Microelectronic Engineering at the Rochester Institute of Technology (RIT), Rochester, NY. The results of the project were first presented as part of the 23rd Annual Microelectronic Engineering Conference, May 2005 at RIT.

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II. PROCEDURE FOR FABRICATION

A. $TiSi_2$ Formation

The process began with the use of n-type <100> Si wafers with a starting resistivity of 15 Ω-cm. Initially, the critical aspect of experimentation was the ability to form $TiSi_2$. The deposition of Ti was via sputtering on the CVC601 Sputtering System. Before the sputtering, the wafers were dipped in a 50:1 HF solution to remove any native oxide that may have existed on the surface of the wafer. This 20 second HF dip ensures a better contact between the sputtered Ti layer and the Si substrate. Three wafers were sputtered; one wafer acted as a dummy with a strip of tape, which was later tested using the Tencor P2 Profilometer for a step-height of the Ti film deposited. The two remaining wafers were loaded into the Bruce furnace for formation of the C49 phase formation. The furnace recipe was customized specifically for this application and titled "Haydock Anneal", as recipe #740 for tube 7 of Bruce 2 furnace. This recipe was designed to ramp up to a main soak step of 6 minutes at 650°C, and then ramp down to room temperature. One of these wafers was sent to the University of Central Florida for RBS analysis. An additional six wafers were processed with a blanket Ti film, then using this anneal recipe for the C49 silicidation phase. Three of the six wafers were run through a Rapid Thermal Annealing (RTA) process for the C54 silicidation phase. From each set of three, one wafer was etched using a $1H_2SO_4 + 2H_2O_2$

solution, was measured for sheet resistance, and was examined using the SEM.

B. Device Fabrication using $TiSi_2$ product

With confirmation from the RBS data and the resistivity probe that $TiSi_2$ had in fact been formed, the processing for the device wafers began. Four wafers were cleaned and approximately 500Å of thermal oxide was grown on the wafer surface in the Bruce furnace. The next step involves the coating of photoresist and then photo-patterning. All lithography performed used a mask set which contained Transfer Length Method (TLM) structures, which will be used later for measurements and data analysis. After the patterning of the oxide layer, the oxide was etched using an HF Buffered Oxide Etch (HF BOE) for 1 minute. At this point, all four wafers were sputtered with a Ti blanket layer over the oxide and were annealed using the Bruce furnace recipe designed for the first C49 silicidation phase.

After the first Ti anneal, two of the four wafers were processed in the Rapid Thermal Anneal furnace at 900°C for 90 seconds each. The second anneal in the RTA is designed to create the second C54 silicidation phase. The remaining Ti that was not consumed by the silicidation process was etched for 30 seconds in a wet-etch solution containing $1H_2SO_4$ + $2H_2O_2$ that was heated to 90°C.

For contact formation, Al was sputtered and patterned on the front side of the wafer and the contact pattern was etched using the Al wet etch. Al was also sputtered on the back-side of the wafer for a second electrical contact.

One wafer from the first phase and one wafer from the second phase were each tested for electrical behavior and were later SEM-ed for cross-sectional images.

III. RESULTS

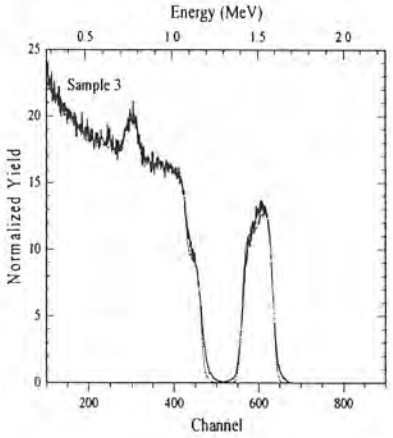

Figure 1 – RBS spectrum from University of Central Florida.

As seen in Figure 1, the RBS analysis detected the presence of several different films. Compositionally, there were three main layers that were detected by the RBS analysis. The first base layer was the Si substrate. Nearing the surface of the wafer, there was a layer detected that was composed of 33.3% Ti and 66.6% Si with a thickness of approximately 1180Å. This layer is the $TiSi_2$ layer desired from this process. The last layer detected by RBS was at the very surface and was composed of 33.3% Ti and 66.6% O_2 with a thickness of approximately 1100Å. These thicknesses are approximated because the RBS analysis gives a thickness in terms of atoms/cm^2 and the desired measurement is in terms of standard measure. This can be converted using the following equation:

$$t = \frac{T\sum\left(M_i F_i\right)}{\rho N_A} \qquad (1)$$

Where t is the real thickness in metric measure, T is the RBS thickness provided in atoms/cm^2, M_i is the atomic weight in grams/mole, F_i is the fraction of material in the compound, ρ is the compound density in g/cm^3, and N_A is Avogadro's number of 6.025×10^{23} atoms/mole. For reference, the atomic weight of $TiSi_2$ is 104.05 g/mole and the density is approximately 4.39 g/cm^3.

Sheet Resistance (ohm/sq)		
	Furnace	***Furnace +RTA***
	2.703	0.774
	2.825	0.702
	3.165	0.721
avg.	2.898	0.732

Table 1 – shows the sheet resistance measurements for the blanket $TiSi_2$ wafers.

The information provided in Table 1 shows that the sheet resistance across a blanket wafer of $TiSi_2$ drops by almost four times between the wafers treated with only the furnace anneal and the wafers that had undergone the second anneal in the Rapid Thermal Anneal process. The following SEM image shows a cross-section of the blanket wafer:

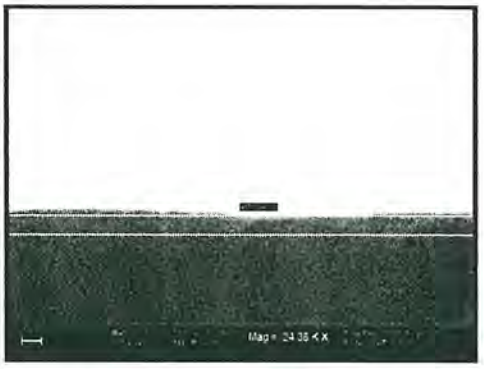

Figure 2
Cross-sectional SEM image of a blanket wafer treated with furnace and RTA anneals. The film thickness is given by the SEM as being 197.4nm.

The RTA processing for the three blanket wafers were monitored closely for any possible variations in temperature and also to see if the furnace maintained the proper anneal temperature. The temperature profiles are shown as follows:

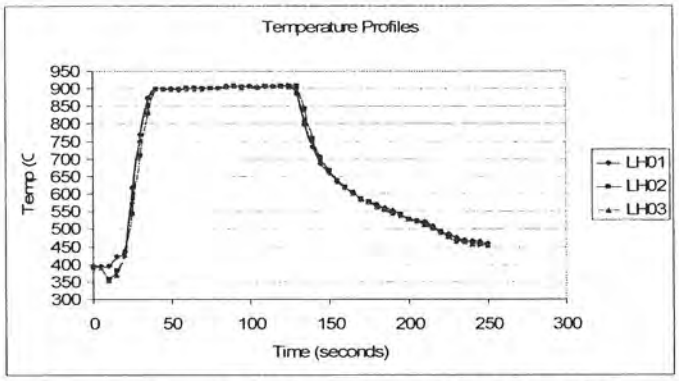

Figure 3 – Temperature profile graph from the Rapid Thermal Anneal process.

The anneal recipe, as shown in Figure 3 has good uniformity and repeatability with a temperature of 900°C for approximately 90 seconds. This recipe will be used for later processing with the device wafers.

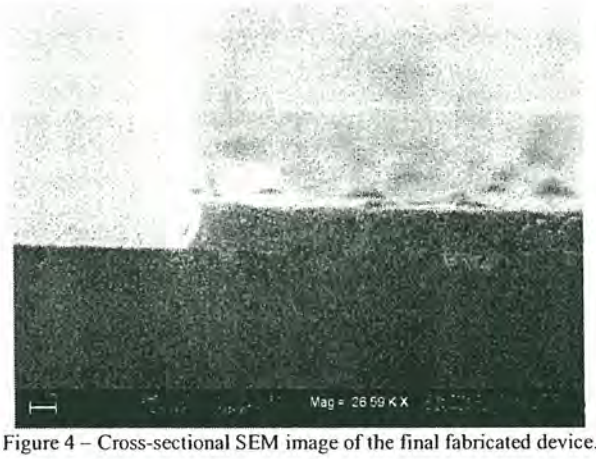

Figure 4 – Cross-sectional SEM image of the final fabricated device.

After fabrication of the device wafers, two of the wafers, one from each thermal furnace treatment, were prepared for SEM imaging. The above image, shown in Figure 4, shows the cross-section from a wafer that had seen both the furnace and second anneal treatment.

Again, one of each wafer treatment was taking to the test lab for electrical characterization. The mask set that was used contained Transfer Length Method test structures. These structures appear 'ladder'-like and are equally spaced from each other. With these features, the overall distances could be measured from contact to contact and the contact resistance can be measured. The following graphs show I-V curves and summarizes the ohmic behavior of the 12 um x 12 um contacts before and after the RTA processing.

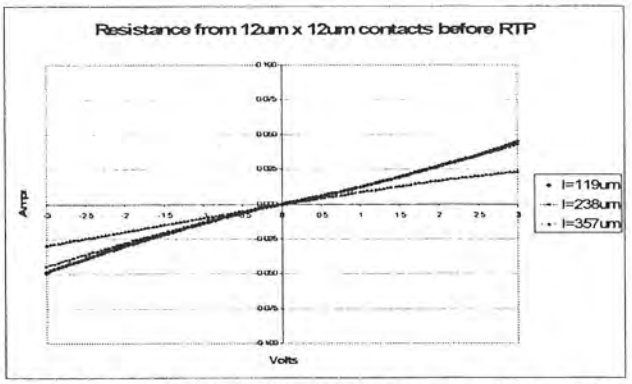

Figure 5 – I-V plots for 12um x 12um contacts at varying distances before RTA.

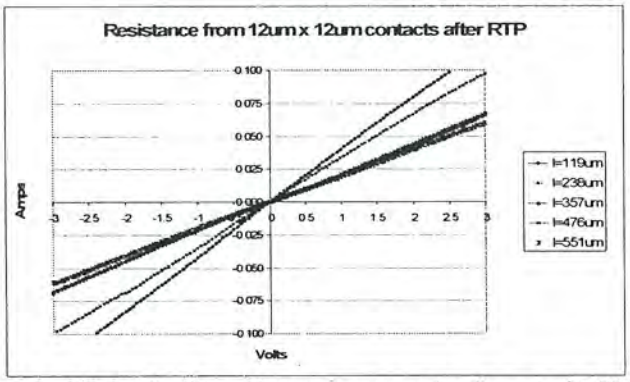

Figure 6 – I-V plots for 12um x12um contacts at varying distances after RTA.

Figures 5 and 6 show the relationship between the distance between contacts and the value of resistance. The steeper slope shown in Figure 6 corresponds with a lower resistance value, whereas the shallower slope of Figure 5 depicts that the wafers that did not receive the RTA process have a higher resistance on the $TiSi_2$ contacts. The following graph summarizes both Figures 5 and 6 to show clearly how the resistance changes in respect to the distance between contacts for each furnace anneal treatment.

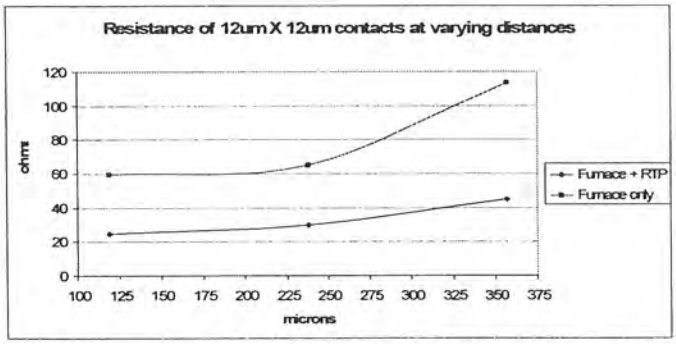

Figure 7 – Comparison between furnace treatments with relation to resistance and distance between contacts.

From Figure 7 it is clear to see that the resistance drops nearly a third between the furnace only treatment and the furnace treatment that was followed by the RTA process.

IV. Conclusion

A successful process was designed for the fabrication of TiSi2 and its dual phases of C49 and C54. The two phases were recognized by the significant shift in sheet resistance after the second anneal was performed using the Rapid Thermal Annealing process. With the knowledge from this experimentation, the production of ohmic contacts with $TiSi_2$ can be implemented into future processing at RIT.

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Laurel E. Haydock, originally from Webster, NY, received her B.S. in Microelectronic Engineering from Rochester Institute of Technology in May 2005. She had attained co-op work experience with Motorola's CMP Research and Development group in 2003 and with Freescale Semiconductor's Device engineering group in 2004. She will be returning to Freescale Semiconductor as a rotational engineer starting July 2005.