Integration of Nickel Monosilicide (NiSi) into an RIT SMFL NMOS Device

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Abstract—**A nickel silicidation process has been developed for the Semiconductor & Microsystems Fabrication Laboratory (SMFL) at Rochester Institute of Technology (RIT). NiSi and Ni_2Si were obtained in doped source/drain and polysilicon gate regions respectively at rapid thermal annealing (RTA) condition of 500°C for 60 seconds. The sheet resistance of nickel silicide in both regions was measured to be 0.45Ω/□ – 0.5Ω/□. Nickel silicide was also integrated into an RIT NMOSFET process where silicide was formed over the S/D and polysilicon gate regions. Rutherford Backscatter and x-ray diffraction data showed the formation of NiSi phase in the S/D region and Ni_2Si in the polysilicon region. Preliminary electrical data from NiSi S/D NMOS showed an increase in drain current by about 1.5 orders of magnitude, an increase in threshold current by 1 order of magnitude, a decrease in threshold voltage by ½ , and significantly better gate control.**

Index Terms—**Nickel Silicide, NiSi, NMOS Integration, RBS, XRD, Silicide.**

I. INTRODUCTION

As CMOS technology transitions between process nodes, the junction depths and contact cuts for the source/drain regions are decreased. It is important that the materials used to form metal contacts to these regions have extremely low contact and sheet resistances. One class of material that meets such strict requirements is a silicide - a low resistivity alloy that forms between silicon and several metals. Titanium silicide ($TiSi_2$) and cobalt silicide ($CoSi_2$) have been thoroughly studied in industry and implemented into modern devices. However, alternative silicides are needed to ensure further device advancements due to the limitations of these traditional silicides. $TiSi_2$, for example is an ideal technology for larger linewidths (greater than 0.25 μm), but due to the linewidth dependence on its resistivity, it is not applicable for smaller geometries. One attractive alternative is nickel monosilicide (NiSi). NiSi has been reported to have comparable resistivity as traditional silicides, yet consumes less silicon during formation. NiSi also exhibits considerably less line width dependence, is formed with a single thermal treatment, and has a relatively planar silicide-silicon interface. However, implementation of NiSi into future generation devices has been delayed by the limited knowledge of its thermal stability and process integration.

The objective of this work is to develop and implement a nickel silicidation process into a MOSFET device at RIT. The RIT SMFL 2μm NMOS process was used to fabricate transistors in which nickel silicide was formed in the source/drain as well as the polysilicon gate region. The Rutherford backscatter spectroscopy (RBS) technique was used to determine the specific nickel silicide phase(s) and thickness formed in the S/D and gate regions. In addition, x-ray diffraction (XRD) was used to confirm the presence of nickel silicide in the respective regions of interest. Nickel silicide S/D and gate NMOS device has been fabricated using RIT SMFL 2μm NMOS process in conjunction with the normal NMOS device for baseline comparison of performance.

II. EXPERIMENTAL PROCEDURES

A. Nickel Silicidation Process Development

The development of nickel silicidation was done using 6" p-type silicon wafers with sheet resistance in the range of 620-680 Ω/□. Each wafer was divided into four regions as shown in Fig. 2.1.

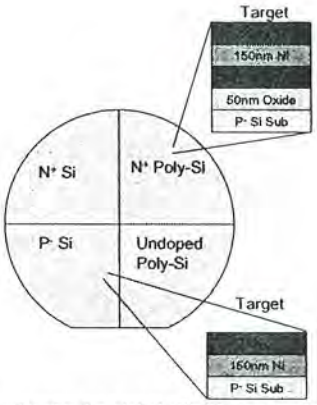

Fig. 2.1. Division of wafer for nickel silicidation experiment.

The upper two regions are highly doped N^+ silicon and poly-silicon regions representing the conventional source/drain and polysilicon gate MOSFET respectively. The lower two regions are the starting P^- silicon region and non-doped polysilicon

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region. These lower regions is anticipated to represent future SFET and FinFET source/drain and gate region where the conventional S/D and polysilicon gate doping will be completely replaced by silicides. More emphasis will be placed on studying the upper two regions. Results from these highly doped regions will be critical in the subsequent integration of nickel silicide into a NMOS device.

All starting wafers were cleaned using the standard RCA clean method common in the semiconductor industry. The RCA cleaning is necessary to minimize metal and organic contamination. A pad oxide with thickness of 50nm was thermally grown in dry O_2 ambient on all wafers, and a low-pressure chemical vapor deposition (LPCVD) polysilicon film with a thickness of 200nm was deposited on top of the grown oxide. The polysilicon and pad oxide were then completely removed from half of each wafer, with the major flat oriented as shown in Fig. 2.1, using dry etch chemistry with positive photoresist protecting the other half of the wafer. The protective photoresist was then removed and a new coat of photoresist was spun. The newly spun photoresist was then removed from half of each wafer with the axis perpendicular to that of the remaining polysilicon and pad oxide. This is to block the subsequent ion implantation process. All wafers were then implanted with P^{+31} ions having energy of 75 KeV. The protective photoresist was then removed and all wafers were annealed in a thermal furnace at temperature of 1000°C for dopant drive-in and activation. Upon the completion of the thermal process, all oxide grown during the thermal drive-in was removed from the surface of the wafer by wet etch in HF chemistry. This was followed by a RCA clean with an additional HF dip at the end prior to metal deposition. The wafers were immediately loaded into the CVC 601 sputter tool and allowed to pump down overnight with at least 10 minutes heating to promote faster outgasing of the chamber. Nickel metal, with thickness comparable to that of the polysilicon and oxide stack, was sputtered onto all wafers at base pressure of less than $5x10^{-6}$ Torr and deposition pressure of 5.0 ± 0.1 mTorr in an argon ambient (~17.0 sccm). A thin titanium capping layer was also sputtered on top of the nickel layer to prevent oxidation and contamination of the nickel metal layer prior to silicidation without breaking vacuum.

Each wafer was RTP annealed at different time and temperature. The specific process details may be found in Table I. The temperature was varied from 500°C to 750°C for a duration of 60 sec or 120 sec. The pyrometer temperature sensors of the RTP were limited to a range of ~380°C or above, and the stabilization of such low temperature was not adequate. Therefore, no runs were done at temperature below 500°C where Ni_2Si was known to be formed at.

Once the silicidation process has completed, all un-reacted nickel and the titanium capping layer were removed by wet etching in 1 part H_2SO_4 : 2 part H_2O_2 at 90°C for at least 30 sec. The removal of titanium is evident by the reddish discoloration of the chemical solution.

B. Nickel Silicide NMOS Integration

Upon the successful study of nickel silicidation, the optimal silicidation process and parameters were used to implement nickel monosilicide into an NMOS device at RIT. The robust RIT SMFL 2μm NMOS was chosen for the nickel silicide implementation. The chosen process has NMOS transistors with the critical gate dimension ranging from 0.4μm to 48μm, a gate oxide thickness of 31nm, and a polysilicon gate thickness of 350nm. In addition to regular poly-gate transistors, the design also has metal gate as well as metal gate with field oxide (403nm) devices.

Similar to the conventional use of silicide in device fabrication, the integration of nickel silicide was targeted in the source/drain regions as well as the polysilicon gate. The NiSi integration began after the S/D and poly gate dopant implantation. Once P^{+31} dopant has been implanted, a S/D thermal annealing step at 1000°C was done in a tube furnace to repair crystal damage and active the dopant. This step was done prior to the silicidation process to avoid any unknown and unwanted transformation of the silicide that could have taken place at such high temperature. To avoid any shorting of the source/drain and poly gate, an oxide sidewall spacer was used to provide the necessary spacing between the areas. Nickel silicidation only occurs where the nickel metal is in direct contact with silicon substrate or polysilicon areas. The sidewall spacer was made base on the combine thickness of the polysilicon and the oxide gate stack (360nm). Therefore it was unknown at the time whether the sidewall spacer's width was thick enough to successfully account for the lateral encroachment of the silicide during silicidation. Fig. 2.2 shows the complete details of the silicide integration steps.

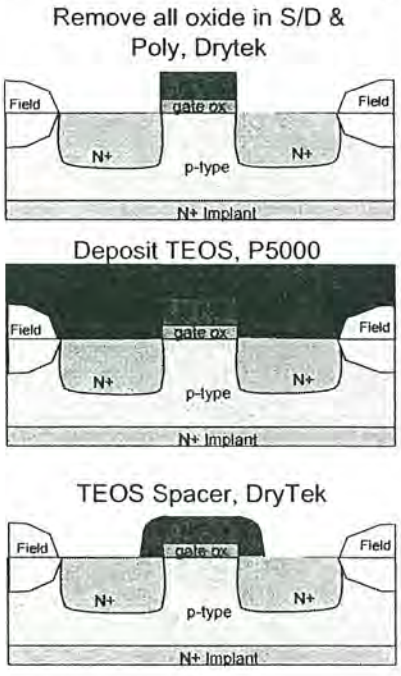

Fig. 2.2a. Nickel silicide integration process flow.

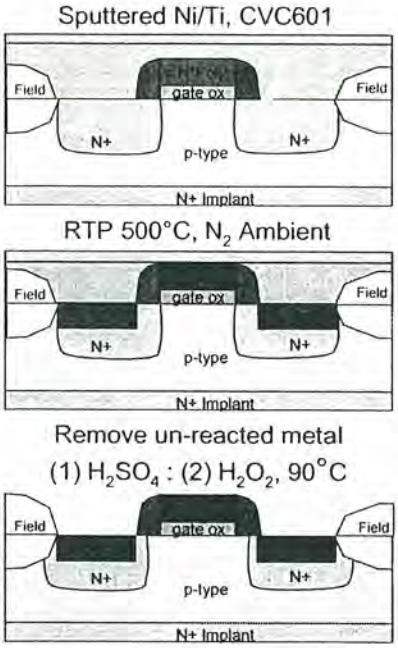

Fig. 2.2b. Nickel silicide integration process flow.

III. RESULTS AND DISCUSSION

A. Nickel Silicidation Process Development

Table I show the sheet resistance (Rs) of the silicon and polysilicon surface after silicidation. The sheet resistance for all regions was in the range of 0.50-1.18 Ω/□ prior to RTP annealing. In term of sheet resistance, results for RTP anneal at 500°C were the lowest, suggesting the presence of the NiSi phase. There is a slight increase in sheet resistance for annealing temperature at 520°C for 120sec. Assuming lower noise level in the Rs Mapper tool, the results suggest the initial transformation of the NiSi into $NiSi_2$ and that the slight increase in Rs is due to the slight mixture of $NiSi_2$ with NiSi silicide phase. The Rs values for the RTP anneal at 750°C clearly show the presence of predominantly $NiSi_2$ phase characterized by significantly higher Rs. In addition, significant visual changes were observed on the wafer surface after the RTP process. On the side with the substrate silicon exposed, yellow colored rings were seen near the edge of the wafer. This discoloration has been seen before in other project involving titanium silicide. Therefore, it was hypothesized that the discoloration seen here was the initial reaction of the titanium capping layer since the nickel metal was thinnest near the edge of the wafer.

TABLE I
POST RTP ANNEALING SHEET RESISTANCE

RTP Condition		R_s (Ω/□)			
Temp (°C)	Time (sec)	N^+ Si	N^+ Poly	P^- Si	Poly-Si
*500**	*60*	*0.45*	*0.58*	*0.50*	*0.59*
520	120	0.41	0.93	0.60	0.94
750**	60	1.45	6.86	0.55	4.95

*After the removal of all un-reacted metals, the wafer received an additional RTP anneal at identical time and temperature. A negligible difference in Rs was found.

**After annealing, a yellowish discoloration was observed around the outer edge of the wafer with bare silicon. A whitish line of discoloration was observed on the surface of both polysilicon regions. The yellowish discoloration was due to the initial reaction of Ti metal.

In order to observe the effect of subsequent thermal processes on the newly formed silicide, the wafer was given an additional RTP anneal at 500°C for 60sec after the wet etch removal of all un-reacted metals. The resulting change in Rs measured after the second RTP anneal was found to be negligible. This suggests that the silicide was able to withstand subsequent thermal processing such as the sinter process at 450°C.

Clearly, the optimal silicidation condition to obtain NiSi with the lowest sheet resistance is at 500°C based on the limited runs shown in Table I. To further investigate the actual phase(s) formed on this particular wafer, a sample from the doped silicon and the doped polysilicon were sent out for RBS analysis. The sample was taken from another wafer with RTP treatment at 500°C for 60sec. No wet etching chemistry was done to remove the un-reacted metals. An RBS analysis is capable of distinguishing between different nickel silicide phases as well as the depth of the silicide. Fig. 2.3 shows the results obtained from the RBA analysis.

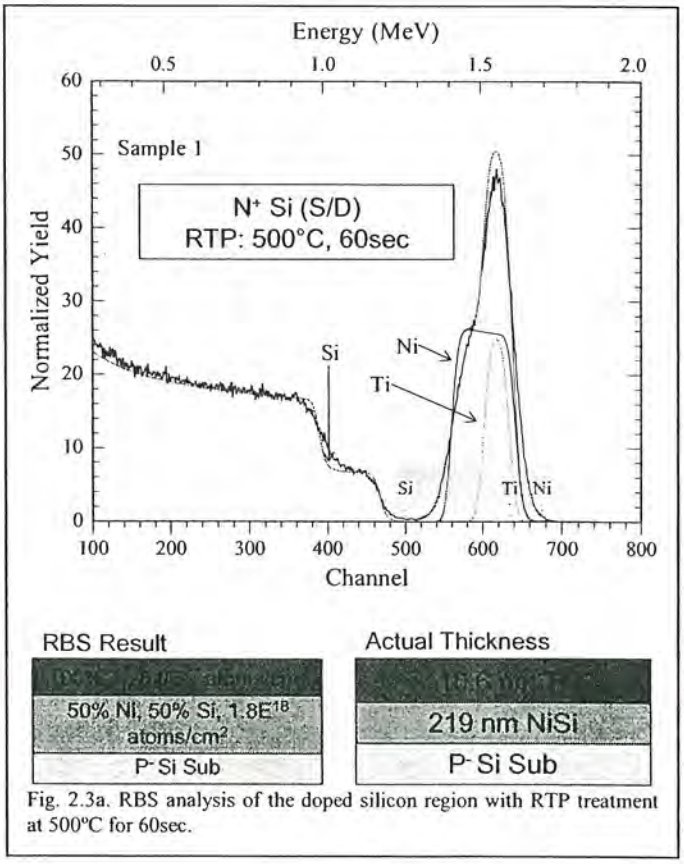

Fig. 2.3a. RBS analysis of the doped silicon region with RTP treatment at 500°C for 60sec.

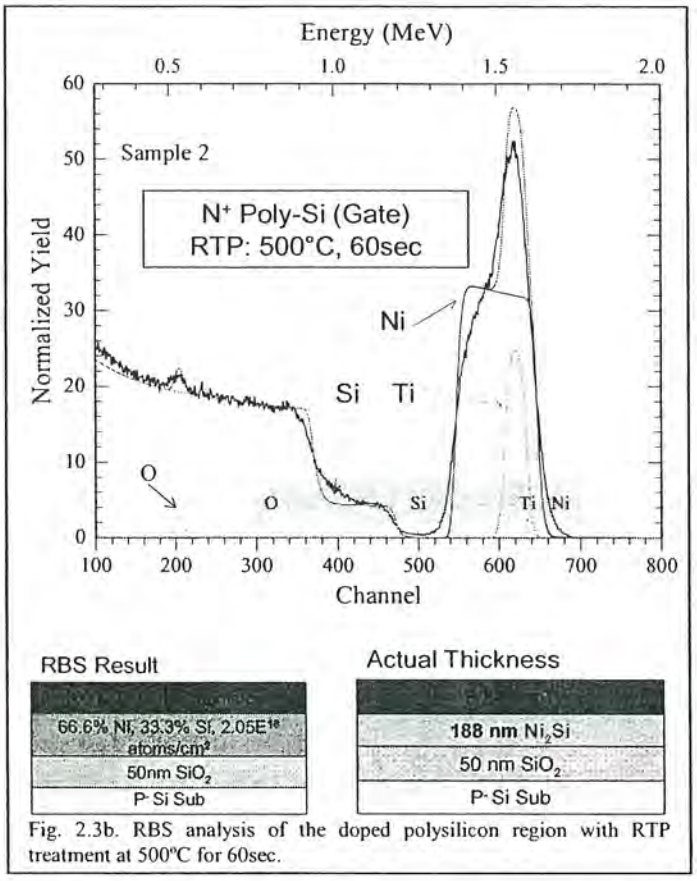

Fig. 2.3b. RBS analysis of the doped polysilicon region with RTP treatment at 500°C for 60sec.

The RBS plots give the surface markers for each element found. These markers are found near the x-axis in the shaded rectangular box. In Fig. 2.3b for example, the oxygen surface marker is found near the channel value of 300 where as the nickel surface marker is found around 680. If an element's peak is found on its surface marker, then that element is located on the surface of the sample. For Fig. 2.3b, the Ti peak is found directly on its surface marker which can be interpreted as being located on the surface of the sample. The Ni peak is found slightly to the left of its surface marker which suggests the actual location of the nickel to be immediately following that of Ti. The cross-sectional view in Fig.2.3b depicts the correct order of the film stack. Similar analysis applies to the doped silicon sample in Fig. 2.3a. The RBS analysis also gives the absolute composition ratio of each element in a film. For the doped silicon sample, 100% of Ti with a concentration of $6x10^{17}$ atoms/cm^2 was found. There is exactly a 1:1 ratio of Ni:Si found below the Ti layer. This clearly indicates the predominant presence of NiSi phase as concluded from the Rs results. However, the Ni:Si ration found on the polysilicon sample was 2:1 which clearly correlates to the predominant presence of Ni_2Si phase. This is the initial silicidation phase of nickel silicide with Rs value slightly higher than that of NiSi. The presence of Ni_2Si is due to an incomplete phase transformation during the RTP anneal step. A longer annealing time is needed to completely transform this phase into the targeted NiSi phase.

The concentration of each film given by the RBS results can be converted into actual film thickness through the relationship shown in equation 1. To ensure proper conversion, the atomic density of each film composition must be known. Refer to equation 1.

$$t = \frac{T\sum(M_i F_i)}{\rho N_A} \quad (1)$$

t = actual thickness
M = atomic mass
ρ = atomic density
T = RBS thickness
F = fraction ratio
N_A = 6.025E^{23} atoms/mole

The atomic density of the Ni_2Si and NiSi has been reported as $6.09x10^{-2}$ atoms/Å^3 and $4.11x10^{-2}$ atoms/Å^3 respectively [18]. These correlate to the thickness of 188nm and 219nm for the Ni_2Si and NiSi film respectively. From the calculated silicide thicknesses, the silicidation rates were calculated to be 3.13nm/sec and 3.65nm/sec for doped silicon and polysilicon areas respectively. However, there was no trace of pure nickel left on the surface of both samples as shown by the RBS results. This gives rise to some ambiguity as to whether the silicidation actually took place throughout the entire 60sec anneal. If the silicidation was shorter than 60sec due to total consumption of available nickel metal, then the rates could be higher. There must be some presence of un-reacted nickel after the RTP process in order give total confidence into the rates obtained. Nonetheless, the RBS analysis did provide a confirmation of NiSi phase in the doped silicon area and Ni_2Si phase in the polysilicon area.

XRD analysis was also done on a sample taken from the undoped silicon region with RTP treatment at 500°C for 60sec. All un-reacted metals were removed via wet etch prior to the analysis. Refer to Fig. 2.4 for details.

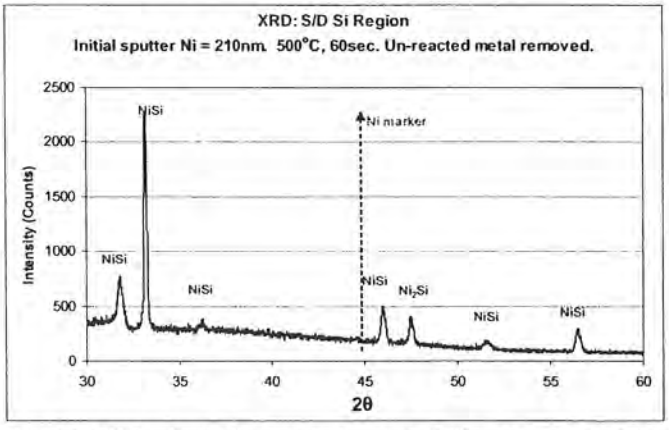

Fig. 2.3. XRD analysis of undoped silicon with RTP treatment at 500°C for 60sec. All un-reacted metals were etched off prior to analysis.

Result from the XRD analysis indeed confirmed the results found from the RBS analysis. There is clearly a predominant presence of NiSi phase in the sample with a trace presence of Ni_2Si.

Based on the results obtained from Rs measurements, RBS analysis, and XRD analysis, it can be concluded that the optimal RTP treatment condition for the formation of NiSi is at 500°C. The duration of the RTP treatment must be vary to accommodate for the desired silicide thickness.

B. Nickel Silicide NMOS Integration

The nickel silicide integration processes in Fig. 2.2 were carried out in conjunction with the normal NMOS device. To

ensure sufficient source of nickel during the silicidation process, a thick layer of nickel was deposited with thickness comparable to that of the oxide/polysilicon gate stack (360nm). A Ti capping layer was also used as shown in Fig. 2.2. Immediately after the RTP treatment, there was significant lift-off of the metal stack in the spacing between each die as well as the perimeter of the wafers. These were areas covered in field oxide. Therefore, it was not unusual for such lift-offs to occur especially with such thick metal stack. Microscopic inspection did not show any lift-off taken place within any device dies. The RTP treatment was done at 500°C for 60sec. After all un-reacted metals have been removed, visual inspection showed a difference in shading of areas where nickel silicides were formed. The surfaces of these areas seemed to be significantly more reflective than that of the control NMOS wafers. There were signs of "burn-in" visible near the alignment marks as well as the printed text areas. In addition, the thin polysilicon gate line seemed to be darker than usual. It was unclear whether the sidewall spacers were still presence through optical microscope inspection.

After the contact holes were etched, all wafers were cleaned using standard RCA cleaning process. An additional diluted HF dip was done to remove all oxide on the contact holes. However, significant changes were observed on the silicide S/D regions wafers after these two steps. As seen in Fig. 2.4, the contact holes on the S/D regions were completely removed. The silicide surfaces were also rougher and no longer had the highly reflective surface seen before.

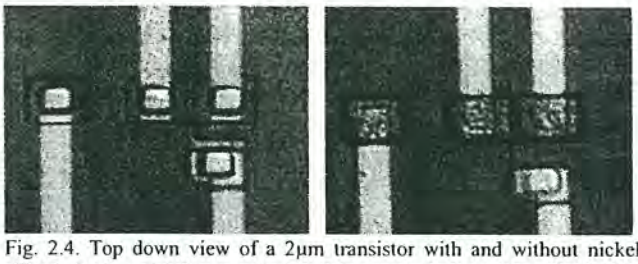

Fig. 2.4. Top down view of a 2μm transistor with and without nickel silicide (right and left respectively). The contact holes of the silicide S/D on the right image were completely removed, and the surfaces were significantly rougher with darker boundary. The contact hole on the polysilicon appeared to be in normal condition.

Due to time constraints, no further investigation was done to determine the cause of such deterioration. However, the root of the problem was suspected to be from the RCA cleaning process. Visual inspection was done prior to the RCA clean, and no such effect was evident. Notice the strict boundary of the surface deterioration ending precisely at the active area boundary. This suggested that the silicide surface in the active areas were reacting with some component of the RCA clean process. Such reaction might have caused a lift-off of some silicide in the area, and thereby removed all the contact. The dark shaded boundary around the active area was likely the result of TEOS field oxide rupture during the lift-off process.

Although the poly-silicide gate remained intact, it is probable that the oxide sidewall spacers no longer exist. No meaningful electrical results were obtained from any poly-silicide gate device. All results seem to suggest a shorting between some critical areas such as the source, drain, and/or poly-silicide gate. In addition, prior to the deposition of nickel metal, the gate oxide etch in BOE as well as the additional HF dip could have significantly undercut the gate oxide or removed the sidewall spacer all together. Such event could dramatically result in undesired electrical test results. The normal NMOS device wafers perform as expected.

There was one type of NMOS device found to function normally in both the silicide and non-silicide wafers. Meaningful electrical results were obtained from the 24/42μm aluminum gate with field oxide device. The field oxide, gate oxide, was 403 nm thick, and the aluminum metal gate was 660 nm (center) thick. Refer to Fig. 2.5 for a top-down view of the devices.

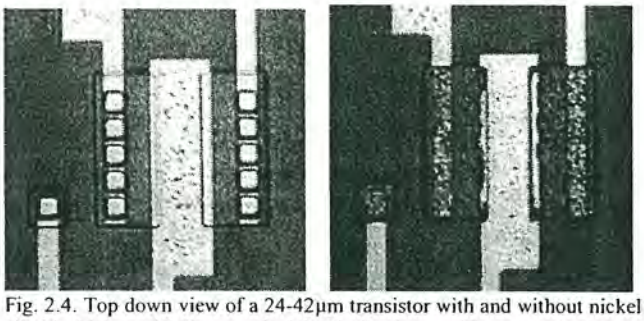

Fig. 2.4. Top down view of a 24-42μm transistor with and without nickel silicide (right and left respectively). Similar issue with contact holes and silicide lift-off in the active areas as describe in Fig. 2.4.

Direct comparisons between the silicide and non-silicide devices show that there are significant differences between the two types of device. The silicide S/D device shows significantly more gate voltage control and higher drain current. The drain currents increase by about 1.5 orders of magnitude relative to that of the normal NMOS. This suggests that there is indeed some silicide remaining in the S/D regions despite the contact holes lift-off. In term of threshold voltage (Vt) and transconductance (gm), the silicide device shows a leftward shift in the threshold voltage by about half the Vt value of the normal device. The Gm value of the silicide also doubles that of the normal device. Refer to Fig. 2.5 and 2.6 for details.

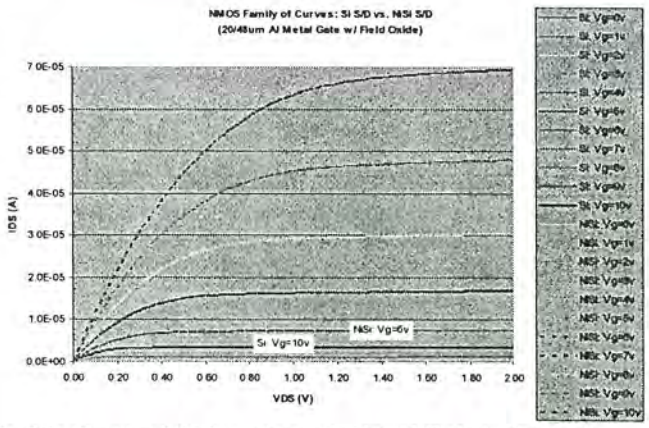

Fig. 2.5a. Overlay of silicide and non-silicide NMOS device family of curves. Significant increase in drain currents observe in the silicide S/D device.

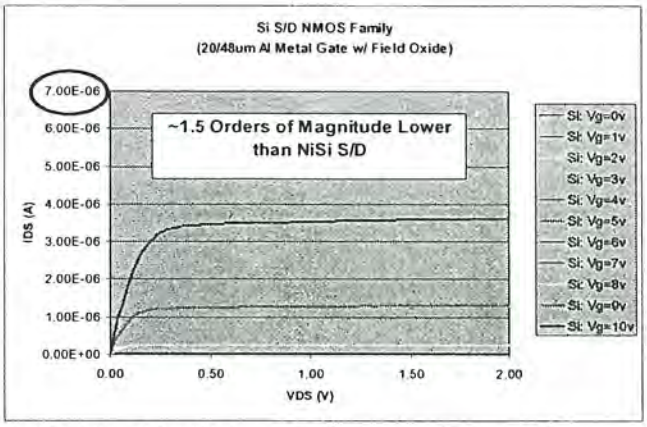

Fig.2.5b. Normal NMOS device family of curves. This is a 24/42μm NMOS device with filed oxide as gate dielectric and aluminum metal as gate.

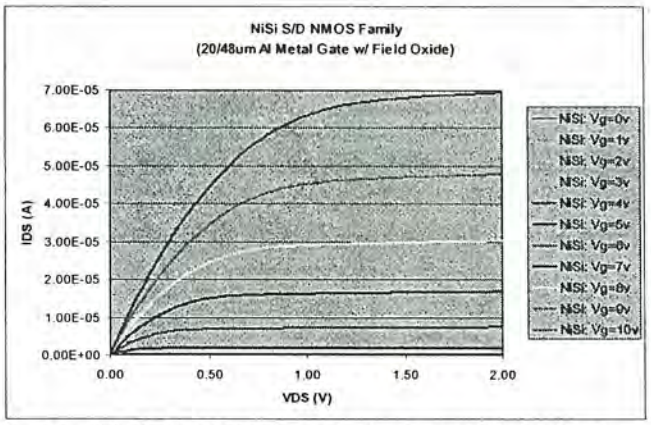

Fig. 2.5c. Silicide S/D NMOS device family of curves. This is a 24/42μm NMOS device with filed oxide as gate dielectric and aluminum metal as gate.

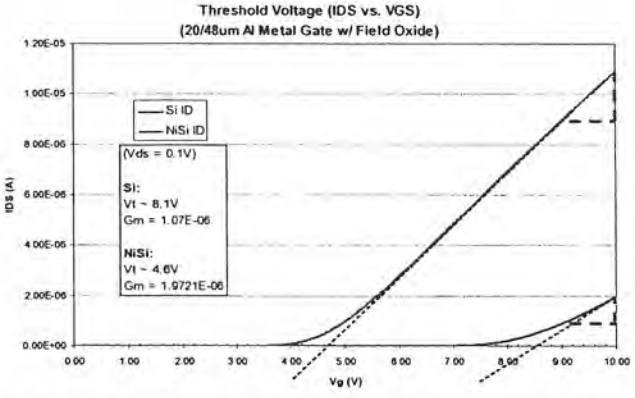

Fig. 2.6. IDS vs. VGS of silicide and non-silicide NMOS devices. With silicide S/D, the Vt was shifted leftward by half, and the Gm was doubled.

IV. CONCLUSION

A nickel silicide process yielding low sheet resistance NiSi has been successfully developed at RIT. The most optimal silicidation condition was established to be at 500°C yielding sheet resistance in the range 0.450 Ω/□ to 0.600 Ω/□. In addition, a nickel silicide integration process has been developed to incorporate NiSi into RIT device fabrication. Additional experiments are needed to validate the integration process and investigate the effect of subsequent RCA cleaning on exposed silicide surfaces. Electrical test results show significant improvement in drain current and greater gate voltage control for device with nickel silicide on source/drain regions. This corresponds to the doubling of the device transconductance value as well as shifting the threshold voltage leftward by about half the Vt of non-silicide device.

In order to qualify the results and process development of this project, further studies are needed in the improvement of the sidewall spacer process and determine the degree of lateral encroachment of silicide in the S/D regions. In addition, an investigation is needed to determine the specific cause of the lift-off issue found in the RCA cleaning process. Perhaps the subsequent RCA cleaning step can be eliminated altogether to avoid unnecessary complications.

V. ACKNOWLEDGMENTS

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