Characterization of Low Temperature Gate Dielectrics for Thin Film Transistors

G. Robert Mulfinger

Abstract— The goal of this investigation was to ascertain a viable low temperature gate dielectric for an emerging TFT fabrication process at RIT. Various candidates were investigated to find the best solution for a low temperature gate dielectric. Materials studied include low temperature oxide (LTO) using low pressure chemical vapor deposition (LPCVD), plasma enhanced chemical vapor deposition (PECVD) silicon nitride, and PECVD Tetra Ethyl Ortho Silicate (TEOS). Capacitors were fabricated with these materials, as well as a standard thermal oxide as a control. Wafers were examined both with and without anneals at 600°C in order to study bulk oxide and interface charge levels. Surface Charge Analysis (SCA) and C-V curves were generated in order to analyze and compare charge levels of the various treatment combinations.

***Index Terms*—C-V Analysis, Low-temperature dielectric, interface charge.**

I. Introduction

THE advancement of thin-film transistor (TFT) technologies is important for consumer applications such as LCDs (liquid crystal displays). With new improvements in thin-film semiconductor materials, products will realize considerable improvements in device performance. However, the substrate material that TFTs are built on imposes significant challenges in processing techniques and device performance. Unlike traditional crystalline Si substrates, substrates for TFT applications have strict thermal limitations. Specifically, low temperature restrictions make it difficult to deposit a high quality gate dielectric. In comparison to a thermally grown oxide, gate dielectrics deposited at lower temperatures exhibit decreased uniformity and increased charge levels. High charge levels shift the threshold voltages of devices greatly altering their functionality and performance. Thus, it is important to minimize charge levels and obtain repeatable C-V curves before fabricating transistors.

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II. Theory

C-V analysis involves studying the relationships between capacitance and voltage. It is important to study these relationships since they are directly related to the functionality of the MOS transistor. In a MOS transistor, the gate (either poly silicon or metal) acts as a dielectric between an applied gate voltage and the region between the source and drain. This actually acts as a capacitor. The C-V curve of a MOS capacitor is directly dependant on the applied bias. Depending on the bias, the device can either be in accumulation mode, depletion mode, or inversion mode. These characteristics from the C-V curves directly relate to the threshold voltage in a MOS transistor. The C-V curve provides valuable information because threshold voltage is one of the key components in the functionality of a MOS transistor.

Figure 1 shows the ideal C-V curve for a MOS capacitor on P-type silicon. The three regions of operation, accumulation, depletion and inversion can be clearly differentiated.

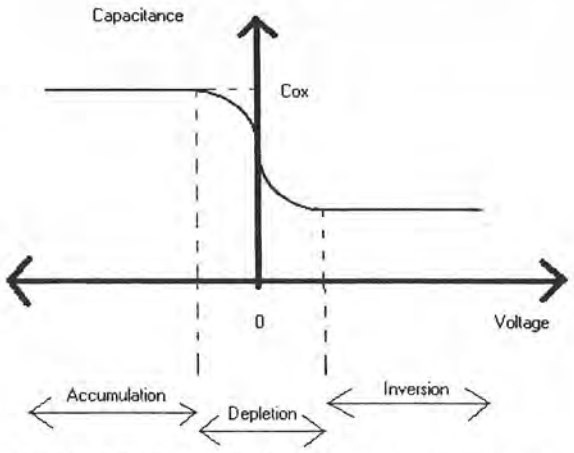

Figure 1: Ideal C-V curve for MOS capacitor on p-type silicon:

In accumulation a negative bias is applied to the metal. This negative bias repels electrons to the oxide/metal interface resulting in a negative charge in this region. Since the oxide acts as an insulator or dielectric, ideally no charge moves within it. As a result, holes accumulate at the surface of the semiconductor at the silicon/oxide interface.

In the depletion portion of the C-V characteristic, a positive bias is applied to the gate (metal). Since the oxide acts as a dielectric, inversion results in a negative charge that will accumulate at the surface of the silicon at the silicon/oxide interface. Even though the substrate is p-type, there are still excess electrons available to accumulate at the surface. While increasing the positive bias on the gate, more electrons are attracted to the surface of the silicon at the silicon/oxide interface. Inversion occurs when the minority carrier concentration exceeds that of the majority carrier concentration (for p-type silicon, electrons are minority carriers and holes are majority carriers.)

For n-type MOS capacitors, the physics remain the same except the gate biases and charge biases are reversed. The ideal C-V curve for an N-type MOS capacitor is shown in figure 2:

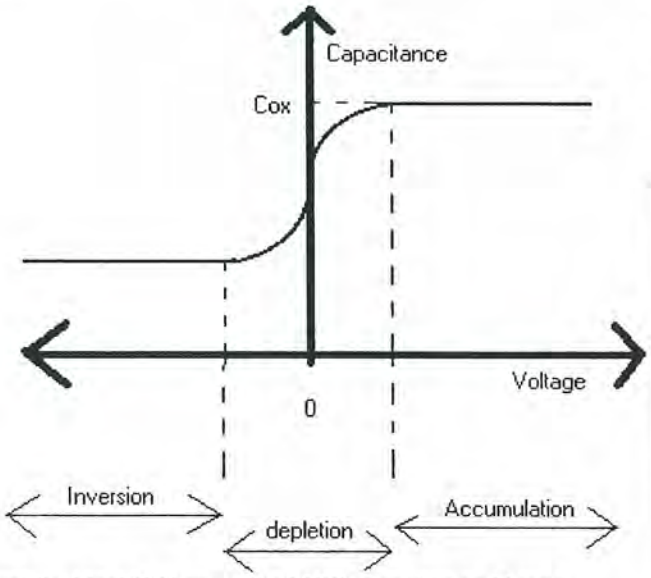

Figure 2: Ideal C-V curve for MOS capacitor on N-type silicon:

Since oxides deposited at low temperatures generally have more positive charge, the C-V curve is usually shifted to the left and the threshold voltage is decreased. This can be seen in the following equation:

$$Vt = Vt_{ideal} + \phi_{ms} - \frac{qNss}{C_{ox'}} \qquad (1)$$

In the expression, the quantity Nss is a lumped sum of oxide trap charge, fixed charge, mobile charge and interface trap charge. This value is the main response in the investigation used to compare the different oxide charge levels.

Two ways to obtain this charge value include using the SemiTest SCA (surface charge analyzer) or the Agilent 4182 C-V analysis tool. The SCA uses light pulses and induced charge to generate fluctuations in AC surface potential and a modulated depletion width at the silicon/oxide interface. When these values are measured, values such as oxide charge, surface concentration and density of interface traps can be determined. The C-V analysis tool plots capacitance as a function of voltage. It can then determine Vt, Vfb and calculate charge levels and surface concentration using the following equations at flat band:

$$V_{fb} = \phi_{ms} - \frac{Q_{ss}}{C_{ox'}}$$

$$Q_{ss} = qN_{ss} = qN_f + qN_{it}(\psi_s)$$

III. Experiment/Results

The experiment began with the comparison of some of the possible low temperature gate dielectrics that can be deposited in the SMFL at RIT. These included PECVD oxide, PECVD nitride, LTO and a standard thermal oxide as a reference. An overlay of these C-V curves can be seen in figure 3 below.

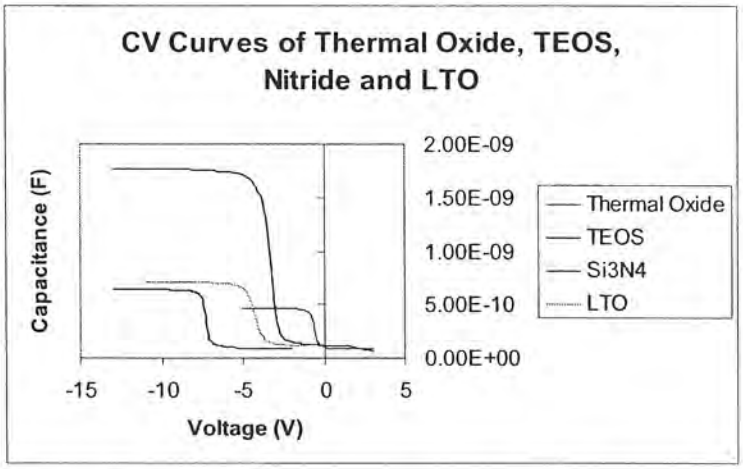

Figure 3: Preliminary C-V curves of various materials

As seen in the above plot, the thermal oxide shifted the least, meaning it has the least amount of positive net charge. The nitride, LTO and PECVD oxide follow in order of their amount of positive charge from least to greatest. It can also be noted that the oxide capacitance of the nitride is much higher than the other materials. This occurred because the thickness of the nitride was smaller and the relative permittivity of the nitride was larger than that of the other materials. (All capacitors tested were made with Al, had an area of 0.015cm^2 and were not annealed or sintered. Other than the deposition of the dielectric, all wafers were processed together under the same conditions for consistency.) A quantitative comparison can be seen below in table 1.

wafer	Xox	Cox(pF)	Vfb(V)	Vt(V)	Nss(/cm^2

	(A)				)
Thermal	502	469	-0.61	0.29	3.96E+10
LTO	550	711	-4.3	-3.5	1.47E+12
TEOS	477	647	-7.31	-6.54	3.03E+12
Nitride	315	1770	-2.96	-2.45	1.63E+12

Table 1: C-V measured values of initial data

In analyzing this data, it can be noted that the charge levels in the thermal oxide are approximately two orders of magnitude lower than the low temperature oxides. The LTO, TEOS and nitride were all in the same order of magnitude and resulted in fairly close values. After the initial comparison, DOE's were done in order to look more closely at nitride and TEOS. A short screening experiment was first set up to investigate the different existing programs for nitride deposition in the Applied Materials P5000 PECVD tool. Table 2 shows the nitride screening experiment that was done.

recipe	Anneal	dep time (s)	Tox (A)	Cox(pF)	Vfb(V)	Vt(V)	Nss(/cm^2)
Si3N4	Yes	4	320	591	-1.18	-0.776	1.19E+11
Si3N4	No	4	315	1770	-2.96	-2.45	1.63E+12
Low N	Yes	7.5	306	1020	-0.383	0.00505	1.33E+11
Low N	No	7.5	314	2030	-1.46	-1.01	6.19E+11
Low H	Yes	14	411	1160	-5.32	-4.76	2.20E+12
Low H	No	14	396	2050	-4.87	-4.27	3.49E+12

Table 2: Nitride Recipe Comparison

The Si_3N_4 recipe is a standard stoichiometric recipe for silicon nitride. The Low-N recipe is a silicon rich nitride which is generally used for low stress applications. (Since gate oxides are very thin, stress is not a concern typically taken into consideration.) Finally, the Low-H recipe is a nitrogen rich nitride. Historically TFT's have used nitrogen rich nitrides because of their electrical characteristics including lower leakage current and conductance values. These nitrides were used as gate dielectrics both with and without a 600°C anneal in H_2/N_2.

From the C-V data obtained, it was determined that the stoichiometric silicon nitride recipe actually resulted in the lowest charge levels. The anneals appeared to decrease the charge level by approximately one order of magnitude for each recipe. Despite having nearly twice the charge as the other recipes, the nitrogen rich recipe appeared to have the best electrical characteristics according to its index of refraction. Literature states that optimum electrical characteristics occur when the index of refraction of the nitride is between 1.85 and 2.0. The Rudolph ellipsometer was used to measure an index of refraction of 1.99 on the two nitrogen rich nitride wafers. The others wafers ranged from 2.25 to 2.5. Further investigation would be needed to better characterize the films and decrease charge. This investigation was not taken up due to non-uniformity problems and other laboratory concerns. Rather than furthering the initial investigation, a more thorough investigation in the PECVD oxide was conducted.

The initial investigation of the PECVD oxide was completed by looking at the standard program (A6-Karl_NLS). This consisted of three main steps:

Step 1: stabilize
-No RF power
-TEOS flows at 400sccm and O2 flows at 285 sccm until stable

Step 2: deposition
-RF power at 255w
-TEOS flows at 400sccm and O2 flows at 285 sccm

Step 3: lift recipe
-RF power at 50w
-O2 at 285 sccm flows until for 10s
-lifts off unreacted TEOS from the surface

These three process steps were done in different orders and with different gas flows to determine if the resulting films would have varying charge levels. The experimental design can be seen in the following table:

Wafer
(1) 30s stab. with TEOS and 02 flowing, dep, lift
(2) 0s stab. dep, lift
(3) 30s stab. In 02 only, dep, lift
(4) stab. In 02, 30s stab. In TEOS and 02, dep, lift
(5) 30s stab. In TEOS and O2, lift, dep, lift
(6) Lift, 30s stab. In O2, dep, lift
(7) Lift recipe, stab in O2, stab. In TEOS and 02, dep, lift
(8) 30s stab. with TEOS and 02 flowing, dep, lift

Table 3: PECVD oxide screening experimental setup

Capacitors were then made with each treatment combination and C-V characteristics were analyzed to compare charge levels. Results can be found in table 4.

Wafer	Tox (A)	Cox(pF)	Vfb(V)	Vt(V)	Nss(/cm^2)
1	477	577	-9.73	-9.02	3.03E+12

2	583	490	-8.35	-7.6	1.61E+12
3	488	575	-10.7	-10	2.46E+12
4	485	582	-10.6	-9.87	2.46E+12
5	338	682	-3.82	-4.25	1.08E+12
6	494	546	-6.88	-6.43	1.47E+12
7	490	578	-7.64	-7.19	1.74E+12
8	475	551	-9.38	-8.63	2.04E+12

Table 4: TEOS C-V data with alterations to the std. Recipe

From the C-V data, wafer 5 showed the least amount of charge. This treatment combination used a fixed 30 second stabilization in TEOS and O_2, followed by the lift recipe, the deposition, and then the lift recipe. This resulted in a significant decrease in charge compared to the standard, unaltered, TEOS recipe. This difference is best observed by looking at an overlay of the two C-V curves in figure 4.

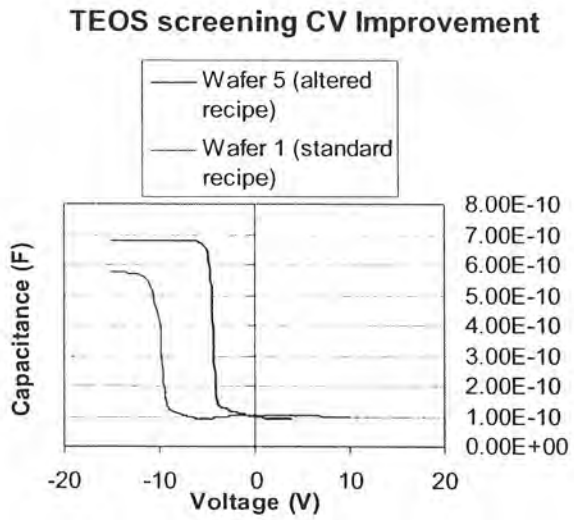

Figure 4: TEOS Screening Charge reduction

After completing the screening experiment and altering the standard PECVD oxide (TEOS) recipe, a subsequent DOE was conducted to further investigate charge reduction by means of a 600°C anneal in H_2/N_2 and 450°C sinter in H_2/N_2. PECVD oxide with the altered recipe was made into capacitors with no anneal and no sinter, anneal only, sinter only and anneal with sinter with replication. The following figure shows three of the four treatment combinations C-V curves.

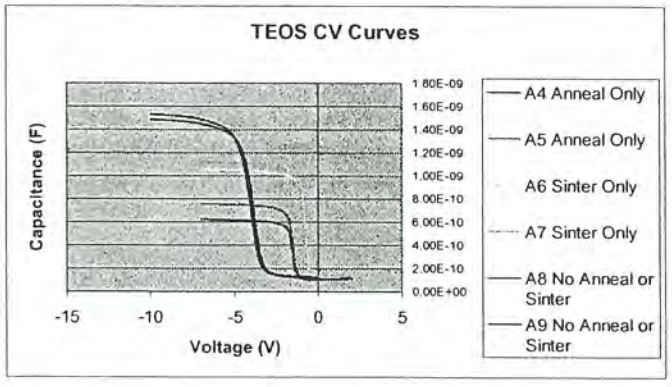

Figure 5: C-V curves for three treatment combinations

The data obtained shows that the sinter was the most significant factor in reducing positive charge from the dielectric. The anneal also decreased charge levels from the baseline data (wafers neither annealed or sintered). C-V curves collected on the wafers that were both annealed and sintered can be seen below in figure 6.

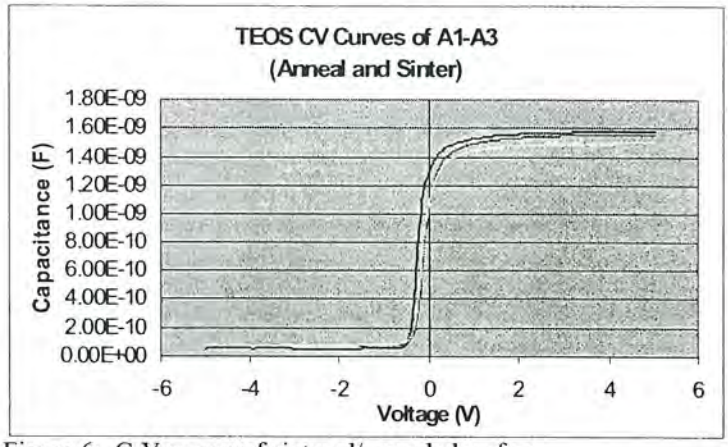

Figure 6: C-V curves of sintered/annealed wafers

A brief analysis of figure 6 suggests that the three wafers in the sinter/anneal treatment combination are n-type since all curves were swept the same way.. Wafers were taken into the lab and placed on a hot probe to verify that they were n-type. The quick test showed that the three wafers were n-type and the other wafers were p-type. (All wafers were taken out of a sealed box of p-type wafers. Serial numbers of each wafer were written down and each wafer was scribed directly out of the box to ensure they weren't confused with any other wafers throughout the process.) The mix up confounded the experiment due to the fact that the entire treatment combination was done on a different type of wafer. However the data still shows that with the sinter and anneal, C-V data is highly repeatable and shows a promising future for PMOS on low temperature PECVD oxide. Quantitative comparisons of the data can be seen in table 5.

Wafer	Tox (optical) (A)	Tox (electrical) (A)	Cox(pF)	Vfb(V)	Vt(V)	Nss(/cm^2)
A1: Anneal and Sinter	357	329	1580	-0.365	-0.838	-4.84E+10
A2: Anneal and Sinter	341	333	1560	-0.216	-0.744	-3.59E+10
A3: Anneal and Sinter	357	345	1500	-0.246	-0.776	-1.59E+10
A4: Anneal Only	353	831	623	-1.58	-0.777	2.09E+11
A5: Anneal Only	333	684	757	-1.57	-0.781	2.50E+11
A6: Sinter Only	332	490	1060	-0.801	-0.0971	5.56E+09
A7: Sinter Only	360	464	1120	-0.869	-0.169	3.69E+10
A8: No Sinter or Anneal	314	338	1530	-3.91	-3.3	2.00E+12
A9: No Sinter or Anneal	336	349	1460	-3.82	-3.18	1.88E+12

Table 5: TEOS data

The first two columns show a comparison of optical thickness measurements and electrically measured thickness. The optically measured thickness was measured with the

Spectramap. The electrically measured thickness was measured using the Cox equation below:

$$Cox = \frac{\varepsilon A}{Tox} \quad (2)$$

The area was entered in to the tool for each measurement, and the permittivity was assumed to be equal to a thermally grown oxide (3.9). Most of the values were in close range, showing that the permittivity was comparable to that of a thermally grown oxide. In certain instances the electrically calculated oxide thickness was much further off. This was most likely due to leakage current in the Cox measurement. in these instances, the Cox value appeared lower than it should have been. Also, when the measurements were taken, the conductance appeared to by higher suggesting that there was some leakage current through the oxide.

As previously noted, the sinter had the most significant impact on charge reduction in the oxide. In the IC fabrication process sintering is known to reduce interface trap charge. This suggests that the majority of the charge in the PECVD oxide is most likely due to interface traps caused by dangling bonds at the silicon/oxide interface. The remaining charges could be characterized as mobile or fixed and could be quantified using a temperature bias stress test in future work.

A comparison of SCA and C-V data was attempted in some of the treatment combinations. Unfortunately the SCA tool failed to measure most of the wafers in the experiment. Once the charge level reached a certain point in the oxide, the SCA could not induce enough charge to obtain accurate measurements. For this reason only data on annealed wafers could be obtained.

SCA data

wafer	Nsc_inv	Qox_inv	Dito_inv
A1: Anneal pre-sinter	6.20E+13	3.66E+11	3.98E+11
A3: Anneal pre-sinter	2.93E+13	1.50E+10	1.76E+12
A4: Anneal Only	6.20E+13	1.99E+11	2.76E+11
A5: Anneal Only	7.41E+13	1.92E+11	2.77E+11

Table 6: SCA data for annealed wafers

CV data

wafer	Nsc (/cm^2)	Nss
A1: Anneal and Sinter	7.40E+13	-3.79E+10
A3: Anneal and Sinter	1.53E+14	-1.09E+10
A4: Anneal Only	4.04E+14	4.56E+11
A5: Anneal Only	4.69E+14	4.75E+11

Table 7: C-V data

Some of the comparisons between tables 6 and 7 are reasonably close. Surface concentration of Al and charge levels of the 4 wafers are on the same order of magnitude. The Density of interface traps is also very high on the SCA data. This is in agreement with the assumption that the majority of the oxide charge was from interface trap charges. Of the two measurement techniques, the most accurate was the C-V analysis. The C-V data is not only considered to be a more direct measurement, but results in more meaningful data because it is obtained after the fabrication process. The SCA data is obtained before metal deposition and sinter. Subsequent process steps could alter the behavior of the film after the SCA measurement.

IV. CONCLUSION

Capacitors were fabricated using PECVD nitride, PECVD oxide, LPCVD LTO and thermal oxide dielectrics for charge comparison. The experimental design showed an improved TEOS deposition recipe for lower charge levels. Post-deposition annealing and sintering resulted in reduced charge levels and lower leakage. Sintering showed the highest significance in reducing interface charge. Further analysis is required for LTO and nitride films.

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