Electromigration Testing at RIT: Thermal Test Development

Lance W. Barron

Abstract— **An electromigration (EM) test mask was designed to utilize both standard ASTM and Standard Wafer-level Electromigration Accelerated Test Structures (SWEAT) four-terminal EM test structures of varying line-widths. The mask was used to pattern 4" test wafers consisting of 300 nm of sputtered aluminum-1% silicon on a thermal SiO2 layer. A custom thermal setup was developed for a Micromanipulator 6000 manual probe station. A new 4" brass chuck was machined to include cooling channels, wafer vacuum, and a thermocouple monitoring system. A resistive ring heater was bonded to the chuck and was controlled via a process temperature controller. Extensive electrical test of interconnect structures was necessary to generate EM lifetime data for the alloy film. Multiple measurements on a given type of test structure were used to generate acceptable sample sizes for mean-time-fail (MTF) statistics. Test data for both ASTM and SWEAT structures demonstrated a lognormal distribution for cumulative failure with a decrease in mean fail time for increased test temperatures. The activation energy for Al-Si at RIT was approximately 0.5 eV for 2.7 um lines of both types of test structures. A test station and methodology are now in place for future EM lifetime studies to be completed at RIT.**

Index Terms— **Electromigration, MTF, Thermal Probe Stations, Interconnect Failure**

I. Introduction

Yield and device reliability have been key parameters for the success of device fabrication since the creation of the semiconductor industry. Yield analysis is completed in the fab through the use of metrology techniques to look for defects and process errors prior to the packaging of the device. Reliability is a much more difficult issue to quantify. Reliability issues arise either during internal device testing at or in the field. As a result, considerable work has gone into predicting the lifetime of devices through the modeling of known failure modes and through accelerated life testing. One such failure mechanism is electromigration. Electromigration is the movement of metal ions as a response to an electric field during current flow in a metal interconnects line [1]. It results in hillocking, line shorting, line failure, and diffusion barrier breakdown among metal lines in semiconductor interconnects.

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As the industry scales further along the ITRS Semiconductor roadmap, increased metallization layers, packing density, and elevated current density will make electromigration an increasingly significant failure mechanism.

The primary project goal to develop the equipment and methodology necessary to measure electromigration at RIT. This included the test mask design, wafer fabrication, probe station construction, and electrical test methodology. An existing Micromanipulator 6000 4" manual probe station was used as a platform to integrate a thermal chuck system with a temperature range of 20 – 250°C. A g-line lithography mask was generated containing a variety of ASTM and SWEAT test structures with varying line widths. This was then used to fabricate simple test wafers for mean-failure analysis and activation energy extraction for both types of test structures.

II. Electromigration Theory

Electromigration can simply be defined as the movement of ion in response to the electric field generated by current in a metal line. This phenomenon can be described via two different mechanisms in metals or heavily doped semiconductors as shown in Fig. 1. [2] Due to the positive charge on the metal ion, it is attracted towards the negative terminal of the electric field in the line, thus would move towards the cathode. However, as electrons are pulled towards the anode, they are scattered off imperfections in the lattices and can impinge upon the metal ion. The momentum transfer from this electron "wind" would force the ion towards the anode. Since the electron momentum transfer dominates over the direct force on the ion, there tends to be a buildup of ions at the anode and voiding near the cathode of the metal line.

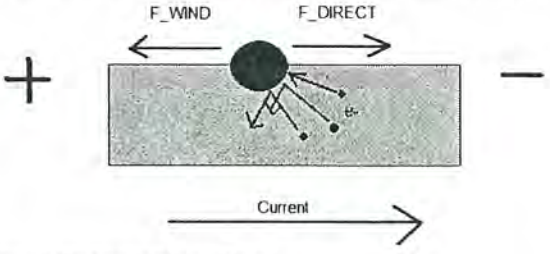

Figure 1 Electromigration diagram.

While there has never been a complete model explaining the electromigration phenomena, there is a semi-empirical equation for the mean time-to-fail (MTF) that was first described by Black, taking a form similar to an Arrhenius relationship [3]:

(1) $$MTF = AJ^{-n}e^{\frac{E_a}{kT}}$$

A is a material and geometry dependant constant, J is the current density, n is the current exponent factor, and Ea is the activation energy. The activation energy for Al-1% Si, a common alloy in the semiconductor industry, typically ranges between 0.4 and 0.7 eV. Note that there is an exponential current dependence that cannot be explained by an Arrhenius relationship and is still a source of significant debate as it can range between 1 and 14.

To extract the activation energy for a given material, a series of MTF data points are taken for a fixed current density at several different temperatures. The log of mean fail time is plotted against one over the product of Planck's constant multiplied by the real line temperature. Note that any Joule heating of the metal lines must be accounted for in this calculation. This should produce a linear data trend, the slope of which is the activation energy of the metal line.

III. Experimental Plan

Discussion of the experimental plan is separated into three sections; the design of the thermal chuck, the design of the test mask, and the fabrication process for the test wafers.

A. Thermal Chuck Design

RIT currently has a variety of probe setups with varying levels of automation. For the high current, time based measurements required for EM testing, it was determined that a manual probe station best suited the project needs. RIT possessed a Micromanipulator 6000 station with a 4" chuck, good xy stage control, good optics, and good illumination. Unfortunately the existing chuck used a polycarbonate backing material, thus was not suitable for temperature based testing. It was decided that a new chuck would be fabricate to alleviate this concern.

The new chuck was to be machined to the same height and wafer dimensions of the existing thermal chuck, but with all-brass construction. It was decided to form the chuck out of three pieces, two 4" brass rounds and a hollow piece of tubular brass to be used to set the chuck height and allow interface with the probe station's xy stage. The top plate was machined to have top-surface vacuum grooves to hold the wafer under test. A second groove was milled in the top plate to allow for the insertion of a thermocouple directly below the wafer for temperature monitoring. The bottom plate was milled to contain water channels and the necessary fittings to attach the chuck to a chiller system. The chiller system could be water, air, or glycol, each allowing for a different operating temperature range. The three pieces were then brazed together to form the chuck, shown if Fig. 2.

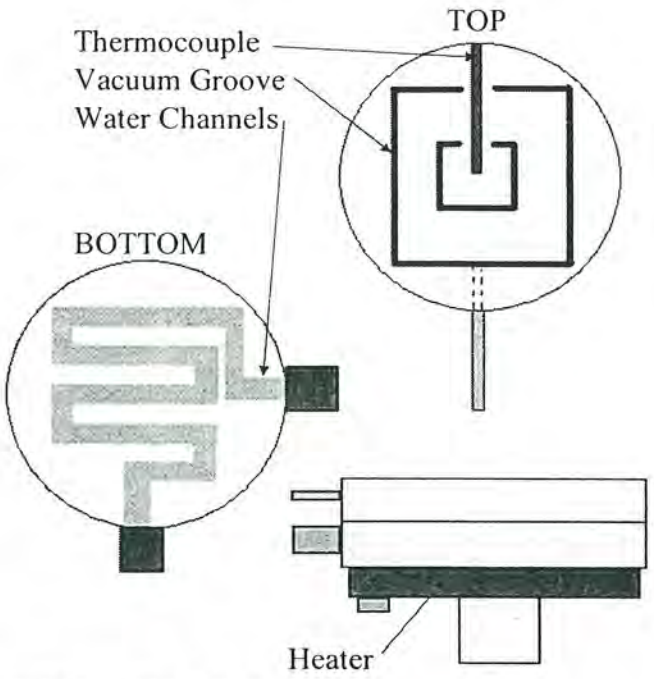

Figure 2: Thermal Chuck Design

A resistive ring heater specifically chosen in materials and power density was bonded to the underside of the brass chuck. The bonding agent was silica based, thermally conductive, electrically insulating, cement manufactured by Omega. Special thanks Pat Warner for his assistance in metal fabrication throughout this project.

To control the heating of the chuck, a process controller was purchased from Omega. It contained two 120Vac 5A relays to power the 300W heater, and was interfaced to a thermocouple directly mounted on the chuck surface. The user simply enters a desired temperature and the process controller will bring the chuck to the set point in 15 to 30 minutes. TCR measurements of metal lines demonstrated excellent linearity in resistance as a function of temperature, indication stable temperature control.

B. Electromigration Testmask Design

The goal of the mask design was to provide a series of test structures for both ASTM and SWEAT structures. ASTM structures as described by ASTM F1259 are simply 800 um long metal lines. One is sketched in Fig. 3.

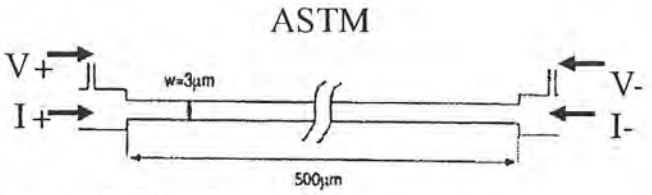

Figure 3: ASTM Schematic [4]

It is a four terminal structure which forces current along a metal line. Voltage is then measured along the metal line and

is charted as a function of time. When voltage across the line drops to zero, the current flowing in the line has caused a line failure. ASTM test structures are generally tested at current densities of 1MA/cm^2, and line failures take a number of hours or days. They were primarily designed for package level electrical test.

SWEAT structures are design for wafer level testing. They utilize much higher current densities, 15-20MA/cm^2, causing fail times that are minutes long, not hours.

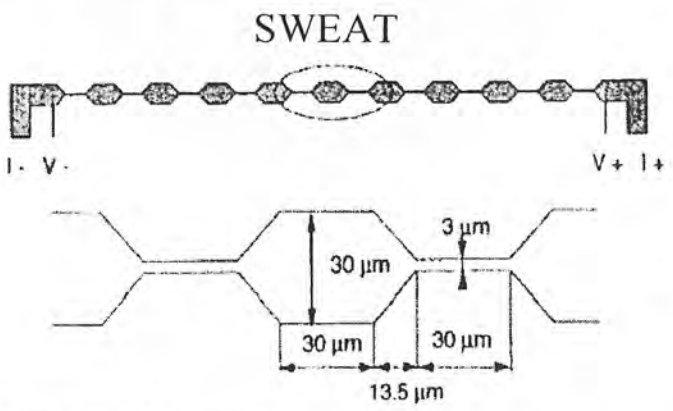

Figure 4: SWEAT Schematic [3]

The SWEAT structure alternates narrow and large line segments to cause current crowding and quick failure times. It is a four terminal structure that is tested in the same manner as an ASTM feature.

The test mask contains three main segments. Each segment contains a row-column array with each column containing a different line width. Each column contains 30 test lines, thus there are 270 test lines of each type per wafer with 9 die. The die size is 20 x 20 mm, and the mask was fabricated using a MEBES writing system in-house. The first segment contains ASTM structures with line widths from 2 um to 20 um. The second and third segments contain different types of SWEAT structures, one with tapered wide line segments as in Fig. 4, and one with rectangular line segments. The SWEAT structures range from 2 um to 10 um in width for the narrow portions of the lines. All lines on the mask are 800 um long. Also included on the mask are 5 terminal Van der Pauw structures for resistivity and line length measurement. No alignment structures were included for multiple level structures.

C. *Test Wafer Process*

The test wafers were designed for quick fabrication, reliable feature sizes, and large numbers of test sites per wafer. The design called for single-level metal lines fabricated on an insulated substrate, SiO2 in this case. The insulating substrate allows for better estimation of the Joule heating in each metal line. As the smallest line segments were 2 um in width, g-line lithography was deemed sufficient for patterning. Additionally, wet etching was employed for the aluminum in response to difficulties with the plasma etch tool. The processing sequence was as follows:

1. Scribe wafers
2. RCA wafer clean
3. 500 nm wet thermal oxide in Bruce furnace
4. Measure oxide thickness
5. Sputter 300 nm of Al-Si via DC magnetron CVC601
6. Measure thickness and resistivity of aluminum deposition
7. Coat Shipley 812 resist on wafers
8. Pattern via GCA g-line stepper
9. Develop in CD-26
10. Wet etch aluminum pattern
11. Strip off resist in O2 plasma asher
12. Sinter wafers in forming gas at 450°C for 30 min.

Wafers were left at each critical process step to accommodate unforeseen processing problems.

IV. Fabrication Results

A. *Finished Thermal Chuck*

All machining, brazing, and assembly was done locally in Rochester at RIT or local shops. Total cost of the entire thermal test setup was ca. $550 dollars, $400 of which was for the temperature controller. In comparison, a commercial chuck system for this application costs ca. $20,000.

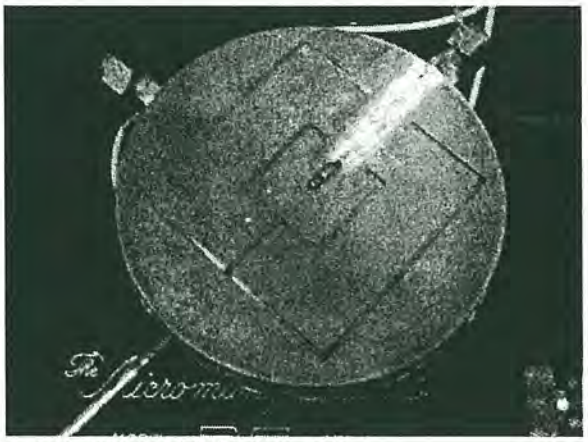

Figure 5: Top Surface of Finished Chuck

Figure 6: Profile View of Finished Thermal Chuck

Figs. 5 and 6 are views of the completed thermal chuck. The top surface contains the vacuum channels and the mounted thermocouple. Also pictures are the fittings for the connection of the chuck to a chiller assembly. The side view details both the brazing and the bonded resistive heater. Fig. 7 shows the finished chuck installed in the Micromanipulator probe station.

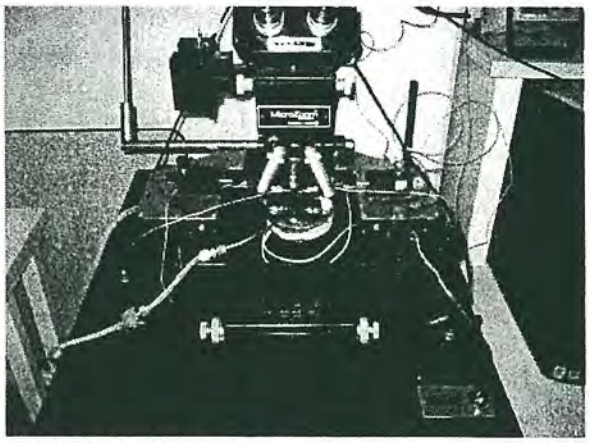

Figure 7: Completed Probe station

The completed test station allows the same xy stage control as the pre-existing chuck. The temperature and vacuum control takes up a minimum of space, and the new chuck can completely replace the brass/polycarbonate chuck assembly.

B. Test Wafers

Fabrication commenced with 12 4" wafers. The wafers were p-type epitaxial wafers of unknown quality, as the electrical characteristics of the wafers were not important for EM test wafers. Two wafers were brought to completion, one being shown in Fig. 8 below.

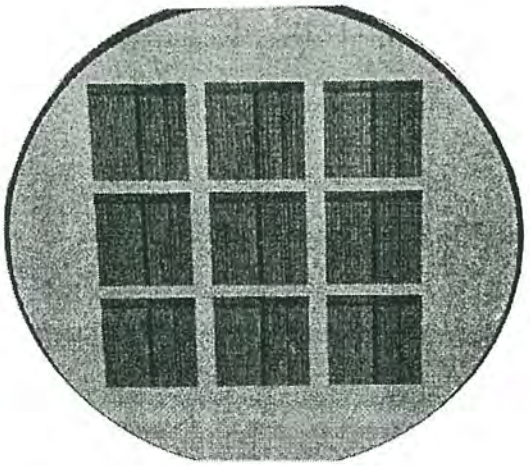

Figure 8: Completed Test Wafer

The final oxide thickness was 500 nm measured optically, and the average aluminum film thickness was 300.7 nm across the wafer surface. The measured resistivity post-sinter was 3.21 Ω-cm, and the measured temperature coefficient of resistivity (TCR) was 0.00344 Ω/K.

V. Electrical Test

A. Test Methodology

It was determined to test at least 10 individual lines for each MTF data point. 20 lines were tested for ASTM structures, and 10 were tested for SWEAT structures. To generate reasonable failure times at achievable absolute current levels, it was chosen to test 2.7 um line widths for both SWEAT and ASTM structures. It was experimentally determined for the ASTM structures that a current of 135 mA cause MTF time on the order of 5-10 minutes for room temperature testing. As a result, all testing was completed at this current level, corresponding to a current density of 17 MA/cm^2. This was well within the wafer level current density range for EM testing. MTF statistics were generated for both ASTM and SWEAT structures at temperatures of 22°C, 75°C, and 150°C for activation energy determination.

B. Electrical Test Setup

To conserve time, it was determined to test the ASTM and SWEAT structures using only 2 terminals. The test configuration for this is shown in Fig. 9.

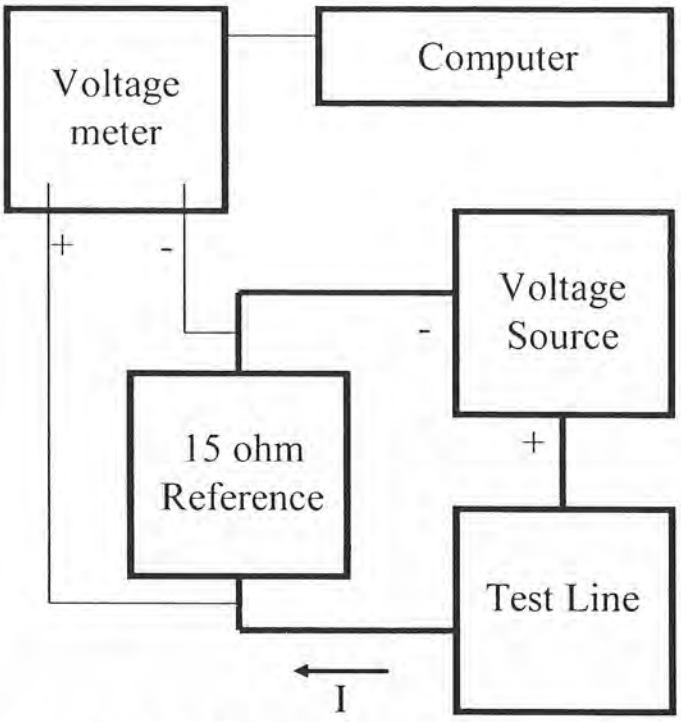

Fig 9: Electrical Test Block Diagram

A voltage source was used to drive a series circuit containing the wafer-level test line and an off-chip 15 Ω resistor. Note that a current limited power supply was desired for testing, but not available at the time. As a result, resistance changes in the test line under current load result in a lower actual current density over the course of the test. A 34401a Agilent multimeter was used to measure the voltage across the reference resistor. This multimeter was interfaced with a PC to sample the voltage level each second. When the voltage across the resistor drops to zero, that time is taken as the fail time. 10 successive measurements constituted one MTF data point. Some other electromigration studies have examined the resistance ratio of the test line, but this requires a 4-terminal configuration. As a result, MTF was the only response variable for this study.

C. *Joule Heating*

The high current densities present in the narrow metal lines causes significant Joule, or resistive heating to occur [5]. Thus changing current densities invariably change the actual temperature of the metal line, rendering a full factorial design un-attainable without a highly controlled environmental chamber. Joule heating in metal lines on an insulating substrate can be accounted for by [5]:

$$(2) \qquad T_{line} = T_{substrate} + \frac{J^2 \rho_0 (1 + \beta T_{substrate})}{(K_{ieff} / t_i t_m) - J^2 \rho_0 \beta}$$

Where T_{line} is the actual temperature in the line, $T_{substrate}$ is the substrate temperature, ρ_0 the resistivity of the material, β the temperature coefficient of resistivity, J the current density, t_i the insulator thickness, tm the metal line thickness, and K_{ieff} the effective thermal conductivity given by [6]:

$$(3) \qquad K_{ieff} = K_i (1 + 0.88 \frac{t_i}{W})$$

Where K_i is the bulk thermal conductivity and W is the width of the metal line. The effect of Joule heating is demonstrated in Fig. 10.

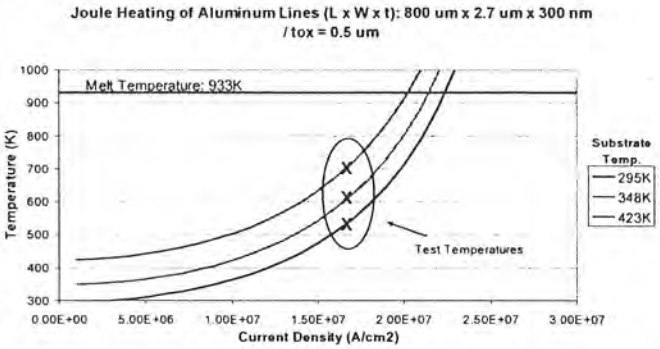

Figure 10: Joule Heating Simulation

Fig. 10 shows that while the ambient temperature for the first test series is room temperature, the actual line temperature was over 500K. The three curves represent room temperature, 75°C, and 150°C respectively. Note that all substrate temperatures generated line temperatures below the melting temperature of the aluminum at the experimental current density.

D. *Mean-Time-to-Fail Results*

The ASTM results shown in Fig. 11 clearly demonstrate the lognormal nature of electromigration. This is evident from the roughly linear trends in the MTF data when plotted on a lognormal cumulative probability plot.

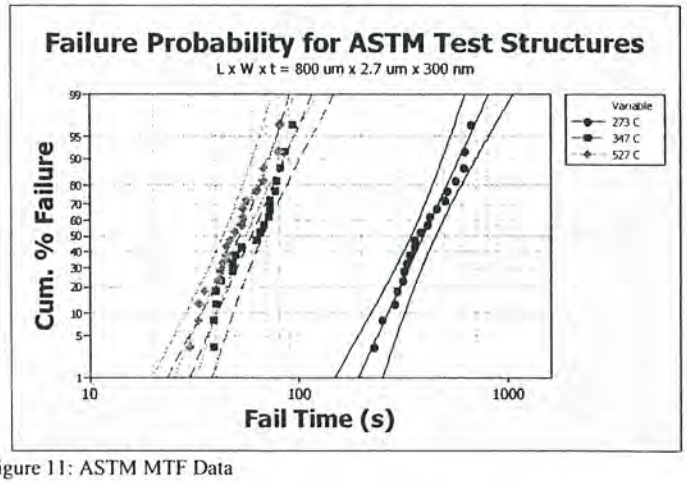

Figure 11: ASTM MTF Data

All three temperatures follow the lognormal trend. As was expected, increased line temperatures generated drastically shorter MTF. Unfortunately the 75°C and 150°C tests partially overlap. This was most likely caused by observed changes in line resistance early in the current loading. This

was most significant at elevated temperatures, thus the highest temperature test potentially was stressed by a measurably lower current density. This problem could have been alleviated by obtaining a current limited power supply.

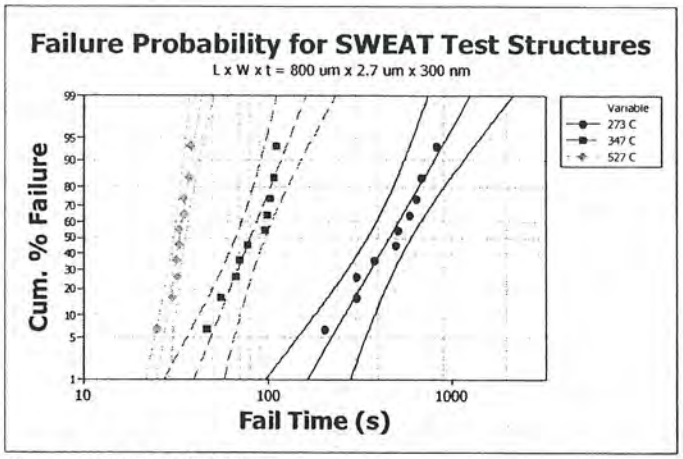

Figure 12: SWEAT MTF Data

The SWEAT data shown in Fig. 12 also exhibits a lognormal distribution, but without the current density problems associated with the ASTM structures at high temperatures under this accelerated current loading. There is clear delineation between the three different temperature set points. This suggested that the SWEAT structure indeed is a more reliable for fast, wafer-level testing.

The data contained in Figs. 11 and 12 were used to extract the activation energy for electromigration per Black's equation. The results are plotted in Fig. 13.

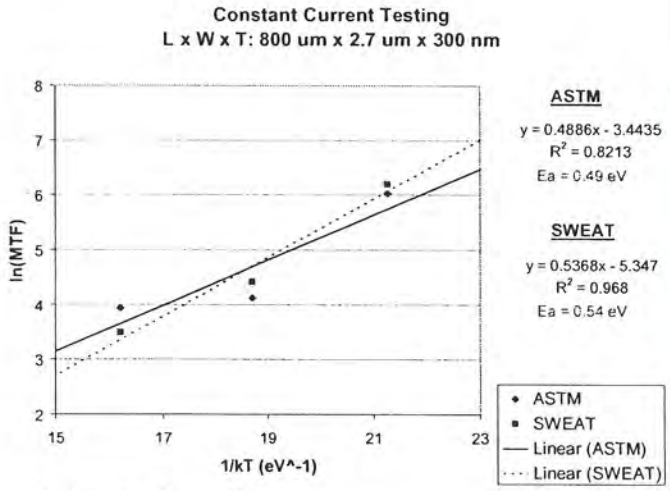

Figure 13: Activation Energy Plot

Both ASTM and SWEAT structures yield an activation energy of approximately 0.5 eV. This is within the previously measured range for Al-Si cited in literature. It is important to note that the well delineated MTF data points obtained for SWEAT structures at the three different temperatures generated a more reliable trend line than the ASTM data.

VI. Failure Analysis

Figs. 14 and 15 are microscope images of fabricated test lines. In each image, the line on the left was tested, and the line to the right was not tested.

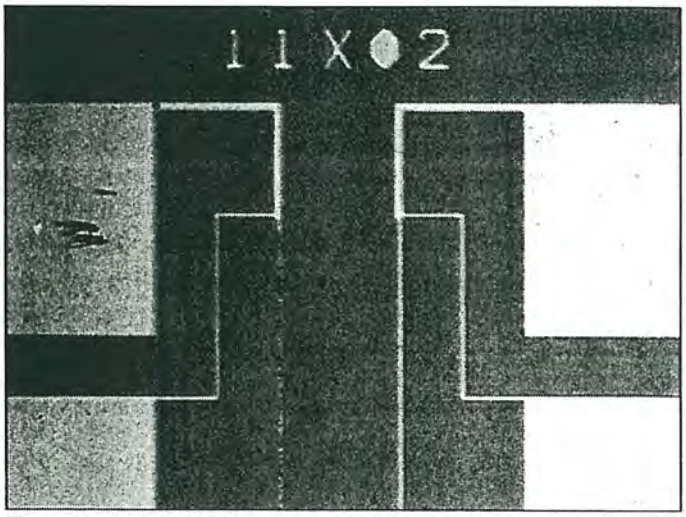

Figure 14: ASTM Optical Inspection

The tested line clearly looks blackened in comparison to the untested line. The discoloration was consistent across the entire line length. The discoloration is a clear indicator of potential voiding in the line.

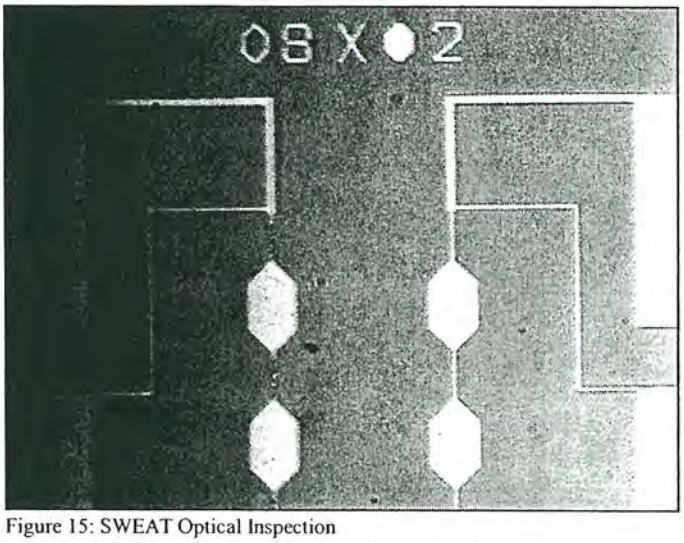

Figure 15: SWEAT Optical Inspection

Again, the tested line is significantly discolored. Note that the discoloration only occurs in the narrow line segments, indicating that the failure mechanism is dependant on current density.

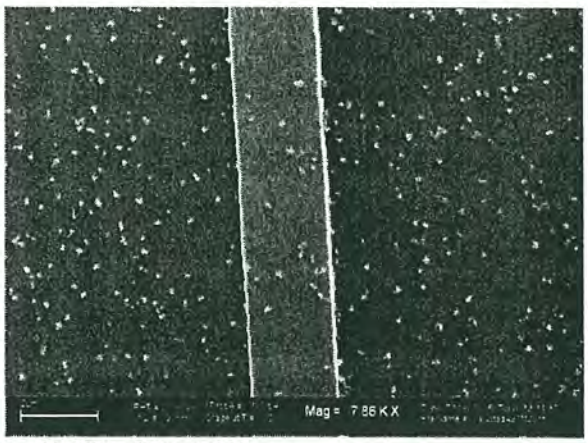

Figure 16: SEM of Untested Line

The SEM image in Fig. 16 shows an untested line. The edge profile is smooth and the surface is relatively untextured. The small particles in the image are simply residue from the wet aluminum etch process. Fig. 17 shows below showns an adjacent line that experienced the accelerated current load.

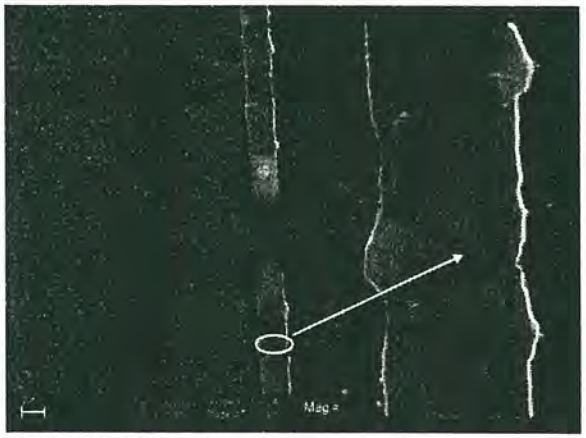

Figure 17: SEM of Tested Line

The SEM image clearly shows voiding as the dominant failure mechanism. It appears that as the viod grew, the surrounding line segment was energetically removed. The inset to Fig. 17 highlights an additional void that has partially severed the line. Note that the line edge is no longer smooth, showing nodules that suggest significant movement of metal atoms in the metal line. This was consistent for both ASTM and SWEAT structures.

VII. Conclusions

A basic methodology for electromigration testing has been developed at RIT. A thermal chuck system was designed, fabricated, and integrated into an existing test station. The thermal chuck was shown to control heat levels at the wafer reliably up to 150°C with potential to operate at temperatures exceeding 250°C. A custom electromigration test mask was designed with a variety of different test features. Wafers were then fabricated to allow for the examination of the failure performance of sputter-deposited Al-Si. Both ASTM and SWEAT structures were shown to follow lognormal failure behavior with activation energies of approximately 0.5 eV. The completed work provides the basis for future electromigration work at RIT.

VIII. Acknowledgments

This work could not have been completed without the support of many people at the Rochester Institute of Technology. Special thanks to Dr. S. Kurinec, Dr. S. Rommel, and Dr. K. Hirschman for their guidance and material support of the project. Thanks to fellow students A. James, D. Jaeger, and most importantly P. Warner, without whom this project would not have been possible. Additional thanks to the staff of the Semiconductor and Microsystems Fabrication Laboratory for technical assistance and equipment support.

References

[1] E. Artz, and W.D. Nix, 1991, J. Mater. Res., 6 (4), 731.

[2] O. Aubel, W. Hasse, M. Hommel, "Highly Accelerated Electromigration Lifetime Test (HALT) of Copper," IEEE Transactions on Device and Materials Reliability, v. 3, n. 4, pp. 213-218, Dec. 2003.

[3] F. Giroux, C. Gounelle, P. Mortini, G. Ghibaudo, "Wafer level electromigration tests in NIST and SWEAT structures," IEEE Conference on Microelectronic Test Structures, v. 8, pp. 229-233, 1995.

[4] T. Nogami, T. Nemoto, N. Nakano, Y. Kaneko, "The electromigration lifetime determined from the minimum time to failure in an 1 acceleration test," Semiconductor Science & Technology, v. 10, pp. 391-394, 1995.

[5] W. Wu, J.S. Yuan, S.H. Kang, A.S. Oates, "Electromigration subjected to Joule heating under pulsed DC stress," Solid State Electronics, v. 45, pp. 2051-2056, 2001

Lance W. Barron (M'76–SM'81–F'87) , born in Syracuse, NY in 1983, completed his B.S. in Microelectronic Engineering at the Rochester Institute of Technology in May 2005. He completed co-op assignments with Texas Instruments in Dallas, TX as a photolithography process engineer and as a MEMS process engineer. He is currently completing his master's degree in Materials Science & Engineering at RIT with the support of a research grant from Texas Instruments. He will be continuing his career at Texas Instruments in DLP Technology Development in September 2005.