Field Induced Band-to-Band Tunneling Effect Transistor (FIBTET)

David Pawlik, *Student Member IEEE*

Abstract— **A field Induced Band to Band Tunneling Effect Transistor was designed, fabricated and tested. The devices are to take the shape of finFETs and plainer devices which will employ mesa isolation technology. Degenerate dopings were achieved through the use of proximity diffusion in a rapid thermal processing tool. Final results include design parameters, fabrication parameters, fabrication techniques, SEM Images, electrical test results & analysis, and areas of continuing work.**

Index Terms— **FIBTET, Negative Differential Resistance (NDR), Peak-to-Valley Ratio (PVCR), Tunneling.**

I. Introduction

CONVENTIONAL CMOS technology is approaching fundamental limits. As a result new devices are being researched as replacements. For years it has been accepted that band-to-band tunneling devices have extremely high switching speeds, lower leakage currents, lower power consumptions, and better scalability. As an added benefit, the I-V characteristic contains a characteristic negative differential resistance (NDR). This characteristic can be employed as a load element in a latch or multi-valued logic circuit.

The ability to move away from a binary counting system and into a ternary, quaternary or even higher system has obvious advantages in computing. The best initial target niche is memory.

However, most research advances have been made in tunneling diodes. Furthermore, reasonable Peak to Valley Ratio's (PVCR) have been mainly achieved in III-V semiconductors, or with MBE grown Si/SiGe resonant interband tunnel diodes. These technologies, which do show significant promise for integration with CMOS, are nonetheless two-terminal structures.

Additionally, diodes do not have any power gain. However, a band-to-band tunneling transistor device that exhibits NDR would have the power gain needed for an all tunneling transistor circuitry architecture. The proposed device, the FIBTET, is structured the same as a finFET except for degenerately doped source, drain, and body regions. It has been shown the I_{ds}-V_{ds} and I_{ds}-V_{gs} characteristics exhibit NDR.

This work is part of the senior design project requirement for a B.S. degree in Microelectronic Engineering at the Rochester Institute of Technology (RIT). The results of this project were presented at the 23rd Annual Microelectronic Engineering Conference on May 10, 2005 at RIT in Rochester, NY.

D. Pawlik is with the Microelectronic Engineering department at the Rochester Institute of Technology in Rochester, NY.

II. Theory of Operation

A. Device Structure

The FIBTET is structured similar to a finFET (See Diagram below).

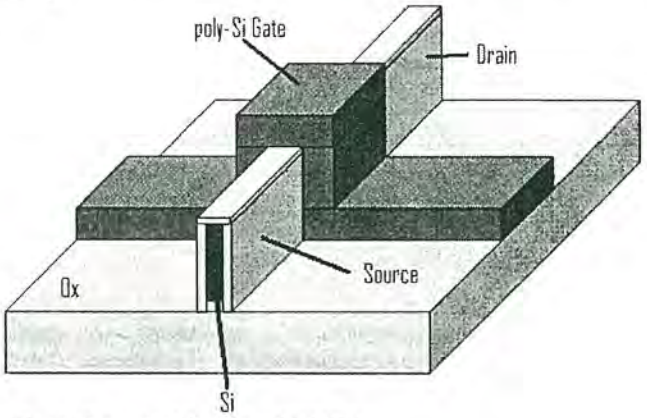

Fig. 1: Conceptual Drawing of FIBTET

The fin is made of crystalline silicon that is placed on top of an isolative oxide. The fin's height should be about twice that of its width. The gate is poly-silicon, with minimal gate thickness.

The source and drain regions are degenerately doped with one type of dopant, and the body region is degenerately doped with the other type. The gate is doped at the same time as the source and drains, however it is not necessarily degenerately doped.

B. Band Structure

Though the device can be doped either PNP, only the NPN doping scheme will be created. For the band structure see figure 2.

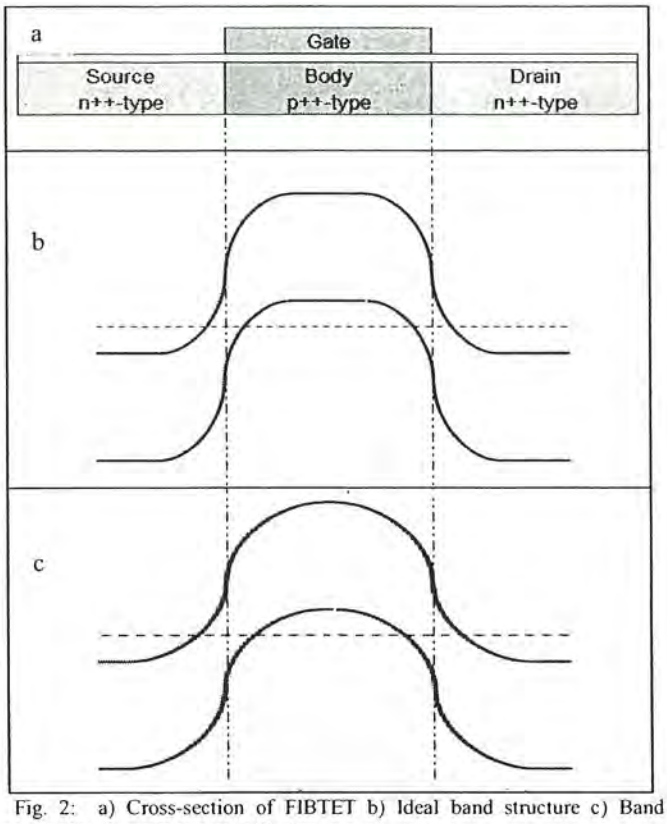

Fig. 2: a) Cross-section of FIBTET b) Ideal band structure c) Band structure if too much dopant diffusion occurs

As seen in Figure 2b, the band gap provides the electromagnetic barrier through which the carriers try to tunnel through. As the valence band in the body region becomes the same energy level as the conductance bad in the S/D regions the tunneling current will be cut off. In other words, as voltage is applied, a tunneling current will flow through the device. When a certain voltage is applied, the tunneling current will go to 0 A, with essentially only a leakage current will be dominant. After more voltage is added, the normal thermal device current will take over.

C. *Expected Results*

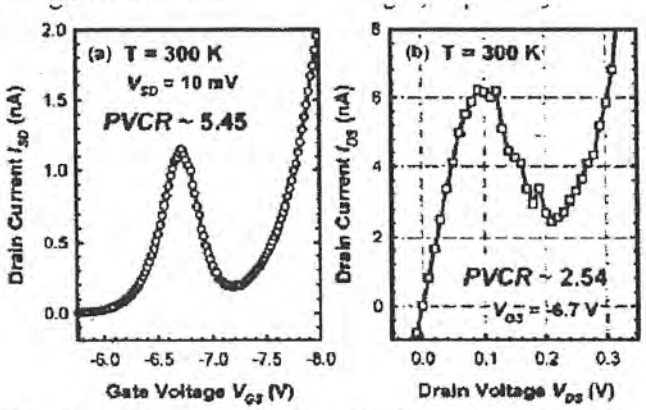

Fig.s 3: a) Ids-Vds curve b) Ids-Vgs . Data from reference [2]

Figure 3a shows the source to drain current characteristics as the gate voltage is swept. Figure 3b is the drain current as the drain voltage is swept. Both curves has a PVCR greater than 2.0, which is recognized as the absolute minimum needed for circuit applications.

In order to get devices with high PVCR values, the PN junctions need to be very sharp and nearly matched in doping levels. If the junctions diffuse and broaden out, figure 2c, than the tunnel barrier becomes much large. Since tunneling current has an exponential relationship with barrier thickness, the tunneling current will dramatically decrease. It does not take much before the tunneling current becomes washed out by the leakage current, as can be seen in figure 4.

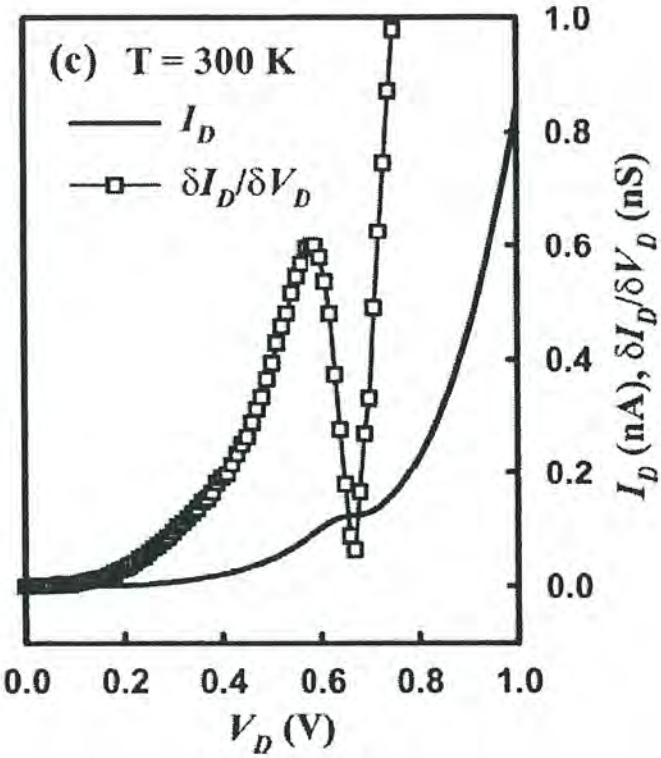

Fig. 4: Ids-Vgs curve with conductance (slope). Data from reference [1]

As seen in figure 4, there is no PVCR to speak of. However, there is a kink in the I-V curve. This kink is due to an increased current drive due to tunneling. However, the tunneling current is less than or equal to the leakage current. A plot of the slope (conductance) more distinctly shows where tunneling current exhibits.

D. *Multi-Value Logic*

As mentioned above a PVCR of at least 2.0 is needed in order to create multi-value logic circuits. The easiest way to obtain multi-value logic is a tunneling SRAM circuit. 2 tunneling diodes are placed in series, and another device (such as a MOSFET) can be used to drive a current (See Figure 5).

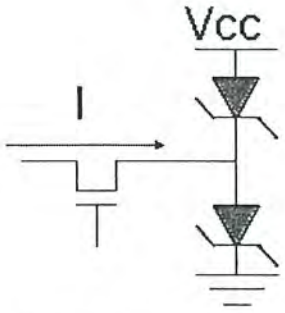

Fig. 5: Tunneling SRAM circuit for trinary logic

For the operation of this circuit, a simple load-line analysis can be performed. See figure 6.

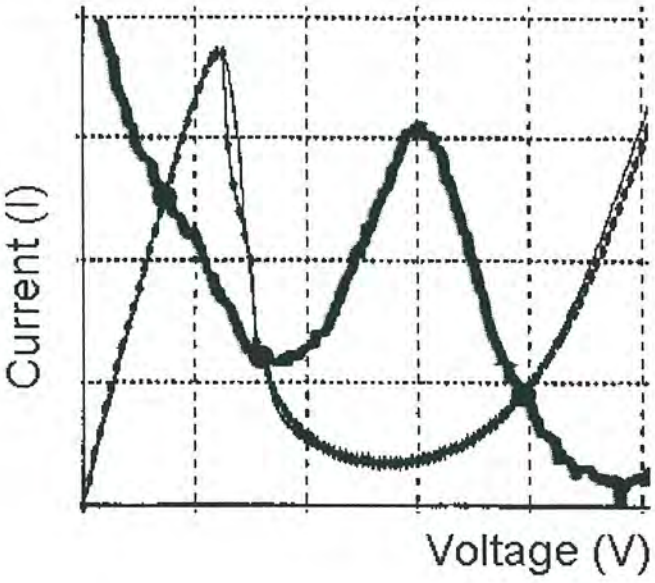

Fig. 6: Load Line for tunneling SRAM

The load line in Fig. 6 has two stable operating points, corresponding to the intersections of the load and drive diodes in the positive differential resistance regions. In the NDR region, however, the circuit is inherently bistable. Thus, biasing in this range will tend to force the circuit to latch either to a 0 or 1 state. The drive current determines the voltage level. In principle if several of these device are connected in series, the number of intersection points will increase. Therefore, a 0, 1, or 2 can be stored in this cell, instead of just a 0 or 1 if the load is determined by two series connected diodes. The storage capacity of a base "x" system compared to binary can be calculated with equation 1.

$$n_x = \frac{\log(2)}{\log(X)} * n_2$$

Equation 1: calculation to find number of bits needed in a base "X" system to provide same storage capacity as binary. "n" is the number of bits, the subscript determines the base number, and "X" is any whole number.

For a base 4 SRAM, half the number of bits are needed for equivalent storage in a binary system. Also, The number of devices (3), is half that required for traditional SRAM cells (6). So there is an increase in storage capacity per cell and per unit area.

III. Processing & Procedure

A mask set was designed with the intent of having fin based tunneling transistors (FIBTETs), tunnel diodes (with horizontal current flow), normal transistors, normal diodes, and resistors. Also, the same devices in the form of planar mesa structures were designed. The fabrication is to be done on SOI wafers, therefore mesa isolation will be sufficient. To accommodate all of the devices, plus electrical test structures, 7 masks were needed.

A 42 step processing procedure was than developed. Originally the procedure included a ploy-silicon sidewall spacer image transfer process in order to create the thin fins. Ion Implant was going to be employed to get dopants into the devices. RTP was to be used for dopant activation, and a thermal OxyNitride gate dielectric grown using a furnace. Most etches need to be an-isotropic, and therefore done using a RIE tool.

The spacer image transfer procedure is a precise technique that does not rely on good photolithography in order to create very small structures. See reference [3] for details. The target fin width was 70nm, with a height of 120nm.

Though fins were successfully created, the procedure was modified such that only planar tunneling devices and resistors were created using mesa isolation techniques. This resulted in a much shorter and easier procedure. Also, a proximity diffusion technique using RTP was used in order to introduce the dopants into the device structures. See reference [4].

IV. Results

Fin structures of 65nm in width (figure 7) were successfully created. However, due to differences in etch rates between bulk and SOI wafers caused these devices to be lost.

Fig 7: Fin structure (65 nm wide). Location in film stack unknown (most likely into the BOX material)

In future iterations of the project, the addition of stylus profilometry test structure would help to better control the timed etching required. Spectroscopic methods could not be used (VASE was not available) for non-destructive film measurements. Therefore, as soon as the wafer was etched in plasma, the vertical position on the film stack was lost. This resulted in overetching, thereby losing the SOI device structures.

Another attempt was made, where only the planar devices were to be made. This procedure only required a single plasma etch, and therefore could be completed with high confidence. Other etches utilized high selectivity chemical etchants.

Though no tunneling transistor devices have been found demonstrated, multiple diodes have exhibited a kink in their I-V characteristic which may indicate the presence of strong tunneling current. Furthermore, these diodes have extremely low breakdown voltage (< 1 V), suggesting that they are behaving as backward diodes. As seen in Figure 8, no NDR exists. . The slope (conductance) is also plotted. It shows a significant decrease in the slope occurs around 0.15 V, which coincides with the peak voltage in an Esaki diode. Also of note is the very low drive current in this region. This low current and lack of NDR indicates that the PN junctions are too broad. This is most likely due to a drive-in diffusion step that was done after both dopants were placed into the SOI layer. This would cause a band structure more like figure 2c instead of 2b. Additionally, it is possible that during the doping process, the dopants did not completely diffuse through the entire Si film atop the BOX. This may have left a parasitic region that effectively "shorted" the junction.

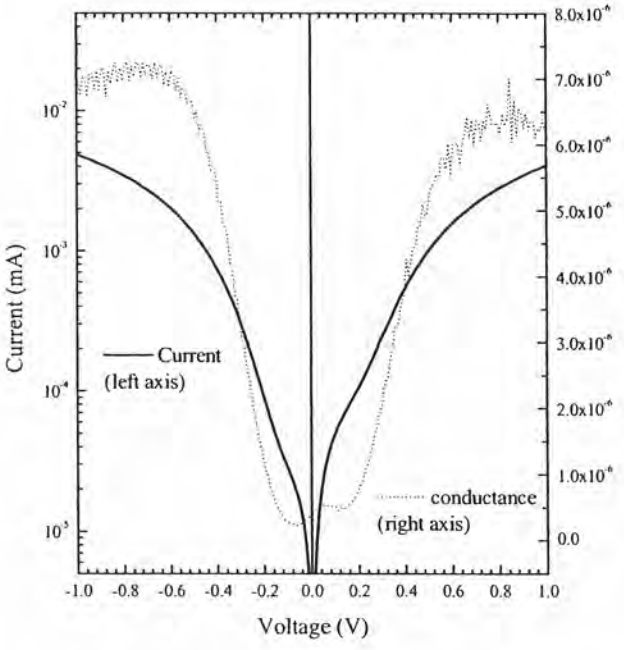

Fig. 8: I-V characteristics of a horizontal planar diode structure with its corresponding conductance

Figure 8 conclusively shows that a tunneling device was created. Assuming there are appropriate profilometry structures in the next mask set, and that the fins are small enough such that no drive-in steps are needed, FIBTETs can be successfully created.

More analysis will be done on the wafer fabricated in order ensure a successful 2nd generation fabrication. Initial wafer mapping shows that some areas of the wafer have bad p+-type resistors, but good n+-type resistors, and vice-versa. Also, due to reprocessing, some devices had significant amounts of SOI etch away. The reason for this is under investigation.

V. Conclusion

A 65 nm wide fin structure was successfully fabricated. Planar tunnel diodes were successfully fabricated. These devices did not exhibit NDR, however show that a horizontal tunneling transistor devices can be fabricated. Special attention must be placed into profilometry structures in order to monitor etch rates and current location in the film stack.

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References

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