Esaki Tunnel Diodes Formed by Proximity Rapid Thermal Diffusion

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Abstract— **For the first time tunnel diodes have been fabricated by Proximity Rapid Thermal Diffusion (PRTD) using spin on sources and the AG Associates 610 Rapid Thermal Annealing Furnace (RTA) at RIT. Initial devices revealed a maximum peak-to-valley current ratio (PVCR) of 1.3 with a peak current density (J_p) of 16mA/cm^2 at 300K. A second-generation design involving proximity diffusion of Boron and Phosphorous resulted in a higher J_p of 3A/cm^2 and an elevated PVCR of 1.97 at 300K. The increased performance is attributed to closer matching of the doping profiles via the phosphorous proximity anneal. This paper discusses the method of fabrication, key aspects of proximity diffusion, and lessons learned during evaluation.**

Index Terms— **Complementary Metal Oxide Semiconductor (CMOS), Esaki Tunnel Diode (ETD), Proximity Rapid Thermal Diffusion (PRTD), Peak-to-Valley Current Ratio (PVCR), Rapid Thermal Anneal (RTA), Spin on Glass (SOG).**

I. Introduction

THE dominant form of digital processing utilizes CMOS technology. In order to create faster chips and higher storage capacities these devices are continually scaled down to smaller and smaller dimensions. However, several problems occur with each new generation of these shrinking devices-increased leakage currents, increased power consumption, and increasing parasitics to name a few. All of these problems are leading many to the conclusion that the industry will reach the fundamental limits of current CMOS technology. That however will not be the end to faster chips and increased storage capacities. Band-to-Band tunneling devices—devices that exploit a finite potential barrier through which electrons may tunnel [1]—can be used to overcome many of these problems.

Employing the effects of quantum tunneling has been sought since 195 7with the creation of the Esaki Tunneling Diode. These devices are in a unique position—containing lower leakage currents, faster switching speeds, and a unique Negative Differential Resistance (NDR)—to revolutionize the semiconductor industry, however control of the impurity profiles within the diode technology and integration with silicon based CMOS technology has proven more difficult.

State of the art tunneling devices require complicated epitaxially grown stacks, which—despite providing abrupt degenerately doped impurity profiles required for electron tunneling—are currently not compatible with 300 mm silicon-based CMOS technologies. Furthermore, the technology required to fabricate them is costly and the processes expensive confining tunneling diodes to the academic arena. Proximity Rapid Thermal Diffusion (PRTD) on the other hand is both efficient and cheap- an exotic means to creating abrupt degenerately doped impurity profiles.

This diffusion technique utilizes rapid thermal annealing technology currently present in the semiconductor industry. In industry, doped layers have been traditionally produced using ion implantation followed by thermal annealing to repair subsequent lattice damage [3]. PRTD is a technique whereby a wafer is coated with spin-on glass (SOG) dopant and separated by a small distance (on the order of 300μm) from a device wafer. When both wafers are heated in the RTA the dopant species of the SOG matrix out-diffuse and dope the semiconductor surface via gas phase transport.

Complex and influenced by many factors—heating rate, cooling rate, source/device spacing, ambient flow rate, source preparation, and device preparation to name a few—PRTD is in a unique position for it agrees with the industry's current technological trend imposing a demand for shallow heavily doped junctions [3].

Unlike ion implantation and molecular beam epitaxy (MBE), PRTD can create CMOS compatible ETDs at a fraction of the cost. This technique provides a fast turn around rate and consumes little thermal budget. With further characterization one can foresee possible back end integration as the doping schemes of CMOS technology begin to require impurity concentrations on the order of $1x10^{21}cm^{-3}$. PRTD may be an answer to Band-to-Band tunneling device integration and if not, at the very least, will provide an alternative doping strategy to those interested in creating shallow heavily doped junctions in a variety of material and topography.

II. Theory

A. Proximity Rapid Thermal Diffusion

Proximity RTD is a complex process consisting of several steps similar to those in a chemical vapor deposition (CVD) process except for the fact that, unlike CVD, the dopant source in PRTD is not fed into the chamber but released from a SOD

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source [3]. The RTA used in PRTD emits ultraviolet (UV) radiation from tungsten-halogen lamps, which surround a quartz chamber used to house the silicon wafer. Silicon absorbs UV readily and as such one may heat the silicon substrate quickly. This heating strategy is responsible for both the diffusion and absorption of the dopant.

In the RTA, temperature is monitored using one of two methods: by attaching a thermocouple to the back of the silicon wafer or by using a pyrometer to monitor the emission of the silicon substrate. Both methods have their advantages and disadvantages: a thermocouple for instance ensures an accurate reading, but is costly and adds to the thermal mass of the substrate; a pyrometer on the other hand is inexpensive and not intrusive, but less accurate especially after line of sight obstruction.

This diffusion technique relies heavily on the preparation of the SOG sample. Unlike CVD, PRTD uses a constant source requiring that the SOG matrix out-diffuse readily for both short and extended periods of time (depending on the impurity profile needed). Studies show that the thickness of the SOG, the cure temperature, and cure time affect its out-diffusion properties. When the SOG is spun thin and cured at higher temperatures the matrix emits less [3]. If both Boron and Phosphorous sources are cured with the same temperature and time the Phosphorous emitter becomes the limiting factor for its diffusion is optimum when cured at 150°C [3].

Due to these restrictions optimum diffusion occurs with thicker SOG layers cured at 150°C-200°C. For this reason the author chose a curing process at 200°C for 20 minutes. This ensured elimination of any volatile organics present in the SOG film, which could harm the quartz chamber during diffusion while at the same time ensuring repeatable highly doped profiles. As a result repeatability in the temperature profiles during fabrication becomes a concern for replication will only occur if the temperature does not vary within each run.

B. Conventional Diode

A conventional diode consists of two doped regions one with an acceptor impurity and the other with a donor impurity. In a conventional diode the p-n junctions are non-degenerately doped—the valance and conduction energy bands are more than 3kT from the fermi energy band—and for this reason tunneling does not occur with little forward bias.

As one forward biases the structure, the conduction and valance bands of both the p and n regions begin to lineup sanctioning thermal current flow Fig. 1. As one reverse biases the structure the conduction and valance bands of both regions begin to separate. This separation can provide the carriers with the kinetic energy needed to ionize a semiconductor atom resulting in the creation of another carrier—known as avalanching—thereby contributing to negative current flow. The term breakdown is given to the voltage at which avalanching dominates and at this voltage the reverse-bias current approaches negative infinity Fig. 1.

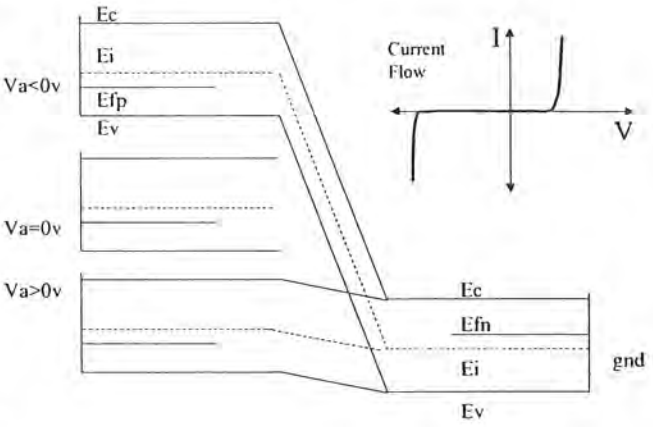

Fig. 1. Conventional p-n diode energy band diagram at Va<0v, Va=0v, and Va>0v biases. When the diode is in forward bias (Va>0v) diffusion current dominates. At a large reverse bias (Va<0v) the energy loss of each carry per collision is enough to ionize a semiconductor atom. This is called avalanching and should not be confused with the Zener process.

The total space charge region generated by the p-n region and modified by the applied voltage may be expressed as (1). It is interesting to note that as the acceptor and donor impurity concentrations increase their effective space charge regions decrease as shown in (2) and (3) respectively. This decrease in barrier width is extremely important when considering the size of the electron and its behavior as dictated by quantum physics.

According to quantum physics and particle-wave duality an electron is more likely to behave like a wave in a confined area [7]. As the wave function of the electron encounters the barrier induced by the space charge region there is a finite possibility that the electron may tunnel through [7]. The probability of tunneling increases as the dopant concentrations of the p-n junctions increase, because the space charge region decreases. For this reason tunneling diodes require degenerately doped profiles.

$$L = \left[\left(\frac{2\varepsilon}{q}\right)\left(V_{bi} + V_r\right)\left(\frac{1}{Na} + \frac{1}{Nd}\right)\right]^{1/2} \tag{1}$$

$$W_A = L\left[\frac{Nd}{(Nd + Na)}\right] \tag{2}$$

$$W_D = L\left[\frac{Na}{(Nd + Na)}\right] \tag{3}$$

C. Tunneling Diode

A tunneling diode is much like a conventional diode for it consists of two doped regions one with an acceptor impurity

and the other with a donor impurity. The difference with a tunneling diode is that these regions are degenerately doped—the valance and conduction energy bands are within 3kT of the fermi energy band—thereby decreasing the space charge region and increasing the probability of tunneling. Ideally, the doping profiles are completely abrupt—allowing a majority of the electric field to drop between the two regions—as shown in Fig. 2.

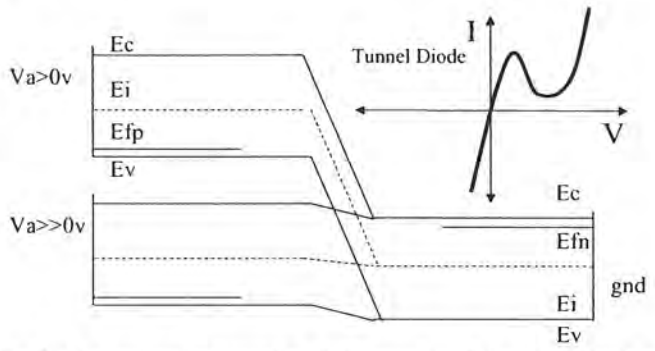

Fig. 2. Conventional p-n tunneling diode energy band diagram at Va>0v and Va>>0v biases. When the diode is in forward bias (Va>0) electrons are capable of interband tunneling (if available energy state exists in which to tunnel). Further forward biasing the TD (Va>>0) results in thermal current. Between these two region TDs exhibit a unique negative differential resistance (NDR).

The ETD current measured by applying a bias may be broken into three component currents: a tunneling component, a thermal component, and a leakage component Fig. 3. The space charge region Fig. 2 helps control the tunneling component. As one forward biases the ETD the probability of interband tunneling increases for a short time before starting to decrease, coinciding with the bias point where the available states in the valence band are no longer in alignment with populated states in the conduction band.. This decrease is attributed to a decrease in the available energy states to which an electron may interband tunnel. Observed while measuring the current flow Fig. 3 and also known as Negative Differential Resistance (NDR)—where resistance increases for incrementally increasing voltages resulting in a current flow decrease—this characteristic is unique to band-to-band tunneling devices.

As the applied bias increases further, the thermal current component dominates and the device behaves like a typical diode. Leakage current—also known as excess current—results from errors in fabrication. Poor isolation, self-induced interstitials, and poor metal contact are a few of the many contributors. Superimposing these three current components results in a characteristic "N" type current versus voltage response Fig. 2.

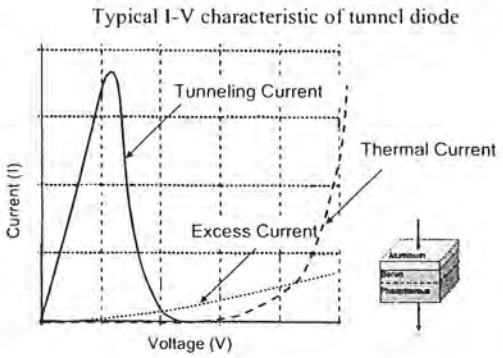

Fig. 3. Three current components of a tunneling diode. Tunneling current, thermal current, and excess (thermal) current add due to the principle of superposition resulting in the final current characteristic of this band-to-band tunneling device.

After fabrication one may characterize the ETD. A high PVCR (4), high peak-current-density (5), and low valley current density (6) are often sought. State-of-the-art devices contain PVCRs greater than 3 and J_ps in the kA range. Such characteristics are often ideal especially when intending to create trinary logic. It is not uncommon to see the PVCR of an ETD drop from 2.8 to 2.0 resulting from an increase in series resistance after integration.

$$PVCR = \frac{I_P}{I_V} \tag{4}$$

$$J_P = \frac{I_P}{A} \tag{5}$$

$$J_V = \frac{I_V}{A} \tag{6}$$

III. Experimental Procedure

The vertical p-n tunnel diode devices were fabricated on 6-inch 1.5mΩ-cm n-type silicon wafers. The highly doped bulk was chosen for the process split required it. Two main splits were considered during fabrication- those devices containing boron profiles only and those devices containing boron and phosphorous profiles shown in Table 1. Modeling these profiles proved difficult and as such one set of devices were made simpler than the others. The background concentration of the n-type silicon wafers was approximately $1x10^{19}cm^{-3}$ and because ETD require degenerately doped junctions the boron concentration of approximately $2x10^{20}cm^{-3}$ ensured that p-n compensation would not occur in these simpler devices. The SOG sources used in this investigation were Phosphorosilicafilm $1x10^{21}$ and Borofilm 100 from Emulsitone.

The device wafers were cleaned using a standard Radio Corporation of America (RCA) clean and each wafer was cleaved into four pieces. This bulk processing ensured efficiency. Research has shown an efficient diffusion scheme exists for phosphorous at 900°C for 1 second, phosphorous drive at 900°C for 90 seconds, and boron diffusion at 900°C for 1 second [2]. As such the following sub splits were considered: 750°C, 850°C, 900°C, and 950°C 1 second phosphorous diffusions followed by a 90second drive-in and completed with a 1 second boron as shown in Table 1.

Time was spent creating the diffusion recipes of the RTA. They needed to be repeatable and accurate so as to ensure replication between each treatment combination. After recipe creation the sources were fabricated. The source wafer type was chosen (6-inch 30Ω-cm p-type silicon) and the sources spun at 3000rpm for 30 seconds at room temperature. They were cured at 200°C for 20 minutes as discussed in the theory section and cleaved into four pieces.

The cleaved device was placed front side up on a base silicon wafer. The phosphorous source wafer was place front side down above the device and separated by three 300μm silicon-carbide spacers immediately after source preparation. The door was shut on the RTA and the diffusion run started three minutes later. The N_2 ambient flow rate was set to 4au (arbitrary units) and heated at 30°C/s. A ramp rate of 150°C/s was considered but disregarded. Research has shown that the lower ramp rate minimizes stress and interstitials created in the device during the ramping process [2].

After the 1second phosphorous diffusion the source and spacers were removed and the phosphorous driven-in for 90 seconds so as to reduce the surface concentration. The devices were cleaned in HF (50:1) for 1 minute, rinsed in DI water, and dried in N2 to remove any native oxide that could block the boron diffusion. Boron diffusion was conducted for 1 second followed by another (50:1) HF dip, DI rinse, and N2 dry to eliminate any native oxide. One should note that the temperature was monitored using a pyrometer.

Aluminum was evaporated to a thickness of 1500A and patterned. Photo Level 1 consisted of aluminum contact definition: a contact mask array of 20μmx20μm, 50μmx50μm, and 75μmx75μm features was used. To provide fine contacts and block the subsequent aluminum wet etch Shipley 1813 resist was soft baked at 115°C for 1 minute and hard baked at 125°C for 2 minutes. The aluminum wet etch was conducted and stopped by visual inspection.

After the contacts were defined the photoresist was removed with acetone. Using the Aluminum contacts as an etch block the devices were isolated using a Dry Tech reactive ion plasma etch in SF_6 4sccm, CHF_3 16sccm, 75mTorr, and 100 W. This recipe formed mesas approximately 3500A deep.

After fabrication the devices were tested using the Keithley 4200 Semiconductor Parameter Analyzer. Current versus voltage responses were measured and evaluated with respect to the fabrication process and die location. A complete comparison between the process splits was not performed. Wafers 1 and 5 proved to be resistors (the PRTD did not work) wafers 3, 4, 6, and 7 proved to be very good diodes. Tunneling devices were found on wafers 2 and 7 their operation is attributed to closer matching of the doping profiles vial the phosphorous proximity anneal and greater boron incorporation respectively.

TABLE I
ETD PROCESS SPLITS

Wafer #	Phosphorous Diffusion	Phosphorous Drive	Boron Diffusion
1	750°C 1sec	750°C 90sec	750°C 1sec
2	850°C 1sec	850°C 90sec	850°C 1sec
3	900°C 1sec	900°C 90sec	900°C 1sec
4	950°C 1sec	950°C 90sec	950°C 1sec
5	-	-	750°C 1sec
6	-	-	850°C 1sec
7	-	-	900°C 1sec
8	-	-	950°C 1sec

IV. EXPERIMENTAL RESULTS AND DISCUSSION

Fig. 4 shows a comparison of the 1st and 2nd generation devices. The tunnel current, valley current, and diffusion current are labeled on the 1st generation device. Notice the low PVCR of 1.3 and lower current density when compared to the second-generation device containing a PVCR of 1.97 and peak-current-density of $3A/cm^2$. This difference is attributed to matching of the dopant profiles. In the first generation device the n-type region contains a concentration of $1x10^{19}cm^{-3}$ compared to a theoretical boron concentration of $2x10^{20}cm^{-3}$ resulting in profiles that are more than one order of magnitude apart. The current drive of the 2nd generation device is much higher due to the match dopant profiles resulting in a narrower depletion region- this was expected.

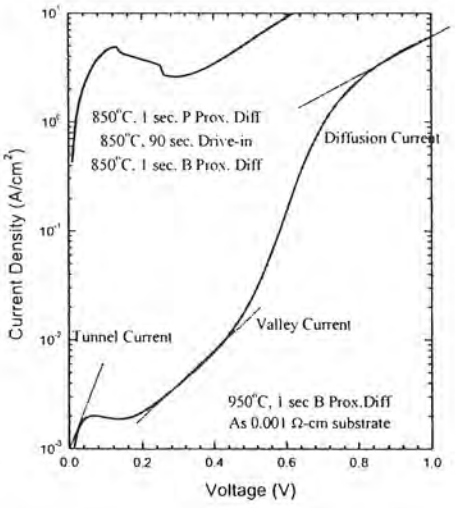

Fig. 4. Comparison of Esaki Diodes formed with B-only and P- and B-proximity diffusion. The current drive of the dual-diffused junctions is higher because matching doping results in a narrower depletion width (tunnel barrier).

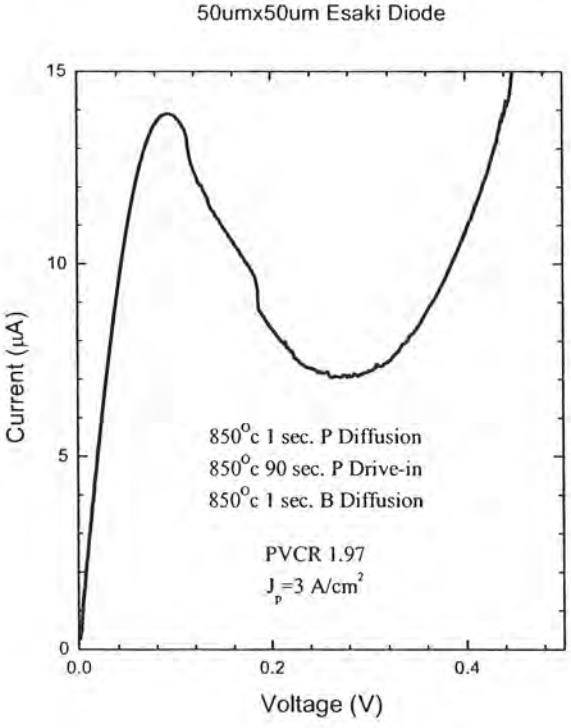

Fig. 5. 50x50 μm² Esaki diode with a 1.97 PVCR and 3 A/cm² peak-current-density. Both P and B were introduced via proximity diffusion.

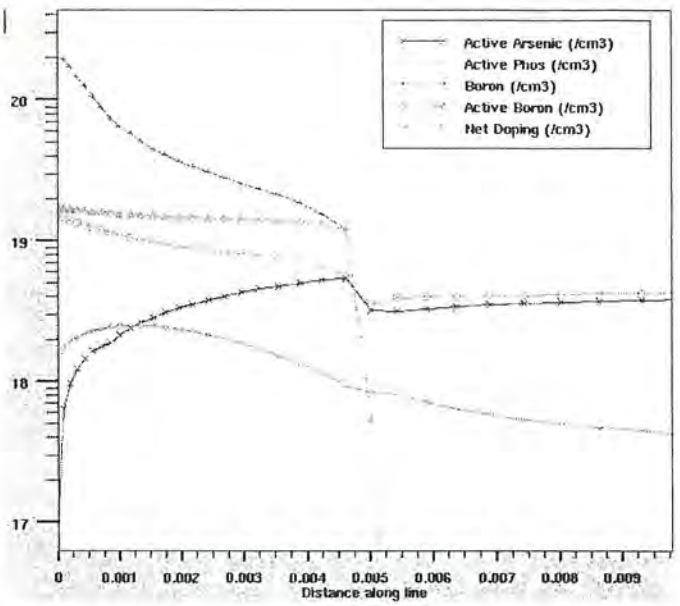

Fig. 6. Silvaco simulation of 850°C B/P/As sample (wafer 2). There is little compensation and the peaks of the boron and phosphorous profiles are an order of magnitude apart. This is to be expected.

Using Silvaco supreme and the temperature profiles recorded during fabrication sanction simulation of the second-generation device shown in Fig. 5. Silvaco simulation, as shown in Fig. 6, reveals a phosphorous surface concentration of approximately $1x10^{18}cm^{-3}$ and boron surface concentration of approximately $1x10^{19}cm^{-3}$. Simulation shows that the doped profiles are separated in concentration by one order of magnitude as expected. Unexpected is the decrease in arsenic background concentration. Research reveals this decrease as a factor involving the creation of interstitials that effectively lower the arsenic surface concentration. The ramp rate of 30°C/s may need to be optimized, but before doing so one should note that the simulation is not accurate.

Silvaco does not model proximity diffusion with great accuracy. For one it cannot simulate the emissivity of the source based on the SOG concentration and source preparation. And it cannot accurately simulate diffusion from the RTA process from the source to the device 300μm away within such a short time frame. The main reason for this is because Silvaco is built with accurate experimental data and little exists when it comes to proximity diffusion. Silvaco provides a good idea of what is going on but should not be trusted without bias.

In Fig. 7 device characteristics were plotted with respect to die location. Taking measurements from center to edge reveals a decrease in current density indicating that the PRTD needs to be optimized. Such variation most likely results from the gas flow rate used. The gas flow rate was adjusted arbitrarily in this experiment (4au). The investigator wanted a large amount of dopant in the device wafer—obtained by lowing the gas flow [3]—while at the same time providing enough gas flow to promptly cool the wafer after diffusion. As such a gas flow rate of 4au was used. After experimentation it was determined that using a gas flow rate of 2au during diffusion followed by a gas flow rate of 4au or higher after would be most optimum.

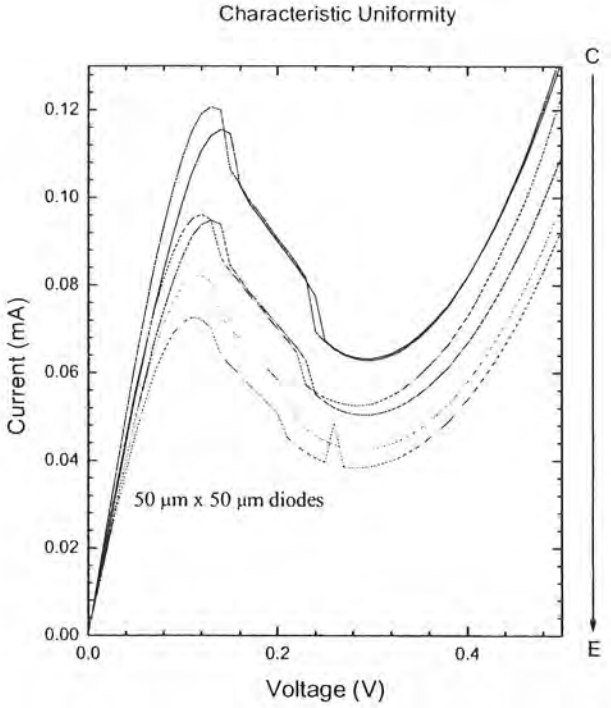

Fig. 7. Comparison of Esaki Diodes formed with P-B-proximity diffusion. Profiles recorded from center to edge show variation resulting from PRTD. An indication that the PRTD needs optimization.

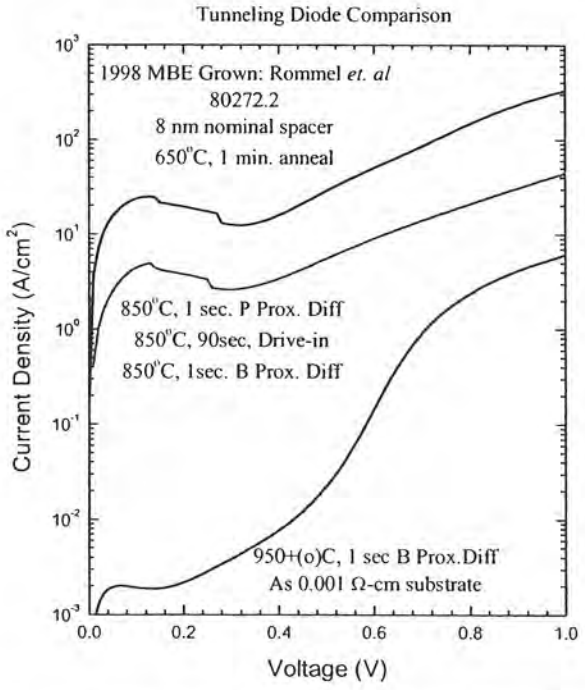

Fig. 8. Comparison of 1st and 2nd generation devices. The 2nd generation device comes close to a MBE grown device fabricated by Dr. Rommel in 1998. PRTD is a fraction of the cost and create comparable devices.

Both generations of Esaki Tunnel Diodes fabricated by PRTD are compared to a tunneling diode fabricated by MBE in 1998 [9]. Observation alone reveals the great improvement between generation and the possibility of further improvement. The MBE device is not far from the PRTD device, but this does not mean that reaching this advanced device's operation will be easy. To do so one must decrease the leakage current responsible for increasing the valley current and increase the devices current density. Furthermore, PRTD must be optimized only then will it be reliable.

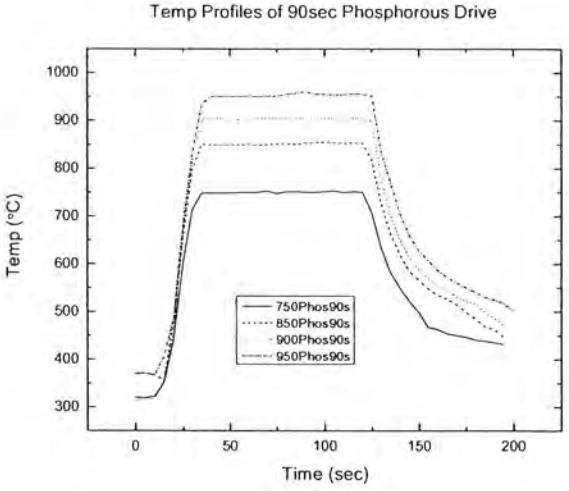

Fig. 9. Comparison of Phosphorous diffusion profiles. Shows that cooling rate depends on the time and temperature used.

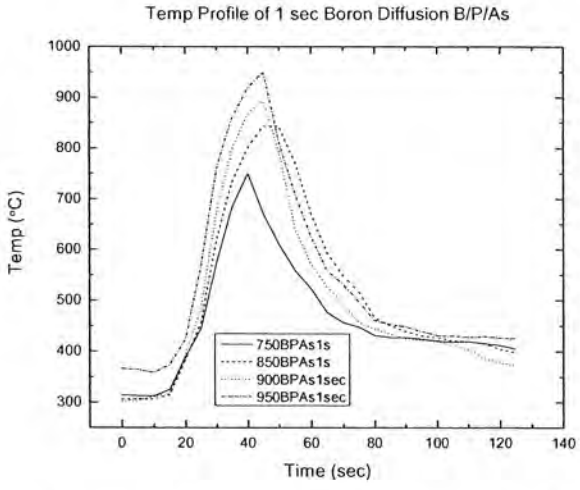

Fig. 10. Comparison of Boron diffusion profiles for wafers 1, 2, 3, and 4. Shows that greater variation exists at shorter times and longer temperatures.

Besides optimizing gas flow, temperature optimization must also be sought. Fig. 9 shows that for high temperatures and longer times the profiles are generally stable. The wafers at these high temperatures also took far longer to cool down. Further experimentation is needed to determine how much of an effect gas flow has on the device wafer's cool rate. It may be optimum to increase the flow for the higher temperatures only. Cooling the wafer fast with little defect introduction is ideal when considering the need for an abrupt junction.

Fig. 10 shows greater variation. In this case higher temperatures exhibit slower cool down rates most of the time. When compared to Fig. 9 however, one may notice that the cool down of Fig. 10 varies much more. Besides the temperature used one must note the method of temperature observation. Using a pyrometer to record the exact temperature profile within such a short time and such large temperatures is inaccurate. Ideally, one would seek the use of a thermocouple. When compared to a thermocouple, a pyrometer is more likely to give false readings especially when considering overshoot.

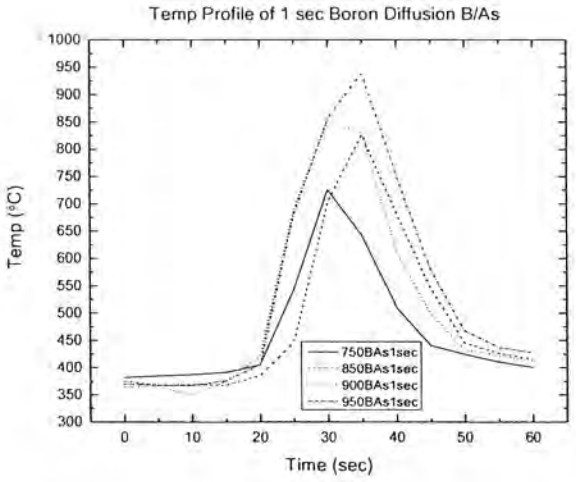

Fig. 11. Comparison of Boron diffusion profiles for wafers 5, 6, 7, and 8. Shows that greater variation exists over time. Wafers 5, 6, 7, and 8 were processed at a later date.

Fig. 11 reveals the effects of run-to-run uniformity. The B/As samples were processed a few days later and in comparison with Fig. 10 reveal greater variation. At this point in time the RTA started malfunctioning. In the case of the 900°C run, the machine would not reach the 900°C target and eventually aborting by turning off. This error in ramping (especially at higher temperatures) leads the investigator to believe that a thin film of material exists within the quarts chamber. If obstruction of the pyrometer's line of site is not the case then such error could be explained by a faulty pyrometer (wiring). It is hard to say what the machine was subjected to during its Spring quarter run—a run in which it is subject to all sorts of materials and processes—but there can be no doubt that something changed between May 16th and May 19th.

Ultimately, when comparing Fig. 9, Fig. 10, and Fig. 11 one can see that an optimum window does exist. Careful tedious experimentation will reveal this window and it is hoped that such a process will lead to a more advanced device well above the MBE device as shown in Fig. 8.

V. Conclusion

It was the purpose of this investigation to produce Esaki Tunnel Diodes formed by PRTD—in house at RIT—a process recently characterized and demonstrated at the University of Notre Dame. ETDs have been fabricated using this diffusion technique and characterized. PRTD optimization must be investigated further and RTA malfunction must be determined before future work can proceed. RIT now has a new doping scheme, which can provide highly concentrated shallow junctions on a variety of material and topography without inducing lattice damage. Further investigation must be performed to determine integration capability and long-term reliability.

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References

[1] L. Esaki, "Long Journey into Tunneling," IBM Thomas J. Watson Research Center, Yorktown Heights, New York, pp. 6-10, Dec. 1973.

[2] J. Wang, D. Wheeler, Y. Yan, J. Zhao, S. Howard, and A. Seabaugh, "Silicon Tunnel Diodes Formed by Proximity Rapid Thermal Diffusion," IEEE Trans. vol. 3, No. 1, pp. 1-9, March 2004.

[3] W. Zagozdzon-Wosik, P. B. Grabiec, and G. Lux, "Fabrication of Submicron Junctions—Proximity Rapid Thermal Diffusion of Phosphorous, Boron, and Arsenic," IEEE Trans. Electron Devices, vol. 41, pp. 2281-2289, Dec. 1994.

[4] S. Surdigo, R. P. Nandgaonlar, B. Curanovic, J. L. Hebdig, R. L. Saxer, S. S. Islam, K. D. Hirschmann, S. L. Rommel S. K. Kurinec, P.E. Thompson, N. Jin, P.R. Berger, "Monolithically integrated Si/SiGe resonant interband tunnel diode/CMOS demonstrating low boltage MOBILE operation," Solid State Electronics 48, pp. 1907-1910, March 2004.

[5] A. Sedra, K. Smith, "Microelectronic Circuits Fourth Edition," Oxford University Press Inc., pp. 353-427, 1998.

[6] A. Seabaugh, "Promise of Tunnel Diode Integrated Circuits," Tunnel Diode and CMOS/HBT Integration Workshop, pp. 1-13, Dec. 1999.

[7] S. Kurinec and S. Sudirgo, "Nanotechnology: Principles, Applications, Ethics, and Social Change," Nanotechnology Foundation, Session 3, pp. 1-12, April 2004.

[8] K. E. Petersen, "Silicon as a mechanical material," in IEEE Trans. Proceedings of the IEEE, vol. 70, pp. 420--453, May 1982.

[9] "Development of Delta-B/i-Si/Delta-Sb and Delta-B/i-Si/Delta-Sb/i-i/Delta-B Resonant Interband Tunnel Diodes For Integrated Circuit Applications," S. L. Rommel, N. Jin, T. E. Dillon, S. J. Di Giacomo, J. Banyai, B. M. Cord, C. D'Imperio, D. J. Hancock, N. Kirpalani, V. Emanuele, P. R. Berger, P. E. Thompson, K. D. Hobart, and R. Lake, 58th Annual Device Research Conference in Denver, CO (June 19-21, 2000).

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