Study of Silicon Solar Cell Array to Power MEMS Cantilever Actuator

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Abstract— A solar cell array to power a on board micro-electromechanical polysilicon cantilever actuator was designed, fabricated and tested. The device composes of two solar cell arrays one array with 330 solar cells and another array with 300 solar cells. The device also consists of several cantilevers. The fabrication process involved over fifty process steps including nine photolithography levels. To optimize the performance of the solar cell array the entire process was simulated using SILVACO SUPREM simulation software. Electrical examination using ATLAS software allowed for parameter extraction of the computer-generated solar cells. Modeling the extracted parameters with device physics equations allowed for a SPICE level-2 analysis that could be verified through electrical testing of the actual fabricated solar cells. Measurements were made throughout the fabrication process. The completed devices were tested and pictures were taken of the cantilevers and solar cell array.

***Index Terms*—solar cell array, polysilicon cantilever actuator, Silvaco Suprem, Atlas.**

I. INTRODUCTION

The purpose of this project is to investigate the possibilities of using a bulk silicon solar cell array as an on-board power source for electrostatic MEMS devices. To demonstrate the solar cell array as an on-board power source, an electrostatic polysilicon cantilever actuator will be fabricated and powered by the array.

The devices were fabricated on four inch P-type wafers with a resistivity of 5-15?/cm. Each die contains two solar cell arrays. The major solar cell array will consist of 330 solar cells connected in series to generate a final voltage of 99 volts. The minor solar cell array will consist of 300 solar cells connected in series to generate a final voltage of 90 volts. The difference in the two arrays is to test different cantilever devices as well as a protection plan incase the major array produces more voltage than 150 volts. The array is broken into several rows comprising of 30 solar cells per row. Each row will have a different aluminum contact design over the solar cell. This will help determine the optimal conditions for the solar cell array. The voltage generated will be used to create an electric field that will force the polysilicon cantilever actuator to move two microns towards the silicon.

The solar cells and polysilicon cantilever actuator will be fabricated simultaneously on a P-type silicon wafer. To help ensure success of the project, the process of the device was simulated using Silvaco Supreme a microelectronic device simulator. The simulation helped in determining times and temperatures of key process steps as well as simulated result for current and voltage that could be compared with the fabricated array. During the fabrication of the device the process flow changed.

II. MOTIVATION

In today's fast growing micro-electromechanical systems (MEMS) industry self-contained power supplies are necessary. The power requirements of micromachined devices are very different from conventional circuits. Many devices need large amounts of voltage to create forces and use external power connections. For many MEMS devices, this conventional method is preferable, but for some operations, like space-based MEMS or free-moving microrobotic systems, a self-contained on-board power supply is desirable.

III. THEORY

Solar cells directly convert light into electricity, and use similar physics and technology as that used in the microelectronics industry. The direct conversion of sunlight into energy using solar cells is called the *photovoltaic effect*. The word photovoltaic is a combination of the Greek word for light and the name of the physicist Allesandro Volta. The conversion process is based on discovery by Alexander Bequerel in 1839. The photoelectric effect describes the release of positive and negative charge carriers in a solid state when light strikes its surface.

The first step in the conversion of sunlight into electricity is the absorption of light. The absorbed light causes electrons in the material to increase in energy, at the same time making them free to move around in the material. However, the electrons remain at this higher energy for only a short time before returning to their original lower energy position. To collect the carriers before they lose the energy gained from the light, a pn junction is typically used.

A pn junction consists of two different regions of a semiconductor material, with one side called the p-type region

and the other the n-type region. In p-type material, electrons grain energy when exposed to light but also readily return to their original low energy position. However, if they move into the n-type region, then they can no longer go back to their original low energy position and remain at a higher energy. The process of moving a light generated carrier from where it was originally generated to the other side of the pn junction where it retains its higher energy is called *collection*. To help better understand how collection works see figure one.

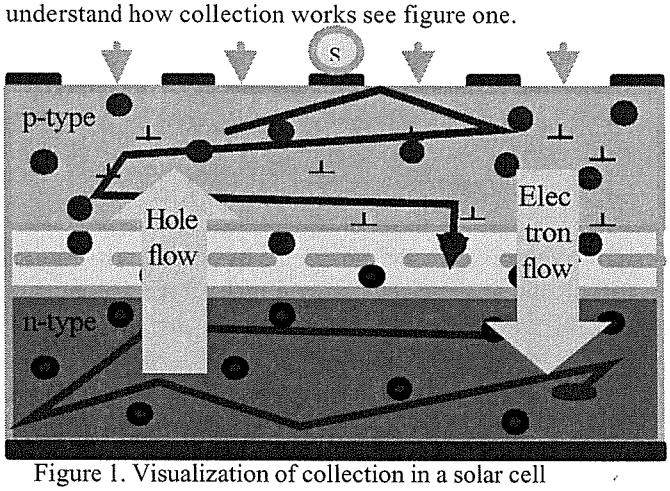


Figure 1. Visualization of collection in a solar cell

Once a light generated carrier is collected, it can be either extracted from the device to give a current, or it can remain in the device and give rise to a voltage. For this project it is important to acknowledge that the voltage is weakly dependent on light radiation; it is the current intensity that increases with higher luminosity. In this project, the amount of current needed is negligible to the 100 volts that needs to be generated. The usable voltage from solar cells depends on the semiconductor material. In silicon it amounts to approximately 0.5 V. A lower voltage of .3v is going to be assumed for this experiment.

For this experiment a P-type wafer is used to isolate the N-type well and an inner P+ well. These wells are designed to always be biased positive with respect to the p-type wafer. This ensures that the pn junction that is formed is in forward bias, and there is no current leaking to the substrate. Current will flow from the P+ region to the N+ region and then over the aluminum to ground. The electric field will travel in the opposite direction. The I-V characteristic follows Ohm's Law: I = V/R. See figure two for a visualization of the solar cell array.

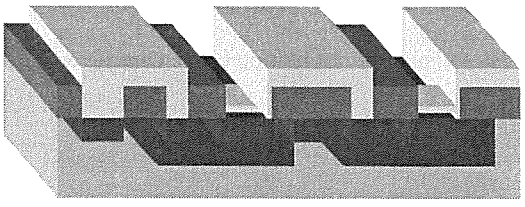


Figure 2. solar cell array. The light blue area is the N-well the dark blue is the N+well, the green area is the P+well, the red area is oxide and the gray area is aluminum.

In order to make the appropriate voltages, single solar cells are interconnected to form larger units. Cells connected in series have a higher voltage, while those connected in parallel produce more electric current. The array in this project will consist of 330 solar cells connected in series to achieve a minimal voltage of 99 volts. Typical arrays are interconnected solar cells embedded in transparent Ethyl-Vinyl-Acetate, fitted with an aluminum frame and covered with transparent glass on the front side. The array in this project will have each of the solar cells embedded in the bulk substrate and connected with aluminum.

The level of efficiency expressed as ? indicates how much of the radiated quantity of light is converted into useable electrical energy. Increasing the level of efficiency will lower the costs of solar cells. However, different loss mechanisms set the limits. The theoretical maximum level of efficiency is approximately 28% for crystal silicon. Some of the loss mechanisms are optical losses, such as the shadowing of the cell surface through contact with the surface or reflection of incoming rays on the cell surface, electrical resistance losses in the semiconductor and the connecting cable, and the disrupting influence of material contamination, surface effects and crystal defects are significant. In this experiment the junction depths of the regions will be looked at to maximize the open circuit voltage of the circuit. Silvaco SUPREM simulation of the device will accomplish this. Also, the placement of the aluminum contacts will be varied to identify what finger pattern collects the most electrons.

Below are the equations used to determine the open circuit voltage (Voc) of the solar cells, the short circuit current (Isc) and the efficiency (?) of the solar cell. Voc is maximized by minimizing Io.

$$V_{oc} = \frac{kT}{q} \ln\left(\frac{I_{sc}}{I_0} + 1\right) \quad (1)$$

Voc is the open circuit voltage k is Boltzmann constant T is the absolute temperature of the cell (K), q is the charge of an electron, Isc is the short circuit current.

$$I = 0 = I_0\left(e^{\frac{qV_{oc}}{kT}} - 1\right) - I_L \quad (2)$$

I_L is the light current generated current. $I_L \sim$ Isc at very low current densities. Io is dark reverse saturation current of the diode Io can range from 10^{-11} to 10^{-14} A/cm2 and also equals equation three.

$$I_0 = \frac{qn_i^2 D_n}{N_A L_n} \quad (3)$$

$$L_n = \sqrt{D_n \tau_n} \quad (4)$$

$$D_n = \frac{\mu_n KT}{Q} \quad (5)$$

Solar cell efficiency (?) can be determined from equation six

$$I_m V_m \quad FF * Isc * Voc \quad (6)$$

FF is a fill factor which is the optimal power setting which equals equation 7.

$$FF = \frac{Vm * \mathrm{Im}}{Voc * Isc} \quad (7)$$

The cantilever will move from the electrostatic forces. An electrostatic force is the force created by a voltage difference between two points. As the voltage between two points increases, the electrostatic force becomes more intense By applying a voltage to the top of the cantilever a capacitance charge will build up and pull the cantilever toward the substrate actuating as ground.

The dimension of the main cantilever actuator is 150 micron long, 5 micron wide and 2 micron thick with stress relieving dimples. The cantilever actuator will move 2 micron down toward the substrate. Two microns was chosen because the movement can be easily observer under a microscope.

To determine the voltage necessary to move the cantilever actuator, first the mechanical force needed to move the silicon two microns must be found. This force is then used with in order to determine the voltage. The equations below were used in determining the voltage necessary to move the cantilever.

The parallel plate capacitor is the most fundamental configuration of capacitive sensors. The definition of capacitance is given in equation eight. The C represents capacitance, Q is the stored charge, and V is the electrostatic potential.

$$C = \frac{Q}{V} \quad (8)$$

The stored electrostatic energy is expressed in equation nine.

$$E = \frac{1}{2}CV^2 = \frac{1}{2}\frac{Q^2}{C}. \quad (9)$$

Neglecting the fringe electric field, the field lines are extended uniformly through the capacitor plates. According to Gauss's law, the magnitude of the electric field, E, is related to Q by equation ten.

$$E = Q/\varepsilon A \quad (10)$$

Setting equations nine and ten equal to each other equation eleven is obtained. Equation eleven

$$C = \frac{Q}{\frac{Q}{\varepsilon A}d} = \frac{\varepsilon A}{d}. \quad (11)$$

is the fundamental expression for the capacitance. The magnitude of the capacitance is related to the distance between the two surfaces and the area that overlap this distance. The equation is also a function of the electric permittivity, which is subject to many influences.

The electrostatic energy from the capacitance creates forces in many directions the magnitude of these forces can be expressed as equation twelve.

$$F = \frac{\partial E}{\partial x} = \frac{1}{2}\frac{\partial C}{\partial x}V^2 \quad (12)$$

In the equation x is the coordinate of interest. The force is perpendicular to the plates this and is the force that pulls the cantilever actuator to the substrate and the magnitude is expressed in equation thirteen.

$$F = \frac{\varepsilon o \varepsilon r A V^2}{2d^2} \quad (13)$$

This force can now be compared to the physical mechanical force needed to move the cantilever. The equation will identify the force required to move a bar of a certain composition in one direction.

$$F = \frac{Y_{\max} 3Ebh^3}{12L^3} = \frac{\varepsilon o \varepsilon r A V^2}{2d^2} \quad (14)$$

In the equation above Ymax is the movement in the y direction, E is Young's modules, b is the width of the cantilever actuator, h is the height of the cantilever actuator and l is the length of the cantilever actuator. The $3bh^3/12L^3$ is determined from the inertia of a bar. It is understood that this is simplifying the cantilever actuator structure and because of the dimples less force will actually be need to be to move the fabricated cantilever actuator. This equation was used as a safe guard to ensure that enough voltage will be applied to the cantilever actuator because the actual dimensions of the final cantilever structure will be unknown until fabrication is complete. The dimensions of the cantilever along with an estimated area between the surfaces to be 25 μm a voltage of 90.2 was determined.

Below is a visual representation of the cantilever actuator.

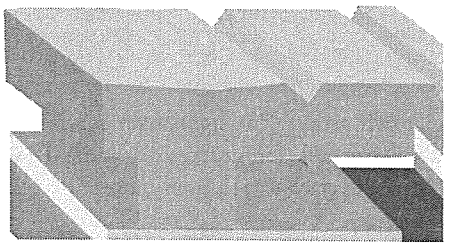


Figure 3 The green layer is the substrate the blue is an oxide level and the yellow is a nitride level the nitride is needed as a dielectric to force the voltage applied to go the end of the cantilever and then to ground.

Silvaco SUPREM Simulation

To allow for optimal solar cell performance the junction depth that is the length that the doped wells travels into the silicon substrate is critical. The doping travels into the silicon substrate by diffusion at high temperatures. For simple doping profiles hand calculations can be used but for complex process flows simulation can give results with more accuracy.

Doping Profiles

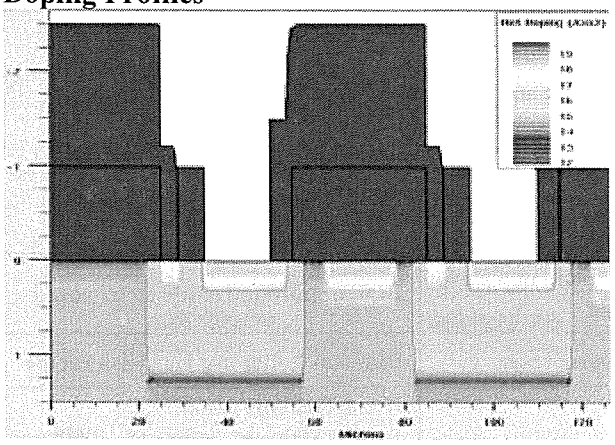


Figure 4

Electric Field

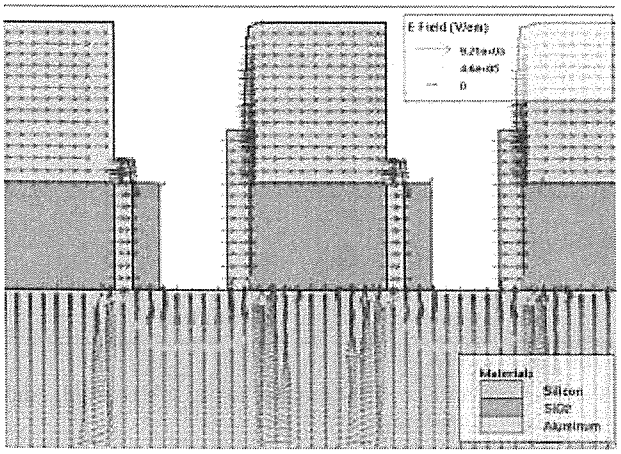


Figure 5

Photogeneration Region

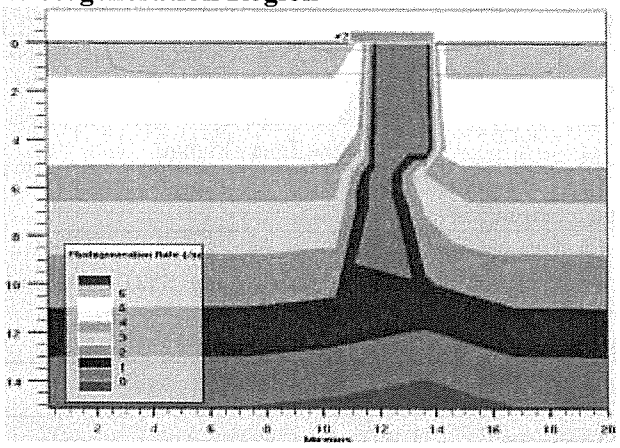


figure 6

Photo Generated Current

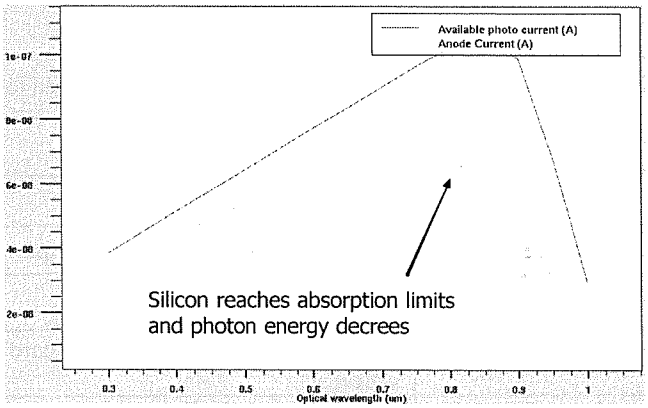


figure 7

Solar Cell Voltage

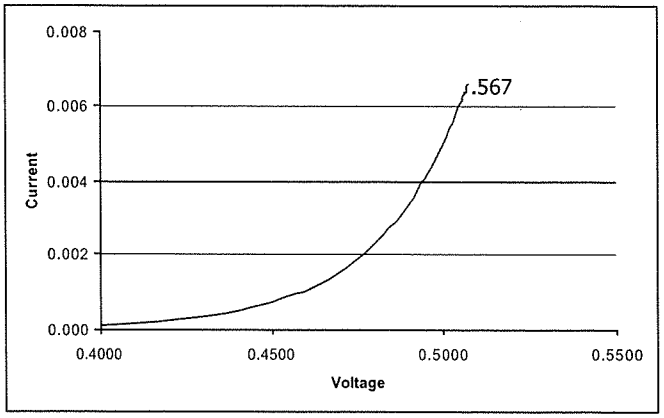


figure 8

Processes Steps

Steps	Technical Info
1. Scribe wafers	
2. 4pt probe wafers	Use 4pt probe station
3. RCA Clean	Done in RCA bench standard process see appendix RCA
4. Grow 5000Å of oxide.	Use Bruce Furnace

5. Measure using nanospectrometer	Use same Nanospectrometer for all measurements.
6. Deposit 3500? silicon Nitride	LPCVD 3500 Å Silicon Nitride Si3N4 Temp = 800-810-820 °C DiChlorosilane Flow 30% Ammonia 30%flow Time =15 min
7. Measure using nanospectrometer	
7. 1st Lithography removal of nitride from solar cell region	Lithography using SVG track and GCA Stepper.
8. Etch Nitride layer	Lam 490 etcher
9. Strip resist	Branson Asher use Hard ash recipe
10. 2nd Lithography for N well (Base)	Lithography using SVG track and GCA Stepper.
11. Etch Oxide	BOE or buffered oxide etch is used to etch glass. BOE is 10:1 water to HF. Etch rate of (1000Å/min).
12. Base Implant	5e12 energy 200kev
13. Strip resist	Branson Asher use Hard ash recipe
14. Etch Oxide	BOE. Etch rate of (1000Å/min).
15. RCA Clean	Done in RCA bench standard process
16. Base Drive in and 500Å oxide growth	10min 800temp in nitro 10min 800temp ramp to 1000temp 310min 1000temp nitro 30min 1000temp dryo2 20min 1000temp nitro 30min 1000temp ramp to 800temp
17. Deposit oxide	5000Å oxide PECVD
18. 3rd Lithography for N+ region for omic contact	Lithography using SVG track and GCA Stepper.
19. Etch Oxide	BOE or buffered oxide etch is used
20. Implant for Omic contact	1e13 energy 20kev
21. Strip resist	Branson Asher use Hard ash recipe
22. Remove oxide	BOE or buffered oxide etch is used
23. RCA Clean	Done in RCA bench standard process
24. Deposit oxide	3. um of sacrificial oxide PECVD done in P5000
25. 4th lithography create dimples in cantilever	Lithography using SVG track and GCA Stepper.
26. Etch into Oxide to make dimples	BOE or buffered oxide etch is used
27. Strip Resist	Branson Asher use Hard ash recipe
28. 5th lithography anchor window and removal of oxide for P+ emitter in solar cell array and high voltage break down stop.	Lithography using SVG track and GCA Stepper.
29. Etch Oxide for anchor and P+ Emitter	BOE or buffered oxide etch is used
30. Strip Resist	Branson Asher use Hard ash recipe
31. RCA CLEAN	Done in RCA bench standard process
32. Dope P+ silicon	Spin coat with Emulsitone ***, spin on at 3000 rpm, for 30 sec Bake at 200 C, 15 min, oven next to implanter
33. Deposit 2 um Polysilicon	LPCVD Tool Temp 650 °C Pressure 330 mTorr Silane Flow 48% Dep Rate 235 Å/min Time 90 min
34. Dope N+ Polysilicon	Spin coat with Emulsitone N-250, spin on at 3000 rpm, for 30 sec Bake at 200 C, 15 min, oven next to implanter
35. 6th lithography cover Cantilver strip poly and oxide off of solar cell array	Lithography using SVG track and GCA Stepper.
36. Etch unwanted polysilicon	Lam 490 Etcher
37. Etch unwanted oxide	BOE or buffered oxide etch is used
38. strip resist	Branson Asher use Hard ash recipe
39. Drive in dopants and Grow 500Å of oxide.	10min 800temp in nitro 10min 800temp ramp to 1000temp Nitro 10min 1000temp nitro 30min 1000temp dryo2 10min 1000temp nitro 30min 1000temp ramp to 800temp Nitro
40. Deposit 10,000Å oxide. LTO	LTO
41. 7th Lithography for Contact cut and removal of oxide from cantiliver	Lithography using SVG track and GCA Stepper.

42. Etch Oxide	BOE or buffered oxide etch is used
43. strip resist	Branson Asher use Hard ash recipe
44. RCA Clean	Done in RCA bench standard process
45. Deposited aluminum on the wafer.	The aluminum is used as a hard mask for the polysilicon actuator the aluminum should be 2 um. Deposited with the CVC evaporator
46. 8th Lithography for aluminum create contact cuts and hard mask for actuator	Lithography using SVG track and GCA Stepper.
47. Aluminum etch	50 C aluminum etch in phosphoric acid
48. strip resist	Branson Asher use Hard ash recipe
49. Etch unwanted polysilicon	Could use Drytech Quad SF6 30 sccm CHF3 30 sccm 40 mTorr 200 watts Rate 1900 Å/min 12 min/wafer
50. Release actuator with Oxide etch	Use HF + HCl etch until structures are released. Time about 20 min.
51. strip resist	Branson Asher use Hard ash recipe
52. Al sinter	Use Bruce Furnace
53. Test	Shine light onto solar cell region record voltage

IV. FABRICATION

During fabrication of the devices the nitride level started to lift off severely after the second implant. This was due to an uneven and excessive nitride deposition. During the nitride deposition the gasses were accidentally shut off. Bruce Tolleson was there and was able to turn on the gasses so the deposition could continue. When recalculating how much time was left on the run I did not account for the time that the gas was shut off. But even though the gas was shut off there was still gas in the lines. This gas continued depositing onto the wafers. This excessive nitride deposition along with the poor uniformity of the nitride film created enough stress for the film to lift off.

When the film lifted off I consulted Dr. Fuller with what I should do and he told me to remove the old nitride layer using a hot phosphors etch remove the base oxide layer and then grow a new oxide and redeposit nitride. The problem with this line of action was that I had decided to make the nitride film my photo alignment layer. Meaning the nitride layer contains the alignment marks that all of the other photo lithography steps align to. If I were to just remove the nitride layer and grow another one my alignment would not be correct and I would probably not have working devices. Dr. Fuller then suggested to grow a thin layer of oxide etch and then continue on. This extra oxide growth should create a step because oxide grows at a different rate over a doped region compared to the silicon substrate.

I proceeded as Dr. Fuller had instructed. This plane of action did have one problem left and that was thermal budget. The original simulation did not account for all theses extra thermal steps. The two oxidation growths and the nitride deposition all are done at temperatures that will diffuse the phosphorus already implanted deeper into the substrate. There also was a time restraint on the rework. I needed to complete all the work in one day in order to deposit my 3 um of oxide using the P5000. The P500 converts from a six inch tool to a four inch tool and was only going to be at four inches for a couple of days. The oxide deposition being performed in the P5000 was crucial because the oxide that it deposits is more uniform than the low temperature oxide done in the LPCVD. Also if the 3 um of oxide was done in the LPCVD it would take over 8 hours compared to 2 hours for the P5000.

The rework was done in time to deposit the 3 um of oxide by the P5000. Unfortunately there was not enough time to do any photo lithography before the oxide deposition. This created a complex series of lithography steps to get back on track. Also the alignment marks were there but very blurry. The alignment of all remaining photo steps was not great, the alignment was usually of a micron or two in either x or y and sometime both but there was nothing to do to eliminate this problem

Do to time restraints and tool availability the wafers were split into two lots. The first lot would be the wafers that would undergo the steps necessary to create the solar cells. The other lot would undergo the necessary steps to create the cantilevers. This allowed me to save time and be able to work on either lot depending on what was available.

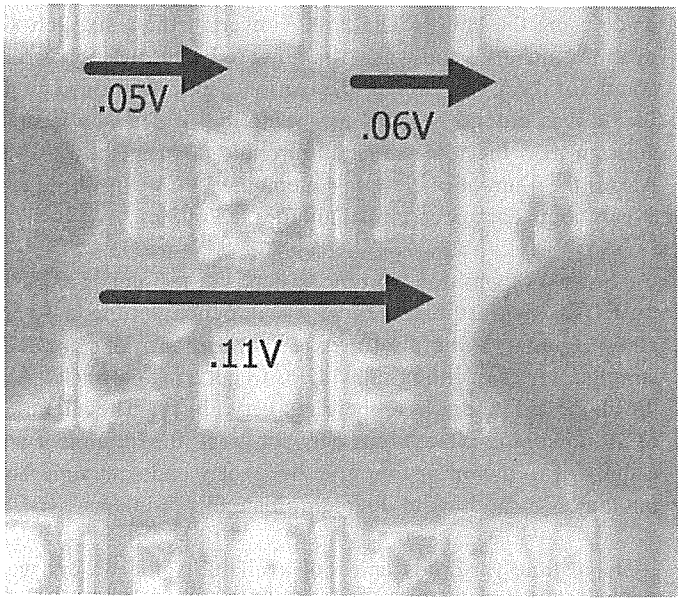
This strategy worked I was able to complete both lots and begin testing. The complete new process flow along with data for depositions and growths is located inside my lab notebook.

V. ANALYSIS

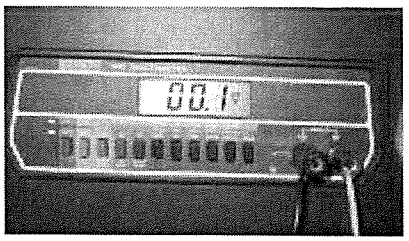
The solar cell array was tested by a multimeter to determine the open circuit voltage (VOC). A probe was placed at both ends of the cell and a voltage was recorded. There were very few cells that worked. Only five working cells total were found. They have an average VOC of .058 V.

One array was discovered consisting of two solar cells. The overall voltage produced by the array was 108.5 mV. One cell had a voltage of 55.7 mV and the other 53.4 mV. This showed a

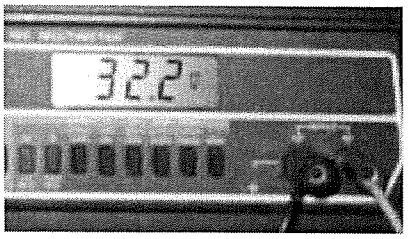
small voltage loss across the two cells but is probably do resistance caused by poor alignment. A third cell was tired in the array but the overall voltage dropped to 80 mV showing that it was not working device. It was resisting the flow electricity. The voltage obtained from the solar cells is less than the expected .3 volts per cell. I believe this is due the fact the junction depths of the solar cell are to deep for optimal performance. Also the alignment problem could have created bad contacts increasing resistance or no contacts at all. A new simulation was done to identify what the new voltage of the solar cells should be. The simulation results were not believed to be accurate. The crossectional view of final the junction depths are not correct. When running a simulation the mesh or the amount of data points taken and where they are taken is crucial if the mesh is not done correctly the results will not be accurate. For the first simulation it took several days adjusting the mesh to create acceptable junction profiles. I was unable to identify a proper mesh for the new simulation. The images below are of that array.



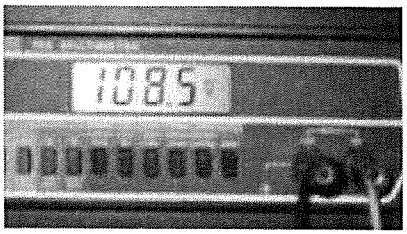
NO light Present



Room light Present

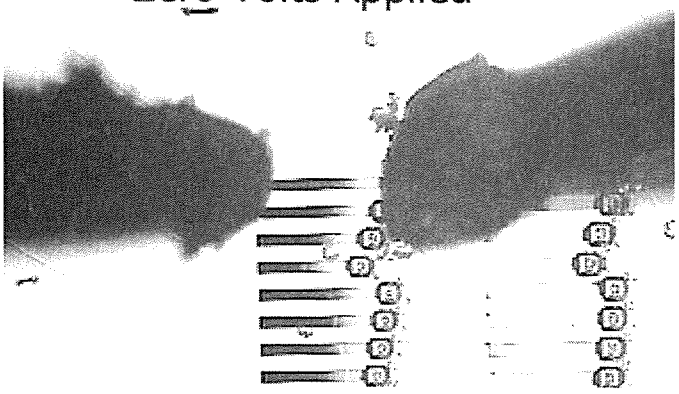


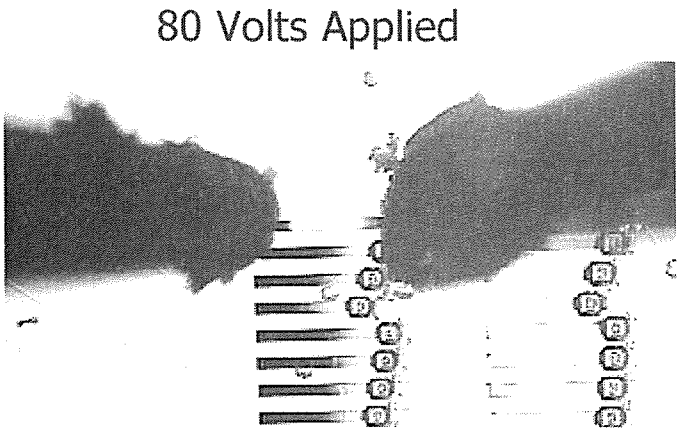
Direct light on wafer



The cantilevers were also successfully tested. Several cantilevers were tested and would pull down to the substrate. There was a problem though the force to pull the cantilevers down to the substrate seemed to bend many of the cantilevers. This bend would not allow the cantilever to return to its original position. I believe this bending might be do to a larger distance between the wafer and the cantilever than calculated or the polysilicon cantilevers are either molecularly weak or to thin. The polysilicon was deposited over two runs and this might have created polysilicon that is not as strong as expected. The polysilicon deposited the first run might not be bonding well with the polysilicon of the second run. These multiple runs also create uniformity issues where there might be arrears that are too thick or to thin. Below is a picture of 200 um long cantilever being deflected by 80 volts of electricity. The movement of the cantilever can be seen by the change in color from black to a shiny white.

Zero Volts Applied





VI. Conclusion

The solar cell array and cantilever actuator were a success despite complications during fabrication a working array was discovered comprised of two solar cells with a VOC of 108.5 mV. Several cantilevers were successfully tested. For future work the process that was used to fabricate the solar cells should continue to be resimulated and compared to the results. Further electrical testing should be done on the working solar cells such as a diode sweep to help better understand there behavior.

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