

Fabrication of Polysilicon Micro Valve Array

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Abstract: Valves are an essential part of pumping systems, which are used in a wide variety of applications including medical, automotive, gas sampling, and gas analysis. The objective of this investigation is to design and fabricate microvalve arrays. The valve consists of a polysilicon flap suspended over a through hole in the silicon. It is intended to allow airflow in one direction and inhibit airflow in the reverse direction.

The design requires only three mask levels, two on the front of the wafer and one on the backside. The front side masks are level: 1 Anchor and level 2: Flap. The backside mask is Holes. Backside alignment was achieved by placing shims between the Anchor and Holes masks, aligning the two masks to each other, and clamping them together. A double-sided polished wafer was resist coated on both sides and slipped between the two masks. Both sides were exposed using a flood exposure from a broadband mask aligner. The backside holes were masked by thermal oxide and etched using a 40% weight heated KOH solution. The wafers were diced and the valves were released.

I. INTRODUCTION

The advent of the microchip has made possible the physical reduction of almost every electronic device that followed. Through MEMS technology, mechanical devices are also being reduced in physical dimensions. Some of the most common MEMS devices range from accelerometers that deploy automobile airbags to gas flow and pressure sensors with a wide range of applications. Mechanical valves are essential parts of pumping systems that permit flow in only one direction. A simple mechanical flap valve is a device that allows flow (liquid or gas) in only one direction. Using bulk micromachining techniques, it is possible to fabricate a miniature version of this device. It would consist of a polysilicon flapper over a hole in the silicon. The hole sizes will be on the order of tens of microns and the same flow principles would apply as in the macro-sized device. The valve can be modeled as an orifice flowmeter allowing theoretical flowrate calculations to be made.

An ideal application for this device is in micro pumping systems.

II. THEORETICAL MODEL

Flow through the valve would be most similar to flow through an orifice, which is governed by the following equation.

$$Q = C_f A_o \sqrt{\frac{2\Delta P}{\rho}} \quad (1)$$

Where A_o is the area of region 1 in figure 1, ΔP is the pressure difference between regions 1 and 2, ρ is the mass density of the fluid or gas, and C_f is the flow coefficient. C_f is experimentally determined and ranges from 0.6 to 0.9 for most orifices.

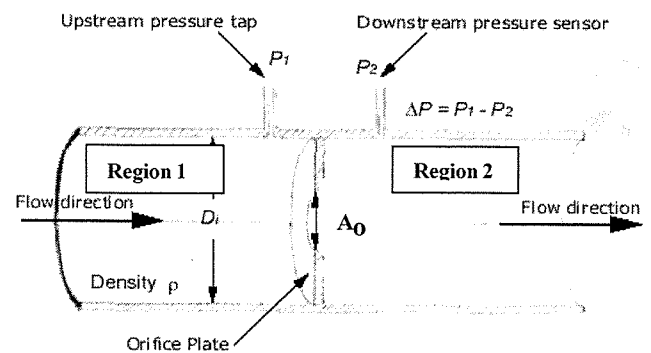


Figure1: Diagram that illustrates the parameters involved in determining flowrate.

For this model, the valve will be oriented such that the back of the valve is toward region 1 in figure 1. The flap will partially obstruct flow, but it will be analogous to a sheet of paper over a hole and its effects on flow in the forward direction are negligible.

III. DESIGN

The flap will be approximately $2\mu\text{m}$ above the silicon and $2\mu\text{m}$ thick. When air pressure is applied to the backside, the flexible flap will bend up and allow airflow. When air pressure is applied from top surface, the flap bends down and closes the hole thus preventing airflow (see figure 2). Since the flap is intended to bend with operation, the effects of stress must be taken into account. The maximum stress on the flap will occur at the corner where it bends. The yield strength for polysilicon is about 1.2×10^6 Pascal. This value will be used as the upper pressure limit in equation (1) to estimate a theoretical maximum flowrate.

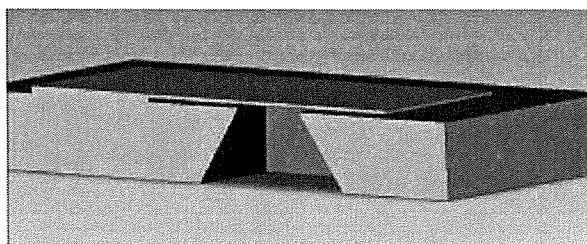


Figure 2: 3D cross sectional view of conceptual valve.

The design consists of three mask layers: Anchor and Flap (Front) and Holes (Back). It was decided to design for 1X masks because stepper systems often have Depth Of Focus issues when having to expose wafers with several microns of topography, as will be the case here. Thick films also cause stress on the wafer resulting in a deformed "potato chip" shape that makes it difficult for the stepper's vacuum chuck to handle.

The through holes will be etched using a heated Potassium Hydroxide (KOH) solution. Assuming (100) wafers are used, KOH etches silicon along the (111) plane at a 54.7° angle to the surface. Given this angle and the wafer thickness, basic trigonometry was used to calculate the required hole size on the backside of the wafer to obtain the desired hole size on the front of the wafer. The design allows for four valve array types each with a different hole size ranging from $25\mu\text{m} \times 25\mu\text{m}$ to $100\mu\text{m} \times 100\mu\text{m}$. The flap in each design completely covers the hole with an overlap of $75\mu\text{m}$. Top view schematics of the array and individual valve are shown in figures 3 and 4 respectively.

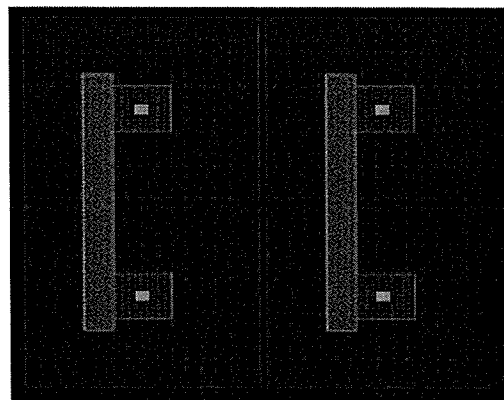


Figure 3: Mentor Graphics layout of valve array.

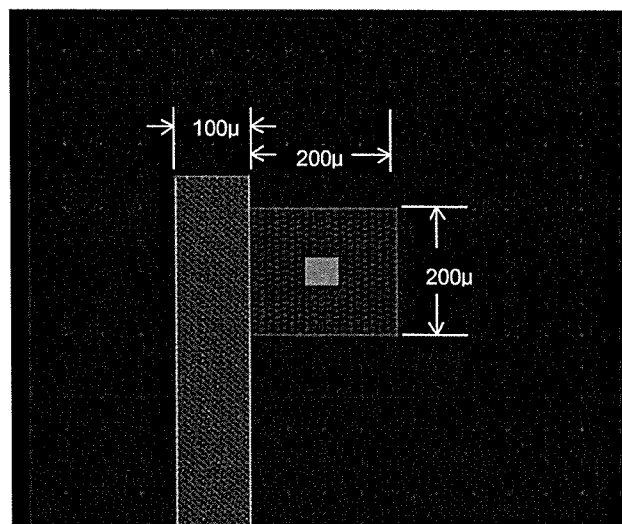


Figure 4: Individual valve dimensions.

Packaging consists of bonding a 4mm tube to each side of the die completely enclosing the valve array and holes. One end of the tube will be placed in an inverted, water filled, graduated cylinder. As air is forced through the valve and into the cylinder, water will be displaced. The flowrate will be the displaced liquid volume per unit time. The tubes will then be switched and the test performed again.

IV. PROCEDURE

Double sided wafers were required for this project but none were available so CMP was performed to polish the backside of the process wafers. The lot was washed and an RCA clean was performed before an oxidation step. The desired thickness was $3\mu\text{m}$ of oxide but recipe 430 on Bruce furnace yielded $2.5\mu\text{m}$ of thermal oxide. Next the wafers were coated on both sides with Shipley 1812 photoresist. All resist coating was done using the hand spinner and all development was done manually. To pattern the oxide, first level and backside lithography was performed by aligning those two masks to each other, clamping two ends together, slipping the wafer in between and flood exposing on the Karl Suss mask aligner. The oxide was then etched and an RCA clean was performed before depositing $2\mu\text{m}$ of polysilicon via LPCVD. Assuming a deposition rate of $235\text{\AA}/\text{min}$ the run was done for the time needed to obtain $2\mu\text{m}$ of poly. A groove and stain was done on a control wader after the poly deposition. Only $1.8\mu\text{m}$ of poly was deposited.

Next, the front sides of the wafers were doped n-type using spin on dopant N-250 and placed in Bruce furnace tube 3 running recipe 115. This was done to relieve stress from the film that might have occurred during deposition. The spin on glass was removed using a buffered oxide etch and a sheet resistance of 14 points per wafer was measured on the ResMap. The average measurement was around $33\Omega/\square$. The backside poly was then removed using the LAM490. About $7\mu\text{m}$ of AZ9260 was coated on the front side and second level lithography was done using the Karl Suss Mask Aligner. With such a thick masking layer, the front side poly was patterned on the LAM490 without having to worry about over etching. Recipe 4inPoly was used for the poly etch.

A diamond like carbon film was deposited on the front side of the wafers using PECVD on the Drytech Quad. The recipe requires 45 sccm of CH_4 at a pressure of 50mTorr and a power of 200 Watts. Next, the through holes were etched in a 40% wt KOH solution heated to 72 degrees. These conditions result in a silicon etch rate of $40\mu\text{m}/\text{hr}$ and an oxide etch rate of $0.2\mu\text{m}/\text{hr}$ [4]. The wafers were etched for 12 hours and carbon film was removed with an O_2 plasma using the LAM490. Finally the release was done in BOE for 4 hours. Figures 5a and 5b summarize the process steps discussed above.

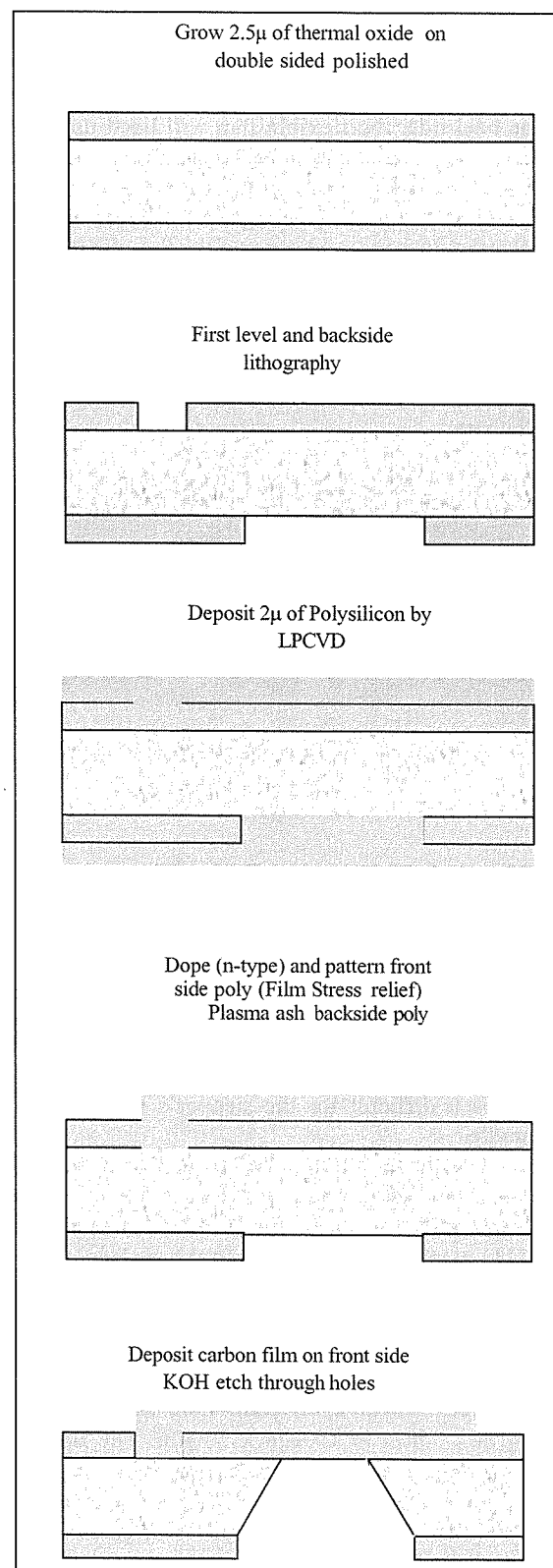


Figure 5a: Process Flow

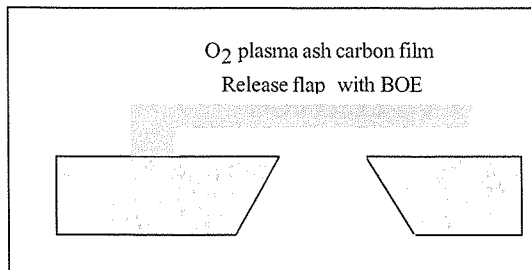


Figure 5b: Process Flow

V. RESULTS & DISCUSSION

Several issues occurred during the KOH etch that made it impossible to test the devices. The first problem occurred when the KOH solution undercut the oxide etch mask separating the holes in the array. This resulted in one large hole being etched to the surface. The partial merging of the etch holes is illustrated in Figure 6. The second problem was that adhesion issues with the carbon film resulted in the front side poly on some wafers being etched away.

A greater separation distance between the holes may have prevented the etch mask undercut. Using a nitride film as an etch mask would have been better since nitride has a very low etch rate in KOH on the order of angstroms per hour. The down side to using nitride is having to incorporate additional process steps.

An improved process would involve the through etch being done with a deep trench plasma etcher. It would offer the following benefits over the KOH etch:

1. Significantly shorter etch time
2. Greater packing density
3. More control over through hole size
4. Avoid need to align to cryptographic planes
5. Avoid need for backside alignment if holes are etched first

This improvement would require a redesign of the photo masks. The front side masks could still be used but the holes mask will have significantly smaller openings.

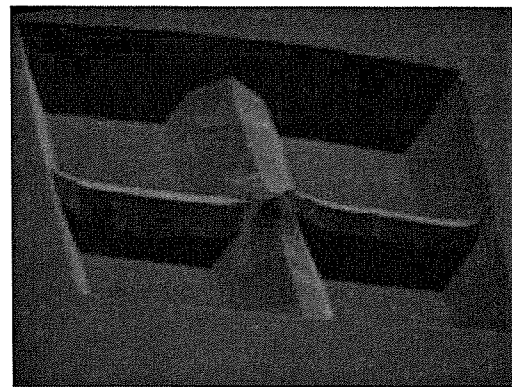


Figure 6: SEM showing etch mask undercut.

VI. CONCLUSION

Key flaws with the valve design came to light after the KOH etch. Had a nitride mask layer and greater hole separation distance been used in the project, it might have been successful. A complete redesign for a deep trench etcher would also significantly reduce processing time. This would give the flexibility to make changes to the planned procedure if unforeseen problems arise.

VII. ACKNOWLEDGEMENTS

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VIII. REFERENCES

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