Silica Waveguide Design and Fabrication using Integrated Optics: A Link to Optical VLSI Photonics Integration for Semiconductor Technology

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Abstract – The hardmask NiCr, has shown to be the optimum alloy in reducing sidewall roughness (SWR) in planar waveguide geometries. Within this study, the NiCr hardmask has been demonstrated using a lift-off of NiCr. In comparison, a NiCr etchant from Transene™ is used to compare how well sidewall roughness is reduced, and how the RIE - CHF_3/O_2 gas mixture improved anisotropy. From the results obtained, NiCr is a robust material that reduces sidewall roughness, and is the best metal to use, with the least amount of transferred striations. The CHF_3/CF_4 gas mixture in the AME -P5000 RIE tool proved to have better anisotropy and selectivity with respect to TEOS/Si_3N_4/Thermal Oxide {5000 Å/ layer} respectively.

Index Terms – NiCr hardmask, SWR, planar waveguide geometries.

I. INTRODUCTION

Intergrated optics are widely research for military and communications applications. Hybrid devices in optoelectronics have improved the versatility of what can be designed, and fabricated all in one intra-chip application. As indicated by the 2003 ITRS roadmap, one major limitation to the speed of CMOS devices is capacitive coupling due to interconnects [4]. Photonic devices integrated onto silicon substrates are one means of alleviating this problem. For example, optical interconnects pass through free space at a much higher rate than traditional interconnects.

In order for a waveguide to be practical, the signal attenuation or optical loss must be engineered to a value below 1 dB/cm. The primary source of loss in waveguides stems from light scattering due to sidewall roughness of the waveguide. Even a sidewall roughness of 50 nm can result in high loss. For this reason, the targeted sidewall roughness is < 10 nm. This paper will explain the mechanisms underlying sidewall roughness. The particular Si-compatible structure examined herein will be an oxide/nitride/oxide structure.

II. THEORY

A) Electromagnetic Principles of Optical Waveguide Theory

The basic idea of a waveguide is a media configuration that guides electromagnetic waves through a fixed path. In particular, the guides that are of interest in this project pertain to "closed waveguides".

B) Waveguide Geometries and Media Configurations

The geometries that will be designed for the project at hand are the following:

(a) straight waveguides
(b) bended Waveguides
(c) tapered waveguides

Straight waveguides can be represented in a Cartesian (x,y,z) coordinate system. A cross-section of a basic planar guide can be represented in the following figure implementing the [$SiO_2/Si_3N_4/SiO_2$/Si (substrate)] configuration illustrated in Fig. 1.

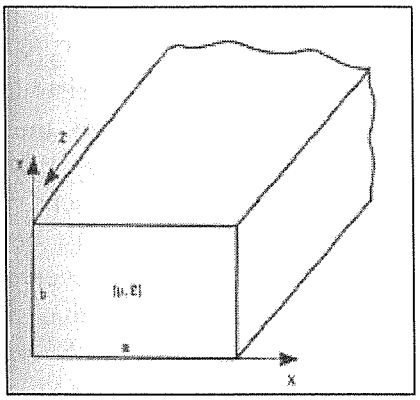

Figure 3: Rectangular/Straight Waveguide [14]

The core and cladding layers will give appropriate scatter ratio to release an effective index of refraction difference Δn. The actual index of refraction values for proposed media via experimentation is:

Actual Material Properties for Silica Waveguide Materials		
Materials	n (index of refraction)	Melting Point [oC]
Si	3.42	1410
SiO2	1.46	1700
Si3N4	2.00	1900

To better understand this concept, the nitride layer shall carry most of the photonic density. At the same time, the oxide layers will confine the light in the nitride, as well as the air interfaces on both sides of the strip. The interface should give a relatively high index between 0.1-0.5.

Further process planning and troubleshooting should give a starting point to optimizing an etch process.

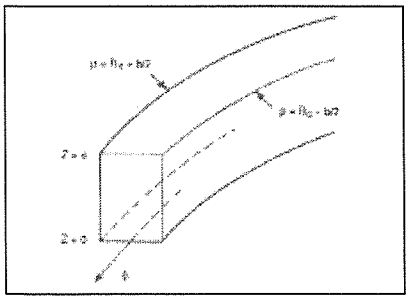

Figure 2 Bended Waveguide Configuration [14]

Looking at the bend in Figure 2, it must be said that the internal reflection of a straight waveguide is disproportioned by a radial dependence. On the other hand, a tapered waveguide is a fan shaped guide that takes either a large or small density of light and outputs smaller or larger light propagation respectively.

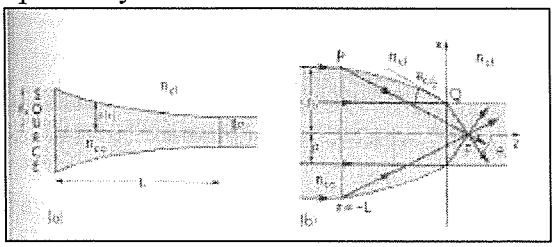

Figure 3: (a) Gradual varying taper (b) Parabolic taper [14]

III. EXPERIMENT

The design parameters at hand depend on the refractive index difference at the oxide / nitride interface. One wants to ensure that there is no oxy-nitride interface that will cause the light to flood into the oxide boundaries. Therefore, there must be satisfactory process control for this. Another issue, perhaps the most influential, is the line-edge roughness of the waveguides. In order for the guides to work at all, the sides have to be extremely smooth. A very careful etch process must be made to minimize roughness at all costs. In order to pattern these waveguide structures, there has been a recommendation of a "lift-off" process [1]. The end product should allow clean sides of the guide regardless of its geometry.

The issue in Figure 4, pertained to the particular etch mask used, resist material, or even the gas composition used in the RIE process. These are part of the fabrication process needed to successfully

fabricate a working waveguide as mentioned briefly in earlier parts of this proposal.

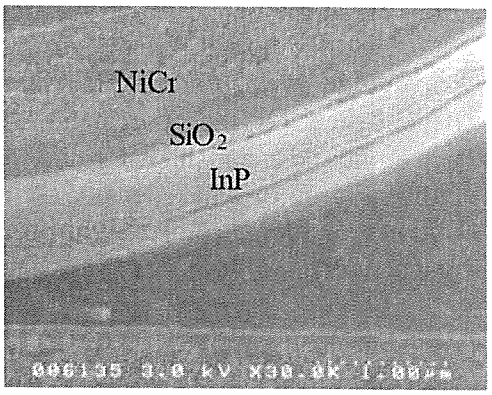

Figure 4: NiCr etch mask used to obtain clean sides [1]

The sidewall roughness of a waveguide must be < 10 nm for this application. In particular, Figure 4 uses InP and InGasAsP materials for the bended waveguide fabrication. Also, it is important to mention that NiCr was chosen due to small grain boundary size.

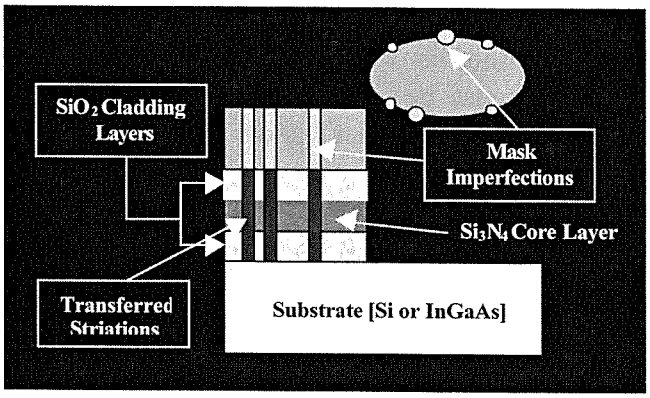

Figure 5: "Shower Curtain Effect" : roughness in the mask transfers to the underlying layer. [1]

A) Waveguide / Image Reversal & Lift-off Process Flow

1) 6" ASM LPCVD - 4" Blanket Depositions followed by manual dispensing of AZ5214E-IR resist on the SVG Track:

Several wafers were supplied by RIT SMFL for the project as N-Type <100> plane / ? = 10-15 Ω-cm resistivity. The earliest experiments involved the proper dose characterization of the polymer to enhance the lift-off phenomena. Before getting into this effect, it must be shown exactly what device wafers received what thickness of dielectric media. Blanket depositions of SiO_2 and Si_3N_4 were organized into a split order of:

Device Wafers	Waveguide Process Description
D1 - D4	Target Tx = 5000 Å - {TEOS/Si3N4/Wet Ox}
D4	Wafer taken from D1-D4 split for VASE Analysis / RIE DOE
D5 - D6	Tx = 1000 Å - {LTO/Si3N4/Bare Si}
D7 - D10	Tx = 1000 Å - {LTO/Si3N4/Wet Ox}

Figure 6 : Waveguide Process Split Description - Cladding / Core layer implementations

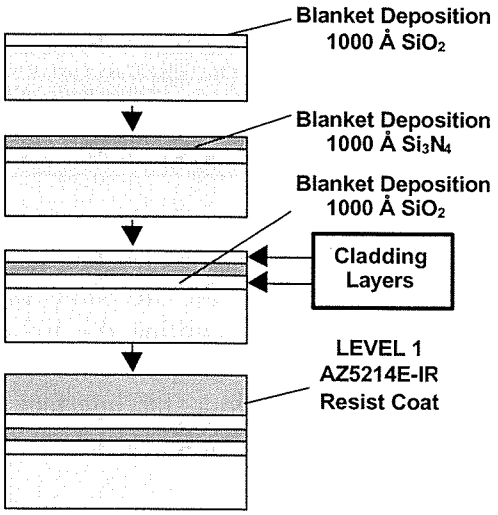

Figure 7: Blanket Deposition of Waveguide dielectrics. Top Layer SiO_2 cladding layer is 1000 Å LTO for wafers D5-D10. SMFL Factory Si_3N_4 is used as base core layer for all device wafers {D1-D10}. A table will be supplied for all thickness variations.

2) Waveguide VLSI g-line Photolithography

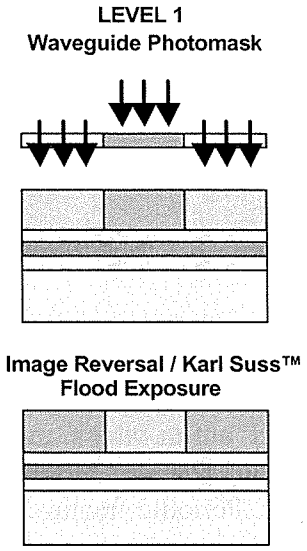

Figure 8: Level 1 g – line Photolithography using AZ5214E-IR resist. GCA g – line exposure time is t = 0.26 sec / 36.25 mJ/cm^2. Softbake temperature is 105°C / Post-Exposure Bake (PEB) is 120°C. Karl Suss™ flood exposure is 400 mJ/cm^2.

Figure 8 gives an accurate assessment of the original RIT SMFL Image Reversal & Lift-off process [2]. An 8 X 8 focus exposure matrix was performed using only 1-minute bake time (both softbake and PEB). The optimum exposure point was found to be 0.0375 sec.

3) Reticle design including geometric dimensions

The polygonal design needed to construct the waveguide reticle consists of L_{eff} varying from 1 – 10 μm. There are 3 vertical stacks at the top of the clear field as shown in Figure 9:

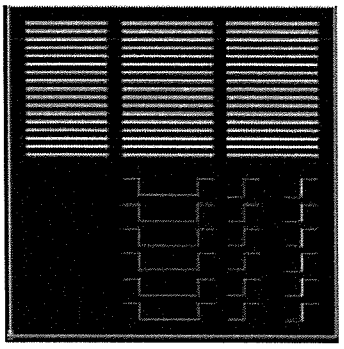

Figure 9: Waveguide Photomask - 20 X 20 um^2 Field Array – GCA Stepper Job: 690WAVE [4X4]

Within the three vertically stacked arrays, there are straight, bended, and tapered geometries. The widths of the straight layers (ΔL_{eff}) vary in a series of 0.2, 2.0 μm increments. Length of the taper fan-in/fan-out is 100 μm, followed by tapering lengths of 20 and 200 μm varieties that are then adjoined into a straight waveguide. In conjunction, the straight waveguide is merged into an identical fan-out taper at the opposing end.

4) NiCr Lift-off Integration

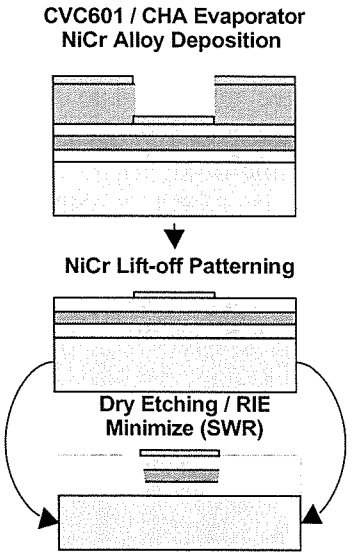

Figure 10 : NiCr Alloy Lift-off Integration

NiCr was sputtered using the CVC601. The chamber is arranged to hold multiple 4" or 6" substrate on a metal platen that is mounted on an axle that is controlled by

the rotostrate mechanism. In this regard, substrates could also be cleaved and taped on the aluminum dummy wafers face down on the platen hub. Teflon tape is used as an adhesive to bond the sample to the dummy wafer. A 4" NiCr Alloy {80 – 20 wt%; 0.25 in thick} was utilized. Since direct line-of-sight is used to avoid sidewall coating during sputtering, this allows the unwanted metal to dislocate around the transferred image (5X reduction).

Similarly, the CHA Evaporator is also exploited to do the same procedure. The metal alloy deposition has completely different physics involved to perform the comparison. A steel bell jar is used to harness the pressure to suspend the melted alloy droplets that propagate through the low pressure ambient. A tungsten boat is used to hold the NiCr pellet, and is tightened down between two electrodes, which will conduct current in a circuit. Importantly, the samples are to be mounted on additional 4" aluminum dummy wafers, and two metal rods are to be placed in parallel to hold the dummies flat directly above the evaporating source (direct line-of-sight).

IV. RESULTS AND DISCUSSION

After careful process optimization, lift-off of NiCr was successfully achieved (Fig. 11).

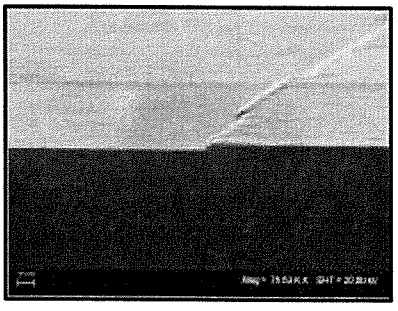

Figure 11: CVC601 Sputter Tool - T_X =700 Å @ 75.53 KX / Sputter Rate = 54.8 Å / sec

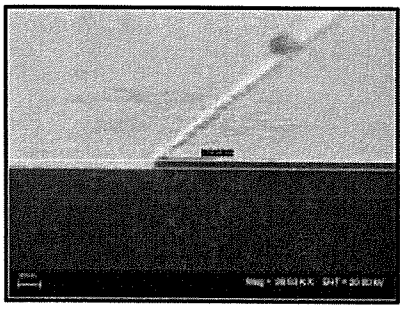

Figure 12: CVC601 Sputter Tool - T_X =750 Å @ 98.63 KX / Sputter Rate = 54.8Å / sec

Figures 11-12 denote some observable roughness at the edges. Some of the metal has truly experienced lift-off in some regions, but in others, there was some oval notching due to MEBES mask loading effects. Periodic fracture lines are apparent to where the sampled direct-write functions have merged the polygons that created the waveguide features (NWAVE690.gds file conversion). Since NiCr has a small grain boundary size, the reactive-ion etch (RIE) could be optimized to balance the surface roughness in many regions. Now that nickel chrome (80 – 20 wt %) has been developed for RIE, other hardmasks such as Cu and Al will be compared to the preceding results.

The result from Figure 11 ensures that planar waveguides can be fabricated in the cleanroom without any residual layers forming in the ASM 6" LPCVD tube furnace. If also available, the PECVD chamber in the AME – P5000 tool, could yield better film uniformity for additional comparison.

The reactive ion etch performed for sample dies cleaved from D7 were sputtered with 1000 Å of NiCr alloy that was subsequently lifted off.

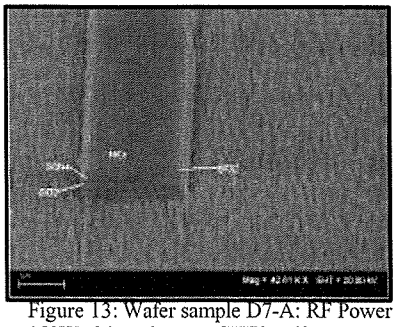

Figure 13: Wafer sample D7-A: RF Power = 150W, O2 – 10 sccm, CHF3 – 60 sccm, Pressure – 35 mTorr

In Figure 13, we can see that the micrograph shows that significant roughness has transferred from the NiCr hardmask (Lift-off). There is also some "grassy" polymer build-up around the perimeter. This situation is being caused by the CHF_3 / O_2 gas mixture being used,. It was determined that the Drytek Quad RIE had it limits to improving the etch selectivity of the dielectric layers. Sample D7-B was prepared with just O_2 increased to 20 sccm. No discernable improved was observed. Sidewall roughness ranged in between 50 – 100 nm range through the waveguide array.

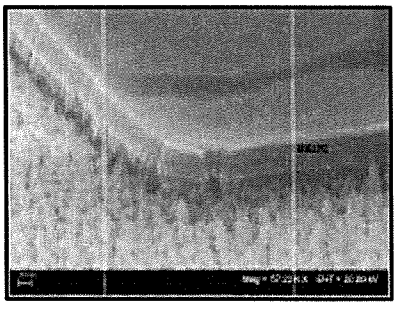

Figure 14: Wafer sample D7-B: RF Power = 150W, O2 – 20 sccm, CHF3 – 60 sccm, Pressure – 35 mTorr

G. Etching of ONO dielectric stacks. AME P-5000 RIE (Wafer D2 – whole 4" substrate).

The following comparison was done using Transene™ NiCr TFN etchant that has an Etch Rate = 50 Å/sec @ 40°C. A hotplate (Dataplate™ – Digital Hotplate Stirrer) was used to heat up the solution, and then the wafer was inserted for about 10 seconds after removing the thermometer. Subsequently, wafer D2 was transported to the AME-P5000 to perform another etch selectivity experiment. The nitride etch rate used was 1700 Å / min, and the TEOS etch rate was set for 1000 Å / min. The underlying thermal oxide layer suffered the image transfer, because there was no etch process available for that layer. Therefore, the TEOS recipe was used to etch the rest of the stack down to silicon.

Figure 15: Wafer D2: AME P-5000 RF Power = 500 W, CF_4 – 20 sccm, CHF_3 – 40 sccm, Pressure – 250 mTorr, B Field – 100 Gauss

Finally, Figure 15 depicts that there is substantial polymer buildup around the feature. Anisotropy is greatly improved, but much work is needed to optimize a custom recipe. The AME P-5000 is a promising alternative to using the Drytek Quad tool. Contamination could also be present due to the fact that the chambers need longer seasoning in between recipes. It is also important to note that there is no O_2 line that goes into the tool. This could also be a useful upgrade to enhance RIE performance.

V. CONCLUSION

Anisotroipc etching of $SiO_2/Si_3N_4/SiO_2$ waveguides was successfully demonstrated. The etch mask, NiCr, was also found to successfully lift-off via AZ5214E resist when a line-of-sight deposition was performed. The resulting

sidewall roughness was on the order of 50-100 nm. Further work must be performed to limit the effects of micromasking due to polymer deposition on the substrate during etching.

VII. ACKNOWLEDGMENTS

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[18] Slides borrowed from Sean Rommel from ECE Illinois /Sarnoff Corp., **1.** Choices for masking materials **2.** Mask Erosion **3.** The "Shower Curtain Effect"

[19] VASE™ analysis was performed by Jianming Zhou

Anthony G. Navarro (S'02) is originally from Basque-Cuban origin, and was born in Rahway, N.J in 1979. His ultimate drive is to become a research scientist in nanophotonic interconnect embedded in semiconductor nanosystems. A former research internship has been performed in the Department of Electrical Engineering in Rochester Institute of Technology, and also an internship in Integration Engineering at National Semiconductor in South Portland, Maine. He has received a B.S. in Microelectronic Engineering in May 2004 at Rochester Institute of Technology. Current prospects involve completing an M.S. degree in Imaging Science there also.