Face-to-Face Die Bonding and Direct Interconnects

Jeffrey A. Steinfeldt

Abstract—**In this investigation and process development project, a novel method for directly connecting two computer chips together, both electrically and physically was developed. This process utilized several processes and materials that are already used in semiconductor manufacturing and packaging. By using these common materials and processes, it simplifies the implementation of the process, and removes several potential roadblocks. It was found that two chips could successfully be bonded together physically and connected electrically.**

Index Terms—**Bonding, Chip Bonding, Copper, Interconnect, Solder Sphere,**

I. Introduction

In order to improve performance of high-end microprocessors, it will become necessary to target power consumption more intelligently, reduce the length of interconnects between sections of the microprocessor, and develop methods to make the manufacturing process more robust to transistor failures. By fabricating different subsystems of the chip individually, leakage can be targeted separately for each component. Individual sections, which are defective, such as SRAM, can simply be discarded without an entire processor being rejected. By then assembling the subcomponents using face-to-face connections, shorter path lengths with lower resistance and capacitance can be achieved, resulting in a three-pronged performance gain.

In this investigation, a novel chip to chip interconnect process was designed, fabricated and tested – direct, face-to-face chip interconnect without through-wafer etching. The connection is made between two copper interconnect layers which are standard in all high-end microprocessors. The process used many materials that are common to semiconductor packaging, and as such, are highly available. The interconnect layer makes use of a thick layer of negative photoresist in which a pad is exposed. The pad is then filled with solder, which is placed through standard solder sphere placement methods. A second chip is then mounted on top with a complimentary process. Additional investigation was made into alternative methods of connecting die without sacrificing packing density or requiring drastically different layout methodology.

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II. Process Development and Design

A. Process Development

Each process step was developed in sequence, as the wafer progress through the line. When there were holdups, such as tools being down, process development was initiated on dummy wafers. Dummy wafers were also used for development of SU-8 coating, as no reclaim was possible. The key to this project was the process integration, which required in-situ analysis and process modification. When tool and facility issues required a deviation from the intended process, results that are "close enough" were accepted, to limit the scope of the project. An example of "close enough" was that copper polish was not possible, a wet etch process for copper was used. In the case of the wet etch, there was an over etch, as CD variation is not critical. Wafers were left behind at key process steps as backups and for process refinement. The design of the two chips allowed for a pair of die to be fabricated, diced, and then flipped, creating a functional pair that enabled a multitude of tests. Different test structures were included to verify electrical characteristics, reliability and manufacturability.

B. Chip Design

Test Chip A (Figure 1) has 2 sets of Cross Bridge Kelvin Resistors to allow for contact resistance measurements, a densely packed cluster of interconnects with the ability to test 64 consecutive interconnects, 32 interconnects, or 16 interconnects, as well as 4 isolated interconnect test structures.

Test Chip B (Figure 2) has the same dense interconnect structure; with the ability to test interconnect chains of the following lengths; 2, 4, 10, 12, 14, 16, 32, and 48. Test Chip B also has the 4 isolated structures seen on Test Chip A.

By flipping chip B horizontally, rotating 180 degrees, and

aligning them with the verniers on each edge the two chips can be bonded together, creating the interconnects between the pair of chips (Figure 3).

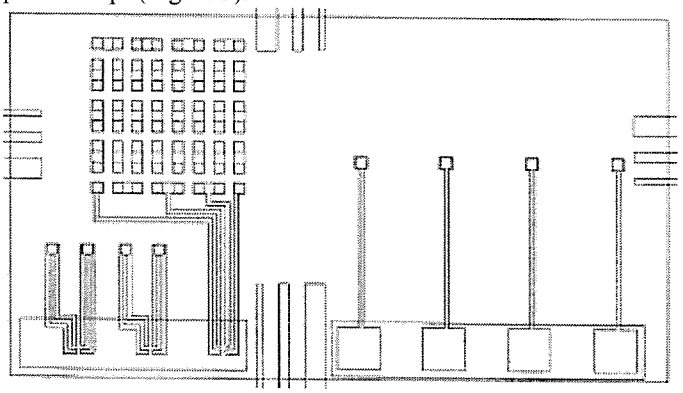

Figure 1: Test Chip A.

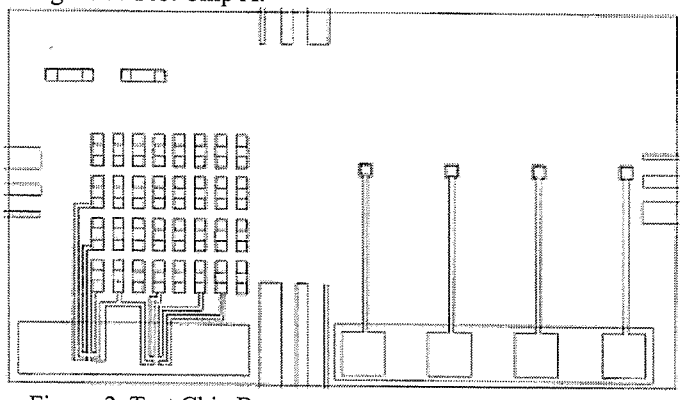

Figure 2: Test Chip B.

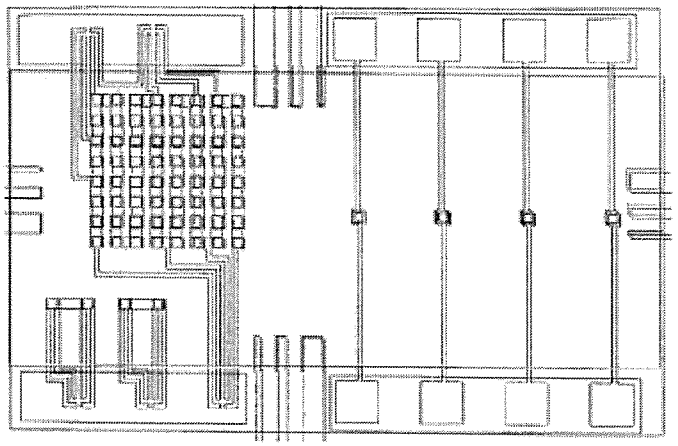

Figure 3: Test Chips A and B aligned.

C. Process Flow

The process that was finally used was based on available equipment, materials and processes. Starting from a bare silicon substrate, silicon dioxide was grown using a wet thermal oxidation process. Ideally, a high quality, low temperature oxide would be deposited, as would be the case in a high-end microprocessor, but this process was not available until after it was needed. Copper was then sputtered onto the oxide. Ideally a damascene process would be used instead, however disposal of copper contaminated slurry was not a feasible option.

The wafers were then coated with Shipley 812 photoresist and patterned using a one-to-one contact aligner. The copper was etched using a wet etch solution of DI water, Hydrogen Peroxide, and Sulfuric Acid. The etch chemistry quickly etched copper by converting it from solid copper into a solution of copper sulfate. The photoresist was stripped using acetone and isopropyl alcohol, followed by a DI water rinse. See Figure 4 for cross section.

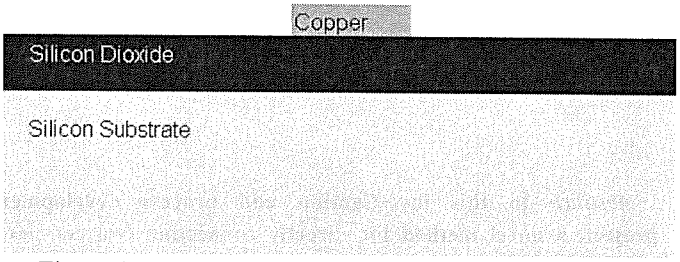

Figure 4: Cross section after copper etch.

The wafers were heated on a hot plate to drive off any water and then coated with SU-8 2050 using a low spin speed to achieve the desired thickness. The SU-8 requires long bake steps in order to remove solvents, which make the resist tacky. Allowing the wafers to cool and finish drying after the bake was complete also assisted in reducing the tackiness of the film. The SU-8 was patterned, also using contact printing. The resist was then baked in order to allow cross-linking and then developed. A hard bake was performed to strengthen the resist. The processing of SU-8 was based on the material brochure provided by the manufacturer. See Figure 5 for cross section.

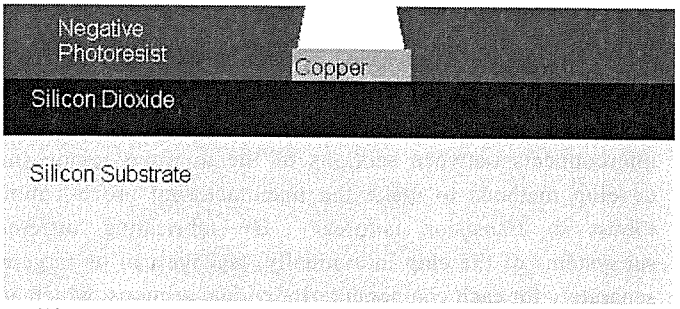

Figure 5: Cross section after SU-8 processing.

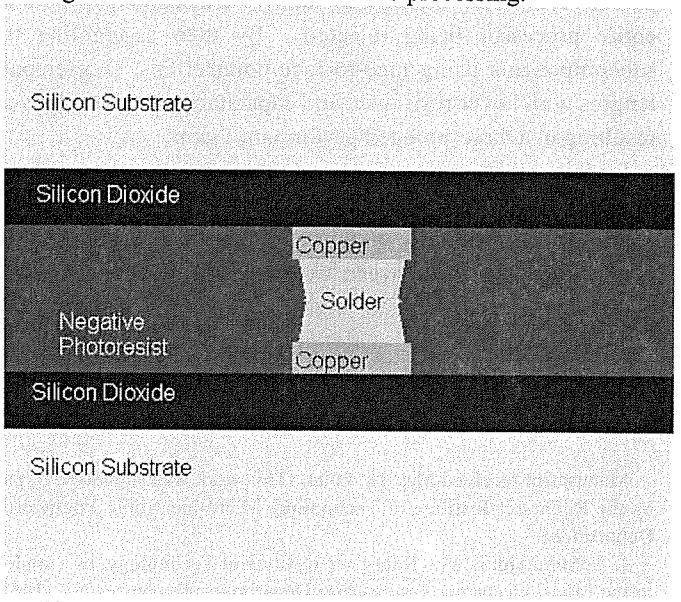

Figure 6: Final cross section.

The wafers were then diced using a wafer saw, followed by a cleaning process and a removal of the protective tapes. The chips were then individually processed, applying solder spheres and heating. The second chip was then placed on top, both chips were heated and force was applied to achieve better contact. This process connected the two chips, both electrically and structurally. See Figure 6 for cross section.

III. RESULTS

Each process was successfully developed and processed in sequence. There was significant yield loss from SU-8 adhesion issues and solder sphere placement. While bonding was proven, the electrical connection on the device chips could not be verified due to an insolating layer over E-test pads. The insulating layer was most likely due to copper oxidation. In order to prevent this, all thermal processing after SU-8 development would need to be preformed in an inert ambient. It was proven experimentally that a copper film, heated in an ambient containing oxygen and water would become insulating.

IV. CONCLUSION

If further work is to be done in this area, there are several ways to improve the processes. Some were not used due to time and financial limitations. Such improvements include developing some sort of method to align the chips. This could be accomplished easily through modification of a microscope stage, as it has control over the x-axis, y-axis, z-axis and theta-axis. A robust stage could also apply the force needed to bond the chips. This system would need to be contained within a simple environmental chamber that could be filled with nitrogen as an ambient, using a simple hotplate for heating the chips.

Film adhesion could also have stood some improvement. The copper adhesion to oxide was poor, but strong enough. This could have been improved though an adhesion layer, however the etch process would have been more complicated. Ideally, TaN would be used with a CMP process, removing the need to etch two metals. The adhesion of the SU-8 to the oxide proved to be an issue that could keep this process out of manufacturing. The adhesion could be improved through further investigation. The limitation to investigating the adhesion failure is that it is not apparent until after wafer dicing, creating a slow feedback loop.

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REFERENCES

[1] 200 mm Wafer Bonding for 3-D Interconnects Using Low-K Dielectrics as Bonding Glue, in Seventh International Conference on Dielectrics and Conductors for ULSI Multilevel Interconnection (DCMIC), pp. 59-56, March 5, 2001, Santa Clara, CA, with J.-Q Lu, Y. Kwon, R.P. Kraft, R.J Gutmann, J.F. McDonald, and T.S. Cale.

[2] Design and Fabrication of Damascene Patterned Interconnections for Face-to-Face Wafer Bonded 3D-Stacked IC Test Structures, 18th International VLSI Multilevel Interconnection (VMIC) Conference, Sept. 2001, invited with J.-Q. Lu, R.P. Kraft, O. Erdogan, Y. Kwon, P. Belemjian, G. Rajagopalan, M. Gupta, J.M. McMahon, J. Mayega, D.-L. Bae, C.K. Hong, T.S. Cale, invited.

[3] Fabrication of Via-Chain Test Structures for 3D IC Technology Using Dielectric Bonding on 200 mm Wafers, to be published in Materials Research Society Digest in 2002, with J.-Q Lu, Y. Kwon, G. Rajagopalan, M. Gupta, D.-L. Bae, J McMahon, C.K. Hong, R.P. Kraft, O. Erdogan, P.M. Belemjian, J.F. McDonald, T.S. Cale, E. Eisenbraun, B. Xu, J. Castracane, and A.Kaloyeros.

[4] Wafer Level 3D Hyper-Integration, 20th International VLSI Multilevel Interconnection (VMIC) Conference, Sept. 2003, invited with J.-Q. Lu, Y. Kwon, J.J. McMahon, A. Jindal, B. Altemus, D. Cheng, E. Eisenbraun, T.S. Cale, R. J. Gutmann invited.

Jeffrey A. Steinfeldt will graduate from the Microelectronic Engineering Department at Rochester Institute of Technology in May of 2004. J. A. Steinfeldt has accepted a full time job with Intel Corporation in New Mexico. J. A. Steinfeldt completed all of his co-op requirements with Intel Massachusetts, a wholly owned subsidiary of Intel Corporation.