Implementation of Backside Vias as an Alternative to Wafer Thinning

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Abstract—**A study has been performed to determine the viability of Potassium hydroxide (KOH) as a wet etchant to create backside vias to devices previously manufactured on thinned wafers. In order to protect frontside devices in the back end of line process, the KOH must not come in contact with the front of the wafer. A number of methods have been investigated with the advantage being in the use of a coat of black wax. This paper will present results obtained from tests with black wax as well as provide insight to the advantages and disadvantages of other protection options.**

Keywords— **backside via, black wax, $R_{ds(on)}$, Potassium hydroxide (KOH)**

I. INTRODUCTION

Each new generation of electronic devices are designed to be smaller, faster, and consume less power. By reducing the overall height of a vertical discrete power device, a lower on-state resistance can be achieved. This directly translates to an increased battery life and reduced internal heating.

One solution is to thin the entire wafer in a back end of line process by using mechanical methods. While a valid solution, this compromises the ability of the wafer to be handled because thin wafers become very brittle and can warp and sag. A Potassium Hydroxide (KOH) etch is being considered as an alternative in creating very deep (~300μm) vias. The advantages of using this wet etch process is fast etch rates (~1μm/min) and uniformity across the wafer. Using nitride as an etch mask provides very high selectivity. The major challenge in using a KOH etchant is to eliminate the chance of positive ion contamination into the oxide of the previously fabricated device, thus modifying the operating characteristics and potentially pushing the device to failure.

KOH has been determined to provide sufficient etch profiles and LPCVD nitride has been shown to act as a sufficient etch mask. A number of methods to protect front-side devices such as fitted holders, masking tapes, and black wax have been investigated.

II. THEORY

In any electrical device, each material, barrier, region, etc. in the conduction path of a device will contribute to the overall series resistance of the device. By lowering this resistance contribution, devices can be designed to consume less power and operate cooler due to a reduction in internal heating. This is also described as lowering the on state resistance $R_{ds(on)}$.

Figure 1 illustrates the regions of a generic vertical device. Note the individual resistance contribution of each region to the total series resistance. If some of these individual resistances can be reduced, that in turn will lower the total contribution and in effect lower $R_{ds(on)}$. It is possible that the contact metals could be replaced by less resistive alternatives, but this has the potential to limit current flow and cause devices to fail. Modifying the source or drain or channel would cause the electrical properties of the device to be modified, so this again is not desirable. That leaves only the substrate resistance to be modified and the easiest way of doing this is through reducing its thickness.

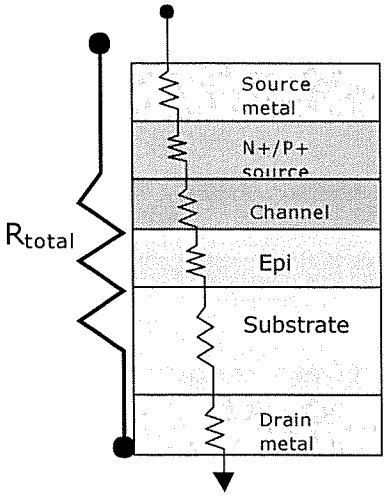

Fig. 1. Series resistance contribution in a generic vertical device.

In order to reduce this thickness a backside via etch in KOH etch has been proposed. KOH etches silicon relatively quickly along <111> planes, creating a 53° silicon etch angle. The concern of using KOH is that it has the potential to

contaminate previously fabricated devices. The positive ions contained in this solution have the potential to contaminate the gate oxide or wells of fabricated devices, thus shifting their electrical properties. Therefore a valid frontside protection method must be developed for this method to be introduced into a back end of line process.

III. Experiment

Previously manufactured 4-inch PMOS device wafers were obtained in order to test the viability of different frontside protection methods. The process steps of creating backside vias were divided between these device wafers and reclaimed scrap wafers so the fabricated devices would not be introduced to high temperature or plasma processing. All backside patterning and true via etching was done on scrap wafers, while the frontside protection was implemented on the PMOS wafers. Since the proposed process flow, as shown in figure 2 requires nitride as a KOH etch mask, actual vias could not be created because the high temperature LPCVD process would cause the Aluminum contact metal on the fabricated devices to melt, thus compromising the integrity of the working PMOS devices.

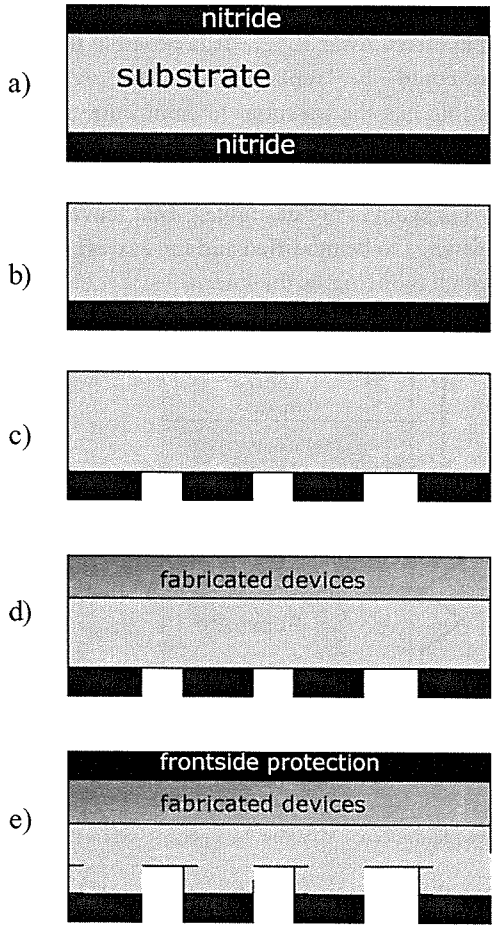

Fig. 2. Proposed process flow for integration of backside vias into production. a) deposit nitride b) blanket frontside etch c) pattern backside and etch nitride d) process as normal e)

A 1200Å LPCVD nitride was grown on a number of scrap wafers to act as an etch mask in the creation of backside vias. The backside of the wafers were coated with resist and then patterned with contact lithography using a Karl Suss MA150 contact printer. The patterned nitride was then dry etched in a Lam490 Auto Etch. The resist was removed and the wafers were etched in KOH while evaluating a number of frontside protection options as discussed below.

A. Protective Tapes

The viability of protective tapes was evaluated because of the ease of implementing this into a process flow. Masking the frontside of a wafer with tape will add little cycle time to the process and allow for wafers to be lot processed. A few different tapes including kapton, and wafer dicing tape were evaluated for their resistance to KOH.

B. Wafer Holder

The use of a stainless steel o-ring sealed wafer holder that had been developed for MEMS applications was also evaluated. By loading two wafers front-to-front into the apparatus and sealing, the fronts are protected, and the backsides exposed for the etch. This is a proven method, however, wafers can easily be broken when manually loaded into the holder and a single holder only allows two wafers to be processed at a time.

C. Black Wax

The third option that was evaluated was coating the front of the wafer with black wax. The in this experiment the wax was hand-painted onto the wafers by dissolving a small amount of the wax in Xylene, and then baking to remove the remaining solvent and to attempt to remove any pinholes in the coat. While this is a time-consuming process, the black wax could be further dissolved and spin-coated similar to a resist process.

IV. Results and Discussion

Figures 3 and 4 illustrate the profiles of a KOH etch. These were obtained by etching a scrap wafer for about an hour with only a few hundred Angstroms of LPCVD nitride used as an etch mask. This illustrates the very high selectivity of

KOH between nitride and silicon.

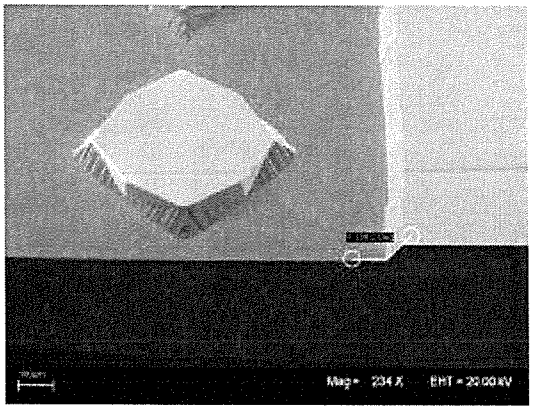

Fig. 3. Cross-sectional SEM view of KOH etch profile.

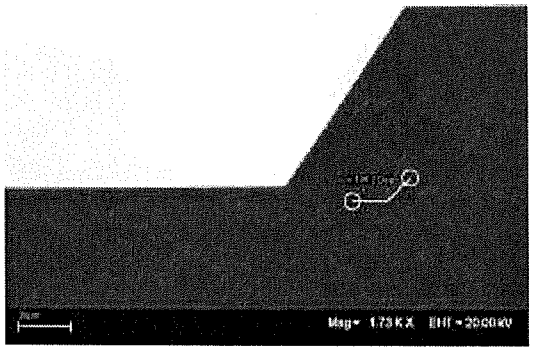

Fig. 4. Cross-sectional SEM view of KOH etch profile highlighting the etch angle.

Results from the backside etch of the patterned scrap wafers showed expected profiles with a silicon etch rate of around 1μm/min and a nitride etch rate of only about 50Å/hour. Using these rates, the 300μm targeted etch depth for incorporation into vertical devices will take somewhere around 5 hours and only around 250Å of masking nitride is required. Due to this long process time, it is very important that the frontside protection options allow for bulk wafer processing.

A. Protective Tapes

Mixed results were obtained from the attempt to use protective tapes. While the both the kapton and dicing tape held up to the KOH etch, there were adhesion issues with them sticking to the wafer. Shortly after introduced to the heated KOH bath, the tapes began to lift-off. With better selection of high-temperature adhesives or thicker tapes, this experiment may have produced better results. Therefore, this method should not be disregarded, but investigated further.

B. Wafer Holder

The wafer holder was shown to efficiently protect the frontside of the device, however, it was not used any further in this work because of the long loading times and its ability to only process two wafers at a time. This could be used as a valid option for a proof-of-concept, however, this solution could not be effectively implemented into manufacturing.

C. Black Wax

The best option for frontside protection was determined to be a coat of black wax. Figure 5 shows the ID-VG plot of a PMOS device measured before and after being exposed (with black wax protection) to a KOH etch. Note that there is no identifiable shift in the threshold voltage, indicating that the KOH did not contaminate the device.

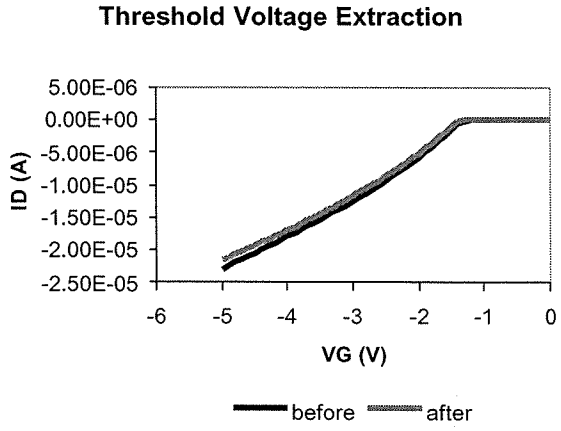

Fig. 5. PMOS threshold voltage measurement before and after exposure to KOH etch.

These results are very promising since they indicate that black wax sufficiently protects frontside devices from positive ion contamination when introduced to KOH. However, when the device wafer was etched in this experiment, nearly 75% of the devices were destroyed because the KOH was able to get beneath the black wax and attack the devices, namely the aluminum contacts. This can be attributed to problems with the hand coating of the black wax. Even though the wafers were baked after coat, some visible pinholes still remained in the wax coat. This allowed the enchant to get under the wax at various locations and destroy the devices.

In order to prevent this, better coating techniques need to be developed. It is possible that the black wax can be completely dissolved into a liquid form in order to allow the material to be spin-coated similar to resist. This will allow for extremely better uniformity and the ability to control thickness.

V. CONCLUSION

This study was successful in demonstrating the ability for black wax to sufficiently protect frontside devices. In areas where the black wax did not lift off, devices did not exhibit any shift in Vt, indicating that there was no positive ion contamination into the gate oxide or device wells resulting from exposure to the KOH etchant. Better coating techniques remain to be developed in order to uniformly protect the entire front surface area of each wafer during the wet backside etch. This technique should also be applied to a true vertical device so that the advantages in the creation of a backside via for thinning purposes can be quantified by electrical characterization.

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