Development of a Full Silicidation (FUSI) Process for Nickel Silicide

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Abstract-**Silicides have been long used to solve the problem of poly depletion effects in the CMOS circuits. The depletion layer in the poly-gates increases the total effective gate-dielectric thickness causing a poor device performance. Many advantages are promised in replacing the Polysilicon gates with metal gates, which include improved sheet resistance of the gates, decreased equivalent electrical thickness of gate dielectric by eliminating the Polysilicon gate depletion effect, and dual work functions, higher than n+ poly work function for NMOS and lower than p+ poly for PMOS in a single full Silicidation (FUSI) of Polysilicon gates. In the ever reducing gate dimension and junction depths, nickel Silicide has become one of the promising candidates for silicides applications in submicron CMOS devices. Nickel silicides has many advantages over other metal silicides due to its one step low temperature formation, low resistivity (14~20 $\mu\Omega cm$), low Si consumption, and its nature of not suffering from resistivity degradation on narrow lines or gates. However, nickel silicides have some problems associated with them such as the large junction leakage current and sheet resistance degradation due to oxygen contamination and rough interface between NiSi and Si. Nickel Silicide was formed on doped Polysilicon to simulate the effects on gate CMOS regions. Sheet resistance will be measured on silicided Polysilicon and results will be introduced in this report as well.**

Index terms-**Ni Silicidation, full Silicidation, metal gate, RTP**

1. Introduction

The Silicide process is defined by introducing metal into silicon, which has been used for a long time to overcome the high resistivity between metal and poly gates and source/drain regions in MOSFETs. Silicides are necessary in small devices that are limited in their performance by the resistance seen in source/drain and poly gates regions. Silicides are also necessary in dual gate devices because by replacing Polysilicon gate electrodes in MOSFETs with metal gates give the choice of work function allowing a higher work function than n+ poly work function for NMOS and a lower than p+ poly work function for PMOS, which would decrease the drive current loss due to mobility degradation and decrease the band to band tunneling across drain to body junction. Using metal gates offers many other advantages like lower gate resistivity, no boron penetration from Polysilicon gate into channel through very thin gate dielectrics as well as reduced electrical thickness of gate dielectric by eliminating depletion in doped Polysilicon gates. Silicides include two types in which they can be formed, the first Silicide is called Polycide process in which the Polysilicon is deposited, as well as the Silicide and both are then patterned, while in the

second process-Salicide-or better known as the self-aligned Silicide, the Polysilicon is deposited and patterned followed by a metal deposition then the Silicide is formed by thermal reaction.

There are different metals that can be used for silicides applications keeping in mind their different properties that contribute to weather the metal can be used or not, such as their Silicidation temperatures, etch capabilities, dominant diffused species, and resistivity. Some of the famous metals that have been used for silicides applications include Titanium Silicide ($TiSi_2$), Cobalt Silicide ($CoSi_2$), and Nickel Silicide (NiSi).

Titanium Silicide ($TiSi_2$) has been used for a long time in silicides technology, but begins to demonstrate limitations in the sub-250nm technology devices. Titanium silicides suffered from difficulties in forming the low-resistivity phase on narrow poly lines, as well as its silicon diffusion dominated formation of silicides leading to problems of bridging. Cobalt silicides ($CoSi_2$) has replaced titanium silicides around the 250nm technology node due to poly line-width problems associated with $TiSi_2$ discussed earlier and due to the fact that $CoSi_2$ does not suffer from narrow-line effects and bridging problems. $CoSi_2$ demonstrated better scalability for sub250nm nodes. However $CoSi_2$ started to have problems associated with it as the device dimensions are scaled down further, these problems include the difficulty associated in forming the low resistivity $CoSi_2$ on poly line-width less than 40nm. $CoSi_2$ also suffered from high sensitivity to ambient contamination as well as high consumption rate of silicon.

The nickel Silicide emerged as a prominent candidate for silicides applications for the sub-65nm advance technology devices. NiSi has many advantages over both titanium and cobalt silicides because of its low consumption rate of silicon, low resistivity reported to be in the range of 15~20 μOcm, and most importantly no suffering from narrow-line effects. NiSi formation process can be performed in a single step annealing forming the low resistivity NiSi phase followed by a selective etch removal of the unreacted nickel. This study will investigate the properties and formation of NiSi on doped Polysilicon to simulate the effects on gate CMOS regions. NiSi polycide is formed on a blanket Polysilicon film and then the polycide's sheet resistance is measured using the CDE Resistivity Mapper and compared to the sheet resistance of the doped poly before the Silicidation step to verify the formation of NiSi.

2. Theory

A. Nickel Silicide (NiSi) formation

The Silicidation process is usually performed by depositing some kind of metal such as tungsten, titanium, cobalt, or nickel on silicon followed by a rapid thermal reaction treatment creating a metal-semiconductor compound that have different properties depending on the processing conditions it has been through, and which have to be controlled and calibrated to get the desired end results. These conditions include the temperature at which the Silicidation step is done, surface and ambient contamination, and self-aligned Silicidation. The desired phase of nickel Silicide for this experiment was the nickel monosilicde (NiSi) which has been reported to form at temperatures around 500^0C allowing for a lower thermal budget. One thing that should be kept in mind when considering the Silicidation temperature, is the distinction of nickel Silicide phase being formed. At higher temperatures of 750^0C and above, another phase of nickel Silicide is formed-nickel diSilicide-($NiSi_2$), which has a higher resistivity than the NiSi reported to be around 50 μOcm^2 caused by silicon agglomeration in the NiSi film taking place at higher temperatures causing a serious degradation in the performance of the devices. Another important issue that must be closely monitored is the ambient contamination mainly silicon

oxides that can be grown on silicon as a native oxide or produced during the processing steps. Silicon oxides negatively affect the process of Silicidation by forming between the metal and the silicon interface allowing for a layer of SiO_2 to be formed on top of the Silicide, thus causing the formation of metal oxides and eventually preventing the Silicide process. This problem can be overcome by depositing a capping layer on top of the Silicide right after the deposition of the Silicide to prevent any growth of native oxide and can be easily removed with the unreacted nickel after the Silicidation reaction. As for the self-aligned Silicidation in nickel Silicidation process the nickel will only react with silicon where nickel and Polysilicon are in contact and as mentioned before the unreacted nickel along with any capping layers used will be etched using a Piranha etch H_2SO_4:H_2O_2 which does not effect any silicides formed.

B. Resistivity Measurements

The sheet resistance measurements is most crucial factor due to its importance in confirming the formation of nickel Silicide NiSi and comparing them to sheet resistance measurements taking after doping the Polysilicon. The technique that was used to determine the sheet resistance of the nickel Silicide NiSi film was by using the four-point probe technique where a current is run two outer probes and measure the resulting voltage between the two inner probes as shown in figure 1. Full wafer sheet resistance measurements were made possible by using the Creative Design Engineering (CDE) Automated Resistivity Mapper.

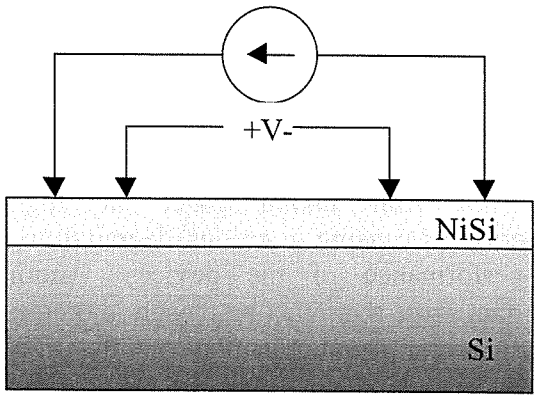

Figure 1: standard 4-point probe

The process was performed on 4" p-type <100> crystalline orientation silicon wafers with resistivity ranging from 1~25 O-cm. An RCA clean step was done to remove any contaminants. A layer of about 1000 A of oxide was then grown in the Bruce furnace using the factory recipe#350. The next step was to deposit about 2000 A of Polysilicon using the LPCVD and factory recipe#650 with a deposition rate of 200 A/min. doping of Polysilicon was done using the spin on doping method by spinning on N250 phosphorus dopant at 3000 rpm followed by a pre-bake at 200^0C for about 15 minutes followed by an anneal in Bruce furnace using factory recipe#120 at 1000^0C for about 15 minutes soak in N_2. Sheet resistance of the doped silicon was then measured as shown in table 1. The Polysilicon was then patterned using the CMOS Poly-gate mask and the G line lithography using the GCA 8000 with dose = 43.5 mJ/cm^2. A Dry etch step was done on the patterned samples using the Dry-Tech quad to etch the Polysilicon using the polyetch recipe. Resist was then stripped followed by an HF 50:1, 1 minute dip step to remove any native oxide that might have grown before the deposition of Ni followed by an SRD step. Nickel was then deposited on the samples by sputtering method using the CVC601 at a deposition rate of 1.52 A/sec with a target thickness of ~1000 A of Ni with base pressure of 1.9E-5 torr, and chamber pressure of 5.1 mtorr at 197.8 V and 0.75 A flowing Ar at 17 sccm. We also tried to evaporate Ni on some of the samples but turned out to be not a good idea to use a thermal evaporator with nickel because at different pressures the boat breaks before the Ni gets evaporated expect for one time where we were able to get a very thin layer of evaporated Ni ~400 A. The Silicidation step was done by a thermal reaction step using the RTP AG 410 at 550^0C for about 30 seconds. After the thermal reaction step, the unreacted nickel was then removed in a Piranha etch (H_2SO_4:H_2O_2 1:2) at 100^0C for about 3 minutes to remove all the unreacted Ni. The final step was to take sheet

resistance measurements on the samples using the CDE resistivity mapper.

4. Results and Discussion

Using the previously outlined process, sheet resistance on the nickel silicided NiSi samples were taken as shown in table 1 using the CDE resistivity mapper.

Poly Resistivity	NiSi Resistivity
Rs ohms/sq	Rs Ohms/sq
74.09	2.08
74.47	1.93
72.60	2.53
78.06	2.31
71.09	3.33
73.31	4.52
77.79	1.49
76.31	2.00
66.37	3.86
75.03	1.86
Ave = 73.91	**Ave** = 2.59

The Nickel Silicide resistivity was then calculated to verify the formation on NiSi:

Rho= Sheet resistance X NiSi Thickness
= 2.59 X 1200E-08
= 3.11 E-05 uOhms.cm

From the previous NiSi resistivity calculation we can see that the NiSi was formed successfully and that resistivity has dropped down significantly. To further invistage the formation of NiSi, SEM images were taking of the samples and in SEM#1 through SEM#3 we can see that there is a layer of oxide on top of silicon and another layer of NiSi on top of the oxide with a thickness of approximately 1200 A, and from the reported values of NiSi silicon consumption rates of about 1.83 A of silicon per A of metal and about 2.34 A of resulting Silicide thickness per A of metal, it appears that we have reacted about 938 A of Polysilicon with about 513 A of nickel Ni.

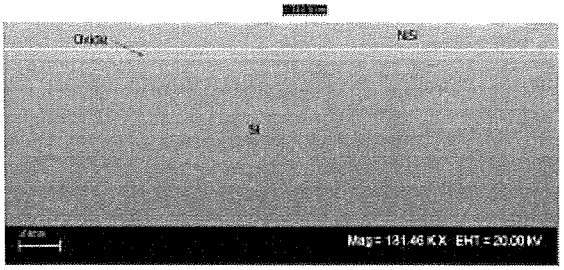

Figure 2: SEM#1 showing thickness of NiSi of about 1200A

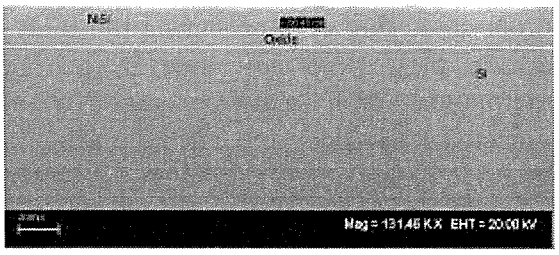

Figure 3: SEM#2 showing thickness of oxide thickness of about 600 A

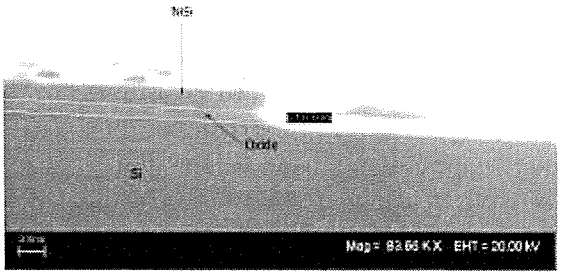

Figure 4: SEM#3 showing NiSi thickness on a patterned sample ~1200 A

$$Ni - Thickness = \frac{NiSi - Thickness}{Silicon - required - rate} = \frac{1200\ \overset{0}{A}}{2.34} \approx 513\ \overset{0}{A}.$$

ıt NiSi phases and determine sheet

$$Poly - reacted = (Ni - Thickness) \times (Poly - required - rate)$$

$$= \left(513\ \overset{0}{A}\right) \times (1.83) = 938\ \overset{0}{A}$$

The resistivity calculated previously for NiSi was about 31 μOcm, which about twice the reported value of resistivity for NiSi of 15 μOcm and that can be cause by couple of reasons including oxygen contamination during sputtering or even during the RTP step because they were not done in a vacuum environment, or it might be caused by some unreacted Polysilicon left after the Silicidation step.

5. Conclusion

This study was successful in forming NiSi that was formed on doped Polysilicon to simulate the effects on gates CMOS regions. In addition sheet resistance was measured using the CDE resistivity mapper and found that it was significantly decreased indicating the formation of NiSi. Further study may include verifying the conversion of Ni to NiSi by fully siliciding the poly, which has to be investigated using x-ray diffraction techniques. As well as varying RTP temperatures to look

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