Capacitance-Voltage Analysis of High-? Dielectric on Strained Silicon

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Abstract—**Device characteristics are reported on HfO_2 gate dielectrics deposited by atomic layer deposition (ALD), and jet vapor deposition (JVD) on strained-Si and bulk Si samples. Capacitance-Voltage (CV) analysis of samples shows comparable interface charge levels between strained-Si and bulk Si samples. A flat band shift of –0.5V was noted between the strained-Si and bulk Si for the JVD samples.**

Index Terms—**Capacitance Measurement, Hafnium, Strain**

I. Introduction

THE scaling of MOSFET devices has allowed for tremendous performance improvements in the semiconductor industry for years. However, with the current trends in scaling the use of a conventional Si-MOSFET will reach its limits by the year 2005 [1]. In order to reach the drive current necessary for the 90nm node a change in the conventional MOSFET structure will be needed. With the introduction of a strained-Si layer in the channel of the device a mobility enhancement can be seen resulting in a higher drive current [2]. Another concern for the continued scaling of MOSFET devices is the SiO_2 gate dielectric. The current devices with 1.3nm gate oxides seem to have reached a fundamental limit with SiO_2. As the gate oxide thickness is reduced below this thickness the leakage currents present between the gate and the substrate present a major concern. In an attempt to circumvent these fundamental limitations extensive investigations have been done in search of high-? dielectrics suitable for the replacement of SiO_2 as the gate dielectric in MOSFET devices.

This study investigates the integrability of strained-Si substrates with high-? dielectrics, Hafnium oxide (HfO_2). Metal Oxide Semiconductor (MOS) capacitors are manufactured using a high-? dielectric for the oxide on strained and bulk Si samples. CV measurements are made on each of the capacitors and the traces are compared to determine interface qualities.

This work is part of capstone design requirement for a B.S. degree in Microelectronic Engineering at the Rochester Institute of Technology (RIT), Rochester, NY. The results of the project were first presented as part of the 22nd Annual Microelectronic Engineering Conference, May 2004 at RIT.

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II. Theory

A. Strained Silicon

Strained-Si is being investigated as a direct replacement to bulk Si for MOSFET fabrication. With the introduction of strained-Si into the channel of the device can increase drive currents, while decreasing the power consumption. Strained-Si substrates are fabricated using multiple epitaxial thin film growth steps forming a stack of films on the silicon substrate. The first film grown on the substrate is a Silicon Germanium ($Si_{1-x}Ge_x$) heterostructure layer, used as a strain introduction layer. Next, a 10-40nm layer of psuedomorphic silicon is epitaxially grown on the $Si_{1-x}Ge_x$ layer. The lattice spacing of the $Si_{1-x}Ge_x$ layer is different than that of the Si layer grown on the relaxed $Si_{1-x}Ge_x$ layer. This difference in the lattice spacing causes the atoms of the grown Si layer to adjust to match the lattice spacing of the underlying layer. As the Si atoms conform to the underlying layer the lattice is stretched in the lateral direction causing a biaxial tensile strain in the silicon lattice. The introduction of the strain into the Si increases the effective mobilities of the carriers in the strained-Si layer. This mobility enhancement comes about as a result of the energy band splitting of the $?_{2\text{-}4}$ conduction bands due to the vertical electric field in the MOS devices [3]. As these energy levels are repopulated the carriers are at a lower energy reducing the effective mass and increasing the low field effective mobilities. The amount of band splitting and the energy band gap throughout the can be calculated using the method presented by Richard based on the percent of Ge contained in the relaxed $Si_{1-x}Ge_x$ layer [4].

B. High-? Dielectrics

As transistors are scaled the gate oxide thickness must also be reduced to maintain a constant electric field in the device. As the thickness of the gate oxide begins to approach 2nm the gate leakage current begins to increase exponentially [5]. These large leakage currents have detrimental effects on the device performance as well as a drastic increase in the power

consumption. The attempt to reduce these leakage currents is the main driving force behind the switch to alternative gate dielectric materials. These leakage currents arise due to electron tunneling through the gate dielectric. With increased scaling the oxide is correspondingly reduced, resulting in elevated leakage currents. By increasing the relative permittivity of the dielectric being used for the gate a thicker film can be deposited while maintaining the same capacitance. By making the gate dielectric thicker the direct tunneling of carriers from the gate can be prevented. The relative permittivity of the high-? dielectric abd the equivalent oxide thickness (EOT) are related by (1).

$$EOT = \frac{\varepsilon_{OX}}{\varepsilon_{hik}} T_{physical} \quad (1)$$

Where e_{OX} is the dielectric constant of SiO_2, $T_{physical}$ and e_{hik} are the physical thickness and dielectric constant of the high-? film respectively.

There are many properties of the new material that must be taken into consideration when choosing a new dielectric. These include the thermodynamic stability with silicon at elevated temperatures, the dielectric constant, and the conduction band offset. Some of the candidates being explored to replace SiO_2 are; Tantulum Pentoxide, Aluminum Oxide, Zirconium Oxide, and Hafnium Oxide. For this investigation Hafnium Oxide (HfO_2) was used because of its physical characteristics, dielectric constant around 20, thermodynamically stable with Si up to 950°C, and has a conduction band offset of 1.5eV.

III. Experiment

NMOS capacitors were fabricated on strained and bulk Si substrates with boron background doping of approximately 5 x 10^{15} cm^{-3}. Strained-Si substrates were donated by AmberWave Systems, upon receipt these 200mm wafers were laser cut into two 100mm wafers. After this, the wafers were cleaned using a standard RCA clean to prepare the surface for dielectric deposition. Wafers were sent to University of Texas at Austin were an HfO_2 film was deposited by ALD, and a TaN gate material was deposited using a reactive sputter technique. At the same time wafers were sent to Yale University for HfO2 film deposition by JVD. Al gate material was deposited using evaporation. The gates were then patterned using a g-line stepper exposure system. The Al gates were etched using a phosphoric, nitric and acetic acid wet chemistry mixture. The TaN gates were etched using a CF4 RIE technique.

The samples were then characterized using a Kiethley 82 CV meter. Capacitance curves were measured from –4V to +2V in the forward and reverse directions. Also, VASE measurements were used to determine the HfO_2 film thickness.

IV. Results and Discussion

The interface between the gate dielectric and substrate is a critical part of the MOS device. The quality of this interface affects all aspects of the operation of the device. A degraded junction between the dielectric and substrate will decrease transconductance lowering the overall performance of the device. SiO_2 has a very high quality interface with Si. In fact this aspect of SiO_2 and Si has been a large driving factor for staying with Si for so long. In order for a new high-? dielectric to replace SiO_2 the charge levels of the interface must be kept low near the levels of SiO_2. Without these low charge levels the new material will not be accepted as an alternative.

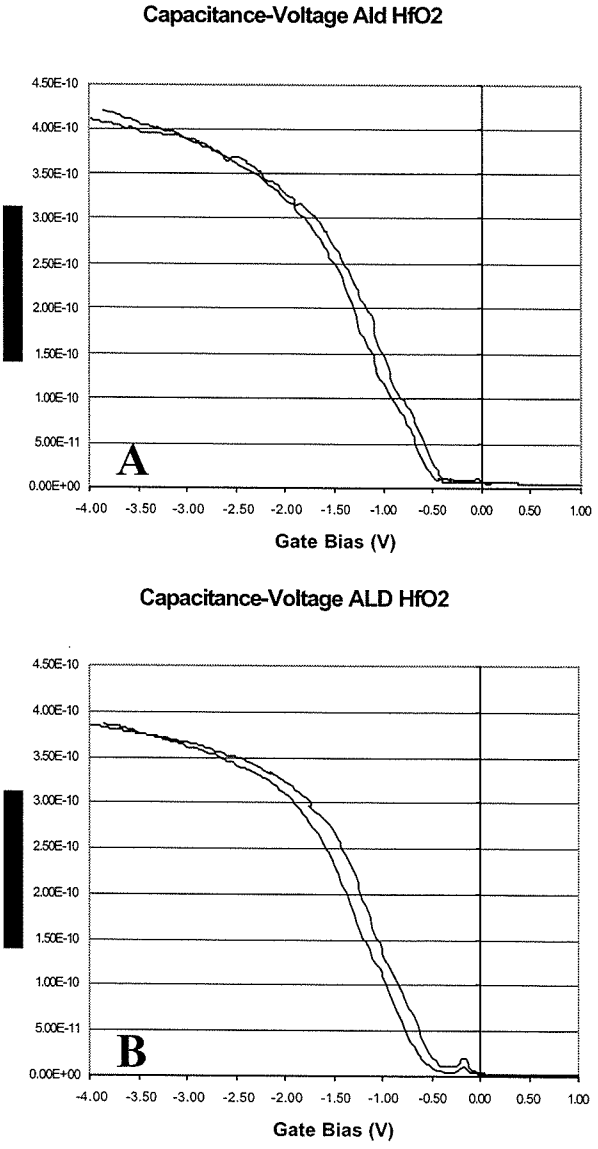

Figure 1: CV Curves for ALD deposited HfO2 filmson a.) bulk Si and b.) Strained-Si

A. ALD HfO_2 Capacitors

Figure 1 shows the CV characteristics at 100 kHz for MOS capacitors with 5nm of ALD HfO_2. The bulk Si trace is shown in figure 1a and the strained-Si trace is shown in figure 1b. The calculated equivalent oxide thickness (EOT) for these samples is approximately 1.74nm for the bulk Si and 1.89nm for the strained-Si sample. These values were calculated using a SiO2 dielectric constant of 3.9 and equation (2):

$$C_{OX} = \frac{\varepsilon_{SiO2} A}{EOT} \qquad (2)$$

Where e_{SiO2} is the dielectric constant of SiO2 (3.9), A is the area of the capacitor and C_{OX} is the oxide capacitance of the capacitor during accumulation. TEM images of the dielectric film show the presence of an interfacial layer between the HfO2 and the substrate. This interfacial layer is mostly SiO2 and is shown to historically be between 0.5-0.7nm for films of this thickness. Using the following equation the high-? dielectiric constant can be calculated.

$$EOT = \varepsilon_{SiO_2} \frac{T_{\text{int}}}{\varepsilon_{\text{int}}} + \varepsilon_{SiO_2} \frac{T_{hik}}{\varepsilon_{hik}} \qquad (3)$$

Where T_{int} and T_{hik} are the thicknesses of the interfacial layer and high-? dielectric respectively, and e_{SiO2} e_{int} e_{hik} are the dielectric constants of SiO2 the interfacial layer and the high-? dielectric respectively. Using equation (3) the dielectric constants were calculated to be 18.8 for the bulk Si sample and 16.4 for the strained-Si sample. The capacitance curves for these two traces overlay one another almost perfectly. This shows that the charge levels in these two samples are nearly identical. The differences in the two traces in the accumulation region is minimal and is most likely due to differences in the as etched capacitor areas.

B. JVD HfO_2 Capacitors

Figure 2 shows the CV characteristics at 100 kHz for MOS capacitors with 5.7nm of JVD HfO_2. HfO2 film thickness was measured using variable angle spectroscopic ellipsometry (VASE). Using the accumulation region oxide capacitance and equation (2) the EOTs for these samples were calculated to be 2.11nm for the bulk Si sample and 2.24nm for the strained-Si sample. TEM images of the JVD samples show that the interfacial layer is slightly larger, approximately 1.2 to 1.5nm of SiO_2. Using 1.2nm for the interfacial oxide thickness and equation (3) the dielectric constants were calculated to be 24.4 for the bulk Si sample and 21.3 for the strained-Si sample. Looking at these two traces the first thing that was noticed is the flat band voltage shift. The flat band voltage of the strained-Si sample is approximately 0.5 volts lower than that of the bulk Si sample. This shift can not be said to be caused by the strained-Si because the ALD samples did not show this shift. At this time the cause of the shift is unknown. Other than the shift the strained sample has less of a hystorisis effect from the duel sweep. This implies that the charge levels in the strained sample may be lower than in the bulk sample.

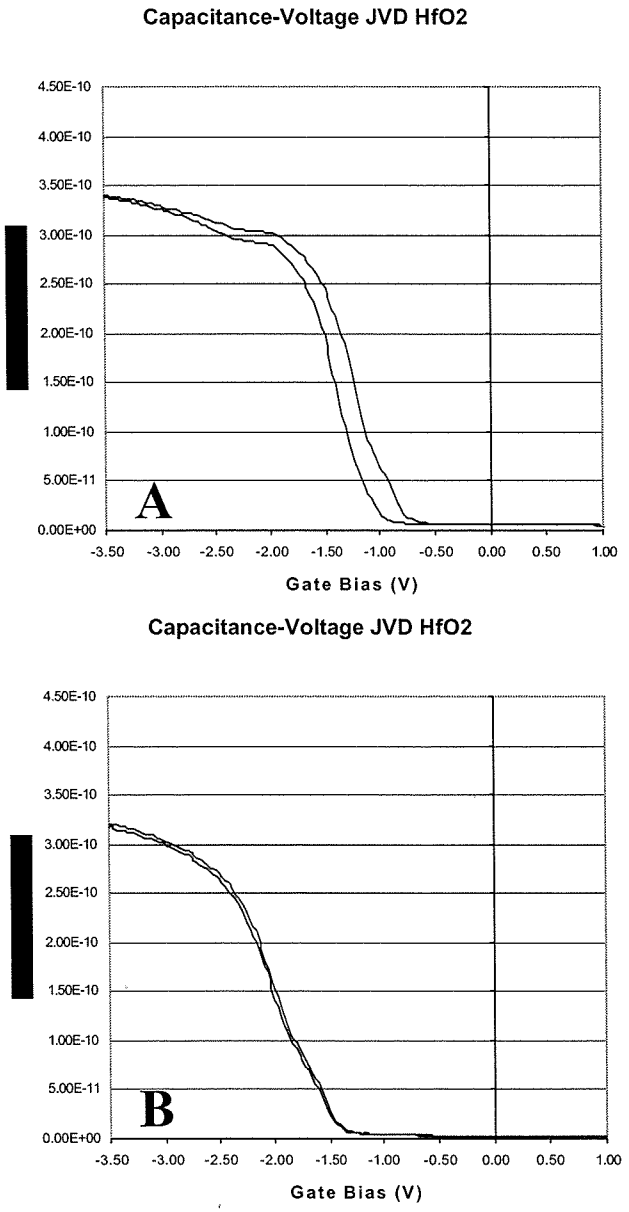

Figure 2: CV Curves for JVD deposited HfO2 filmson a.) bulk Si and b.) Strained-Si

V. CONCLUSION

The study showed the ability of incorporation of HfO2 and

strained-Si in a MOS device. Interface charge levels were shown to not have any large affect on the CV response of the device. Future work should be done to further characterize and explore the effects of the interface on device performance as well as full MOSFET fabrication incorporating HfO2 and strained-Si.

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