Metal Source/Drain Schottky Field Effect Transistors – a Proof of Concept

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Abstract—**Field effect transistors, in which the sources and drains are made of metal (aluminum), as opposed to silicon, have been conceived, designed, fabricated, and tested. For the n-body device, maximum Jon was found to be 74.69μA/μm after a "burn-in" process was performed. For 1V to 10V drain bias, extracted Vtsat values varied between 2.3V and 6.5V, gm between 0.002 and 341μS, sub-Vt slope between 111 and 706mV/dec, and Ion:Ioff between 1.11 and 3.99 decades. The Schottky barrier height was found to be 0.503eV. Additionally, full CMOS operation using one metal for both NFET and PFET operation is proposed and discussed. The long-term goal of the presented device is 3D circuit integration, for which a potential implementation scheme is presented.**

Index Terms—**3D circuitry, metal source/drain, SBMOSFET, SBTT, Schottky source/drain.**

I. Introduction

Over the past few decades, the drastic increase in consumer demand for smaller, faster, and cheaper computing devices has played a major role in driving the semiconductor industry to its current state of technology, as well as increasing the range of applications for microprocessors. Quite naturally, however, new technologies pose new challenges. One such challenge is overcoming the degrading ability of aggressively-scaled transistors to act as desirable switches in digital circuitry, which has been running in parallel with overcoming the degrading ability to manufacture said transistors using conventional methods. Some solutions propose to scale devices in three dimensions rather than the current two (known as 3D circuitry for its suggestion of building multiple semiconductor levels on a single chip), while other solutions propose to better the performance characteristics of the devices themselves by utilizing unique processing techniques. It is the primary purpose of the Metal Source/Drain Schottky Field Effect Transistor (MSD SFET) to attempt to provide the potential for both such solutions with one [relatively] simple approach.

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The MSD SFET was initially conceived as a means to circumvent potential thermal processing issues upon implementing 3D circuitry in microelectronics. However, further investigation shows that the MSD SFET may prove a potential candidate for future device scaling in traditional 2D CMOS.

The MSD SFET itself has sources and drains which are made of metal. With the right type of metal and the right type of semiconductor (i.e., n-type or p-type silicon of a particular doping level), a Schottky barrier is formed at the metal-semiconductor interface (a comprehensive analysis of metal-semiconductor junctions can be found in [1]). A gate is placed perpendicular to the source-body and drain-body interfaces, and modulates the barrier dimensions by accumulating or depleting majority carriers at the interface. In doing so, the interface becomes either more Schottky-like or more ohmic-like, thus resulting in a gate-modulated current flow.

Similar work has, coincidentally, been performed over the years using sources and drains made of metal silicides [2]-[9]. Metal silicides, however, are formed through diffusion of metal through silicon and some subsequent reaction to induce alloying. Since the MSD SFET uses pure metal rather than metal silicides, this silicidation step is not necessary, and it may even be conceivable to use the same process level for both the NFET and PFET sources and drains as well as the first level of interconnects, thus decreasing manufacturing costs substantially.

Some potential advantages that the MSD SFET has over conventional MOSFETs are: 1.) the source-body and drain-body junctions are ideally abrupt (e.g., no dopant concentration gradient exists), and so the device should be less susceptible to short channel effects such as DIBL and Vt rolloff; 2.) since the MSD SFET is a majority carrier device, it should, in theory, experience zero floating body effect when manufactured on SOI substrates; 3.) since the MSD SFET switches through majority carrier accumulation (as opposed to moderate-to-high inversion), it is presumed that a lower voltage is needed to run a MSD SFET than an equivalently-sized conventional MOSFET.

II. Theory

A. SBMOSFETs and SBTTs

Any given Schottky diode can be made to act in an ohmic manner by either using a semiconductor of the opposite doping (e.g., p-type vs. n-type), or by using a heavier-doped

semiconductor. In the first case, the barrier height will decrease in value, and so the dominant current mechanism will be thermionic emission of carriers over the barrier. This is the principle of operation behind conventional SBMOSFETs (Schottky Barrier MOSFETs), where typically an n-type silicon body is used to make a Schottky barrier with Pt-Si, with a barrier height on the order of 0.85eV [1]. Inverting the body region to p-type decreases the barrier height to about 0.25eV [1]. In the second case (using a heavier-doped semiconductor), the effect is that the band bending in the semiconductor at the metal-semiconductor interface increases, eventually to the point at which carriers have a high probability of tunneling through the sufficiently narrowed barrier. Therefore, in this case the dominant current mechanism is tunneling current. The effect of higher dopant concentrations can also be realized by accumulating or depleting carriers from the metal-semiconductor interface (with a gate bias) for a semiconductor of a given dopant level. Such is the principle of operation behind a different form of SBMOSFET, known as a SBTT (Schottky Barrier Tunneling Transistor).

Since conventional SBMOSFET operation relies on thermionic emission for the on state of the transistor, it is desirable for the source/body and drain/body barrier heights to be as low as possible under inversion to minimize contact resistance. This contact resistance can be expressed as [1]:

$$R_c = \frac{k}{qA^*T}\exp\left(\frac{q\phi_B}{kT}\right) \quad (1)$$

where k is Boltzman's constant, ϕ_B is the barrier height, T is the temperature, q is the charge of an electron, and A^* is the effective Richardson constant. Neglecting the temperature dependence of Rc, barrier height becomes the only variable which can be changed to affect the contact resistance in a conventional SBMOSFET.

For the SBTT, the on state takes place during high majority carrier concentrations, and so contact resistance can be expressed as [1]:

$$R_c = \exp\left[\frac{2\sqrt{\epsilon_s m^*}}{\hbar}\left(\frac{\phi_B}{\sqrt{N}}\right)\right] \quad (2)$$

where h is Planck's constant, m^* is the effective carrier mass, and N is the majority carrier concentration. While the same exponential dependence on barrier height is present, the contact resistance is effectively modulated by the gate bias which accumulates or depletes carriers at the source/body and drain/body junctions. Therefore, the effect of larger barrier heights can be countered by stronger accumulation (at least until quantum carrier confinement becomes significant). This allows the SBTT to use large barrier height metal-semiconductor junctions to allow for greater thermal operating stability without a significant loss in on state current.

Considering that both conventional SBMOSFETs and SBTTs start from the same device, and that the only difference between the two is the polarity of the gate and drain biases, it would not be unreasonable to suggest that a transistor with Schottky sources and drains would exhibit both conventional SBMOSFET-like and SBTT-like characteristics with the appropriate biases at each terminal (more on this later).

B. MSD SFETs

The MSD SFET is a form of SBTT, in that switching takes place through accumulation (and so tunneling current dominates the on state current). For the particular design discussed, it is only the NFET which acts as a SBTT, as the goal is to implement CMOS circuitry by using one metal instead of two separate metals for two separate Schottky barriers for n-Si and p-Si. Since this design uses an n-Si body for the NFET, the PFET uses a p-Si body, and so a Schottky barrier formed with the source/body and drain/body junctions in the NFET is either schottky but with a lower barrier height or simply ohmic for the PFET. With zero gate bias, then, the PFET is in the on state and must be switched off through depletion or light inversion.

To utilize such a PFET in CMOS circuitry, however, the device would need two gates, by which one gate (the bottom gate) would have a constant bias which depletes the silicon in contact with the metal source and drain (the off state). The other gate (the top gate), when biased, would counteract the effect of the bottom gate, thus making the source/body and drain/body junctions ohmic again. Such a setup would require a high dopant concentration in the body region for acceptable current drive. A possible implementation using a single gate MSD PFET would use a low-doped p-Si body region, which has very low current drive in the off state. A negative gate bias would accumulate carriers toward the silicon/gate dielectric interface, thus turning the transistor "on." However, since the dual gate PFET allows for greater Vt control, it should exhibit better performance characteristics (namely subthreshold slope).

C. MSD SFET Theory of Operation

In a conventional MOSFET, pinchoff occurs when the difference between drain bias and gate bias is small, such that the channel region near the drain is no longer inverted. This results in the saturation region in the Id vs. Vd characteristic. Understanding the mechanisms behind saturation in the MSD SFET is somewhat less trivial.

Consider Fig. 1 on the following page. At zero drain bias, and for any gate bias, some sort of band bending takes place at the source-body and drain-body interfaces. For an n-Si body SFET, the drain-body diode is forward biased (and so the "barrier height" is the built-in voltage of the diode) and the source-body diode is reverse biased (the barrier height is that on the metal side of the junction). As a drain bias is applied, the built-in voltage of the drain-body diode decreases by $V_{bi} - V_{drain}$, and eventually this diode will turn on much like a standard p-n diode. However, even in the "on" state, the drain current is limited by the source current, and the source-body

diode current is the reverse bias saturation current (for a given source barrier width, there exists a limit as to the number of carriers that can be injected from the source into the body). The energy gradient in the body due to the drain bias, however, will serve to decrease the source barrier width (the degree of this effect is dependent on gate bias, as will be discussed later). The decrease in this width will increase tunneling through the barrier, consequently increasing the maximum amount of carrier injection (this becomes significant beyond the saturation region) from the source. At low drain biases, the maximum source injection current is relatively constant, and not being utilized to full capacity, thus resulting in the linear region of the Ids vs. Vds plot. At Vd(sat), the maximum number of carriers are injected from the source for the specific source barrier width, and within some region afterwards increasing the drain voltage will result in little if any increase in drive current. It is at this point that the transistor is in the saturation region of operation.

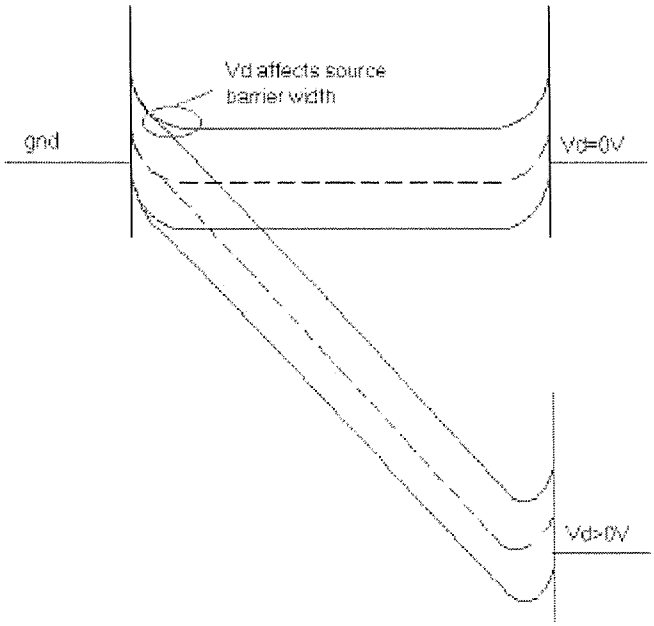


Fig. 1: Metal-semiconductor-metal energy band structure at Vd=0V and Vd>0V for a given gate bias. The drain bias decreases the source-side barrier width, while simultaneously decreasing the built-in voltage of the drain-body diode. This effect has been coined as Drain Induced Source Tunneling (DIST), and becomes significant at very high drain biases.

At drain voltages well beyond Vd(sat), there is enough of a lateral field throughout the transistor such that the drain has control over the source barrier width (the aforementioned DIST effect from Fig. 1). At this point, the maximum source carrier injection current increases with drain bias, and this injection current is fed to the drain-body diode which, at such high biases, is already in an "on" state. This results in a diode-like I-V behavior at very high drain biases. Increasing the gate bias will decrease the source barrier width, thus increasing the lateral field required to further decrease the barrier width. Additionally, an increase in gate bias will increase the built-in voltage of the drain-body diode, thus increasing the turn-on voltage of that diode. At higher gate biases, then, the drain voltage at which DIST occurs is increased.

D. MSD SFETs on SOI Substrates

If SOI substrates were used to manufacture MSD SFETs, it should be expected that the SFET would experience little if any floating body effect (which correlates to the "history effect"). First considering the NFET, the reverse-biased diode is the source/body diode. Applying a drain bias with zero gate bias should result in little charging of the body region, as the majority carriers (electrons in this case) must first traverse the *source*/body junction. Since Schottky diodes are majority carrier devices, in the case of the NFET, only electrons may enter the body region and bring it to some potential. Therefore, only if there were an ohmic contact between the drain and the body (or at very high drain biases such that DIST occurs) would the body be at some potential to induce electron flow from the source, and in such a case, the gate of the NFET would be ineffectual in controlling current flow anyway (as it is now controlled almost entirely by the drain), thus rendering the device as non-yielding.

The PFET is more like a gate-modulated resistor – it starts off as having ohmic contacts at the source/body and drain/body interfaces, and the device is switched off when the gate "blocks" current flow between the source and drain. When the PFET is in the off state, the body region in contact with the source/drain regions is either depleted or lightly inverted. In the depleted case, no net carrier concentration exists, and so the body region cannot charge up to some potential. In a lightly inverted case, presumably the source/body and drain/body junctions see a Schottky barrier which is the same as the NFET in its off state, and it has previously been shown that the body region of the NFET should not float on SOI substrates.

This lack of a floating body effect is an extremely important effect to take note of, as it is considered to be a primary disadvantage regarding circuit design on SOI substrates (due to the resultant dependence of the threshold voltage on the body potential, which is not constant throughout a clock pulse). That the body region of a MSD SFET should not float to a potential allows one to utilize the advantages of SOI technology without the challenge of taming the history effect.

E. 3D Circuit Integration

The notion of 3D circuitry, by which multiple device layers are stacked on top of each other within a single chip, has been around for some time, with efforts performed by various research groups [11]-[18]. These implementations, however, utilize conventional MOSFETs. Likewise, as of yet SBMOSFET and SBTT research has not hinted at applications to 3D circuit integration. Considering the possibility of Schottky CMOS becoming a placeholder on the ITRS roadmap [19], integration of Schottky CMOS into 3D circuitry would seem a natural progression.

The real strength of 3D circuitry is not that individual logic gates can be built using multiple levels (thus consuming less area), but rather that entire logic *branches* can be built on

multiple levels, and that this can be exploited to minimize transmission delays through interconnects. For example, an ALU unit in a microprocessor can be built with three device levels, thus consuming less area. Or, perhaps, the ALU can be built on one level and the SRAM can be built directly on top on another level. With enough levels, it might also be feasible to realize solid state hard drives which operate much faster than the mechanical units in present day computer systems. The potential for maximizing packing density is quite staggering, as are the implications for System-on-a-Chip (SoC) solutions.

Some approaches to 3D circuit integration involve chip-to-chip bonding. This is effective in that it realizes single-crystalline silicon for each device level, thus maximizing performance. The temperatures required for the bonding techniques are low enough so as not to significantly affect the performance characteristics of the fabricated devices. However, that n separate chips must be manufactured to build an n-level 3D circuit results in the final product costing roughly n-times as much. This clearly raises practicality issues for large volume, low-cost fabrication. For high-end systems where cost is not a concern, however, it may well be the best solution.

Another approach to 3D circuit integration is to deposit silicon films on top of previous device layers. This allows a multi-level "chip" to be fabricated on a single wafer, presumably reducing manufacturing cost. The deposited silicon film is recrystallized to form a polysilicon film of some grain size, on which devices are fabricated. The disadvantage to this process is that, by virtue of the devices being manufactured on polysilicon films as opposed to single crystalline silicon films, the devices themselves exhibit poorer performance characteristics due to degraded carrier mobility and increased leakage currents. However, if the grain sizes can be made large enough such that one device, or one logic gate, or perhaps an entire logic branch, can be fabricated within a single grain, then the device performance in such large grain polysilicon films is equivalent to that of single crystalline silicon.

One of the more promising methods for recrystallization of deposited silicon films to large grain polysilicon is known as MILC (Metal-Induced Lateral Crystallization) [14], [15]. Normally, recrystallization takes place vertically, and so the grain size is on the order of the film thickness. For aggressively scaled devices, this is not desirable, as thinner silicon films are becoming necessary to maintain or improve performance. The MILC process uses nickel "trenches" between areas of amorphous silicon. At elevated temperatures, the nickel forms a silicide and diffuses through the amorphous silicon, leaving large grain polysilicon in its wake. Further recrystallization takes place at higher temperatures (albeit over less time). Two level 3D circuits built using this method have been shown to exhibit enhanced performance over 2D SOI circuits [14]. However, the primary issue is that recrystallization takes place over very long periods of time (tens of hours), and at temperatures which may affect device performance.

The most significant challenge to 3D circuit integration, however, is thought to be the optimization of vertical interconnect routing [15], rather than the formation of single crystalline or near single crystalline silicon films. The MSD SFET can be useful for 3D circuit integration in that, in the design presented, the device is more comparable to a switch within the interconnects than the current day perception of devices separate from the interconnects. This in itself has potential for increased 2D packing density, but also has increased potential to overcome device contact issues (also for 2D circuits) at very small sizes, as well as interconnect routing issues for 3D circuits. If very thin interfacial layers (oxide, nitride, etc.) are placed between the metal source/drain regions and the body region, such that the interfacial layer is thin enough to be transparent to tunneling but thick enough or of the right material to slow down or prevent reaction between the metal source/drain regions and the silicon body region, or the interfacial region, at elevated temperatures during MILC processes, then the MSD SFET may prove a universally useful device for both 2D circuitry and most approaches to 3D circuit integration.

III. EXPERIMENTAL PROCEDURE

The devices were fabricated on 4-inch 15Ω-cm bulk n-Si wafers with aluminum as the metal of choice. Aluminum was chosen because it is relatively simple to manufacture Schottky diodes using aluminum and lightly doped n-Si. A top-down view and two cross-sections of the MSD SFETs are shown in Figs. 2, 3, and 4, respectively. The manufacturing process requires seven microlithography levels. Level 1 defines the N+ implant which acts as an ohmic contact to a Al/n-Si Schottky diode. Level 2 defines the p-well implant, which results in a p-Si body for the MSD PFETs. Both implants are performed through a 500Å dry pad oxide, and the anneal/drive-in process uses the same pad oxide recipe. The resulting ~1000Å of oxide serves as a field oxide, through which active areas are defined and etched (Level 3). The exposed silicon surface is put through a pre-evaporation clean (1 min. dilute HF, 1 min. DI rinse, N2 blow dry), and then placed in a bell jar evaporator for pure aluminum deposition (wafers under vacuum in 5-10 min.).

Level 4 defines the metal source and drain as one piece. The photoresist is left on the aluminum, and a silicon etch is performed using SF_6 and CHF_3. The photoresist is then stripped, and a channel define etch is performed which splits apart the source and drain regions (Level 5). The gate dielectric (500Å PECVD TEOS) is then deposited and patterned (Level 6), as is the second layer of aluminum, which acts as the gate electrode (Level 7).

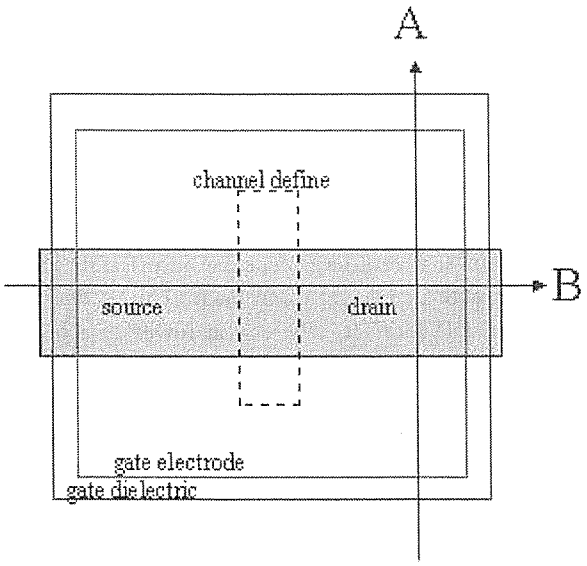


Fig. 1: Top-down view of MSD SFET with cross-sections A (Fig. 2) and B (Fig. 3).

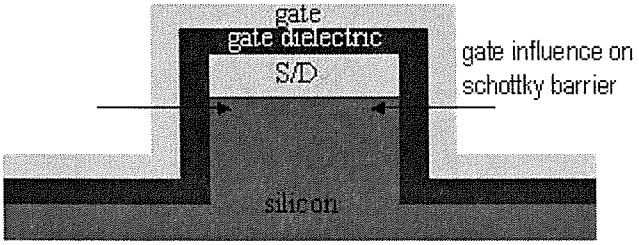


Fig. 2: Cross-section A of Fig. 1.

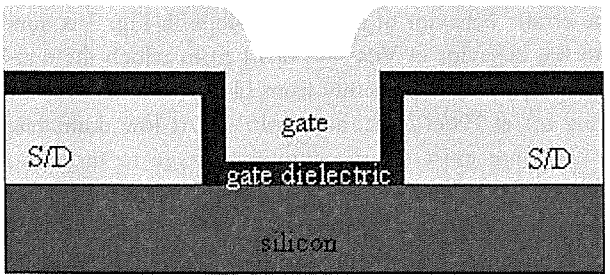


Fig. 3: Cross-section B of Fig. 1.

In various stages of the process, different wafers were sintered at 450°C in H2/N2 forming gas for 15 min. MSD SFETs were manufactured on a total of nine wafers, with four processing splits, as defined in Table 1. One wafer from each of the first three splits was run through the entire 7-level process to fabricate both n-body and p-body SFETs (as well as test structures), while the other six wafers saw a 6-level process for the n-body SFETs and test structures. It should be noted that a complete comparison between the process splits was not performed, as the uniqueness of the I-V characteristics placed a greater importance on understanding the true operating theory behind the device.

TABLE 1

MSD SFET Process Splits

Wafer number	Split definition
2,3,4	Post M1 deposit sinter
5,6,7	Post silicon etch sinter
8,9,10	Post channel define sinter
2,6,10	P-well implant for n-body FETs

IV. EXPERIMENTAL RESULTS AND DISCUSSION

Fig. 4 shows the "burn-in" process performed on an n-body SFET. With the gate set at 10V, the drain is swept from 0V to 10V for a number of runs until the resultant curves begin to look similar. This allows for greater consistency when comparing the results of various devices. It has been found that a burn-in process of 14 runs is sufficient, and that leaving the device untested for one day after the burn-in process has no significant effect on the device characteristics.

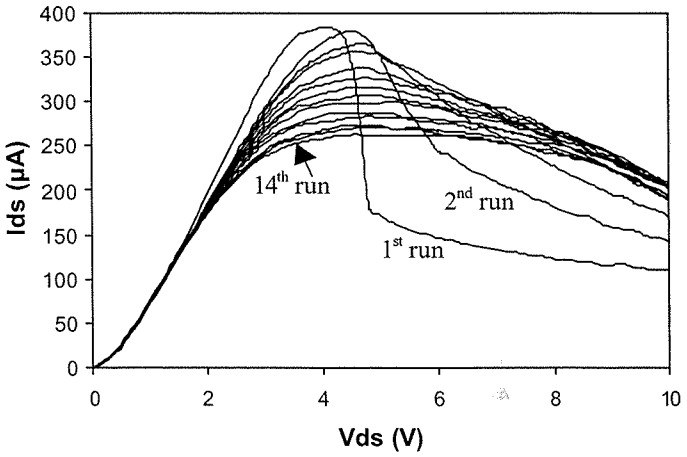


Fig. 4: Ids vs. Vds "burn-in" process of 14 runs for an n-body SFET (Wmask = 5μm, Lmask = 2μm). The gate is kept at 10V and the drain is swept from 0V to 10V until the resultant curve becomes repeatable. It is thought that this burn-in is required so as to minimize the effect of surface states at the metal-semiconductor junctions.

Fig. 5 shows the complete Ids vs. Vds characteristic of the same device for both SBTT-like (first quadrant, n-channel, electron tunneling current) and conventional SBMOSFET-like (third quadrant, p-channel, hole thermionic emission current) operation, as predicted from the theory section. Electron current is seen in third quadrant operation at low gate biases, as these low gate biases are not enough to offset the Vt shift from the oxide charge present in the PECVD TEOS used as a gate dielectric (and so the channel is not yet inverted). Considering this Vt shift, the peak current in the third quadrant should be larger for Vg=10V with a gate dielectric with minimal charge density. Likewise, the peak current in the first quadrant should be lower. Nevertheless, the difference in current

between first and third quadrant operation can be explained by both the difference in electron and hole mobilities, as well as the difference in contact resistance between the inversion and accumulation cases, shown by (1) and (2). It should be noted that under very strong inversion, the contact resistance can be expressed using (2), as the dominant current mechanism becomes hole tunneling as opposed to hole thermionic emission. Fig. 6 shows the Ids vs. Vgs characteristic for the same device, and Fig. 7 shows the sub-Vt slope and maximum transconductance vs Vds.

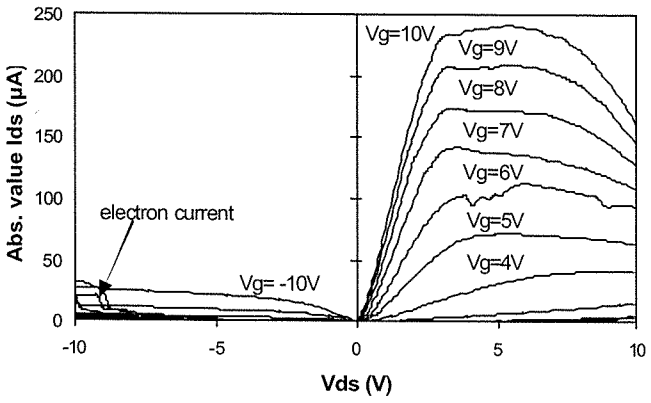


Fig. 5: Complete Ids vs. Vds characteristic for 2μm x 5μm n-body SFET. Peak current in the first quadrant is 242μA. Device width after etch is 3.24μm, corresponding to a peak Jon of 74.69μA/μm. Peak current in the third quadrant is 27μA, or 8.33μA/μm.

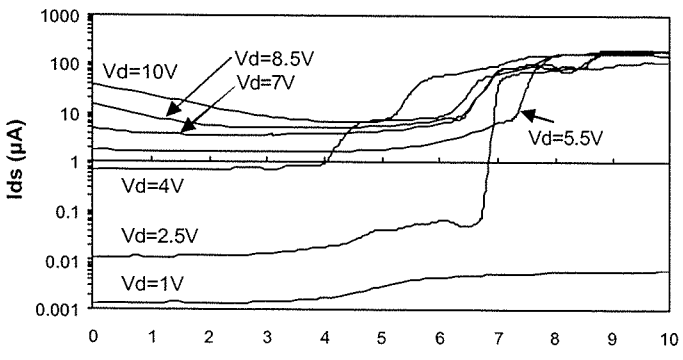
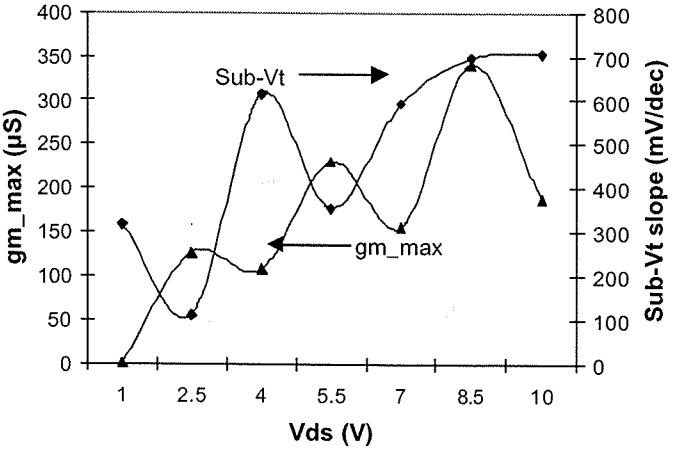


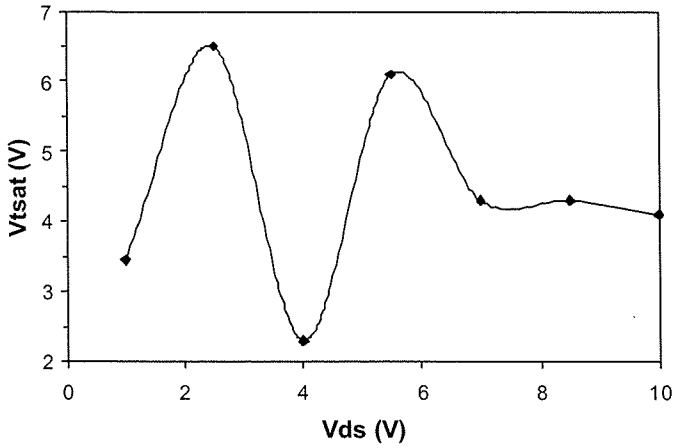
Fig. 6: Ids vs. Vgs characteristic for 2μm x 5μm n-body SFET (n-channel). Vds was varied from 1V to 10V in 1.5V increments.

Fig. 7: Sub-Vt slope and gm_max vs. Vds for 2μm x 5μm n-body SFET (n-channel). Minimum sub-Vt slope is 111mV/dec., maximum transconductance is 341μS.

As Fig. 6 shows, a very large increase in off state leakage current occurs with increasing drain bias. This is due to the aforementioned DIST effect, whereby at lower gate biases, a lower drain voltage is necessary to modulate the source barrier width. The decrease in drain current at larger drain biases for gate biases from 0V to about 3V reinforces this idea, as at higher gate biases the source barrier width is smaller (thus requiring a larger drain bias for DIST).



The erratic behavior of the sub-Vt slope in Fig. 7 is simply due to the behavior at Vds=4V, apart from which the sub-Vt slope increases rather smoothly from 111mV/dec. at Vds=2.5V, tapering off at 706mV/dec. at Vd=10V. At low drain biases, there does not exist a large enough voltage to turn on the drain-body diode, and so little if any current draw is displayed (as shown in the Vd=1V case in Fig. 6). This causes the sub-Vt slope to increase. Therefore, for low voltage operation it is critical to fabricate drain-body Schottky diodes with low turn-on voltages or a drain-body junction that is ohmic. The ohmic case would provide for better low voltage current drive and sub-Vt slope; however, it may also lower the drain bias requirements for DIST to take place, thus potentially increasing off state leakage current.



Vtsat vs. Vds is shown in Fig. 8, and corresponds with Figs. 6 and 7 in that lower sub-Vt slopes result in larger Vtsat values, ranging from 2.3V to 6.5V.

Fig. 8: Vtsat vs. Vds characteristic for 2μm x 5μm n-body SFET (n-channel).

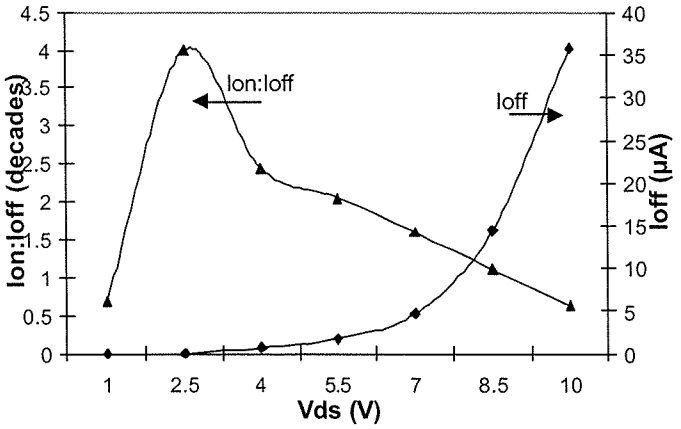


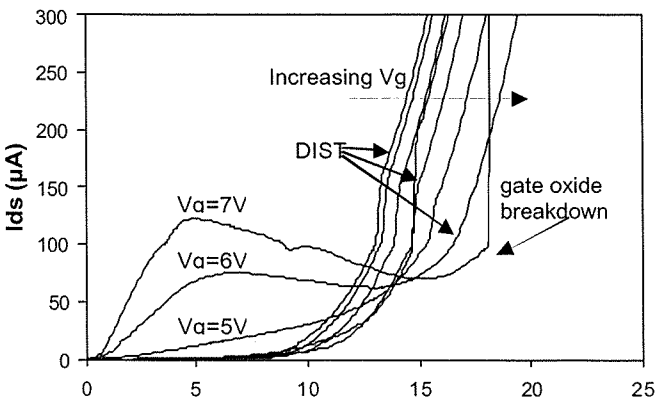
Fig. 9: Ion:Ioff and Ioff vs. Vds for 2μm x 5μm n-body SFET (n-channel). Maximum Ion:Ioff is 3.99 decades. Ioff increases exponentially, in accordance to the diode-like behavior resulting from DIST.

Fig. 10: Ids vs. Vds for 1μm x 10μm n-body SFET (n-channel). Onset of DIST occurs at about 10V and above, increasing with increased gate bias.

Fig. 9 shows Ion:Ioff and Ioff vs. Vds. It is stressed that Vds is used in these relationships, as opposed to Vdd, where the on state current is the drain current at Vg=10V, and the off state current is the drain current at Vg=0V. In looking at Fig. 6, it becomes clear that using Vdd as a metric would not give much information, since large gate biases are required to achieve an on state with little regard for drain bias.

The Schottky barrier height for this device was extracted from test diodes on the same die, using the current-temperature method [10]. Diode characteristics were measured at 30°C to 80°C in 10°C increments, and the resultant barrier height was calculated as 0.503eV.

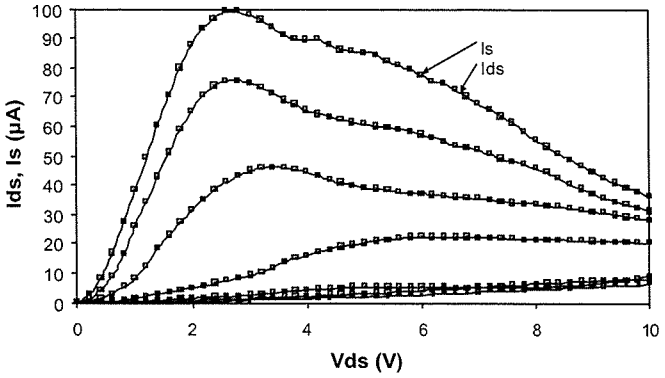
An example of DIST is shown in Fig. 10. As expected, an increase in gate bias results in an increase in the drain bias at which DIST occurs. The plot is a standard Ids vs. Vds relationship, but with the drain swept to 20V. At Vg=7V and Vds~18V, it is shown that the gate dielectric broke down. Further current measurements were at the 100mA rail.



Of particular interest with the n-body, n-channel SFET is the high Vg, high Vd region in Fig. 5. In this region, the drain current *decreases* with increasing drain bias (this is also seen in Fig. 10). The current theory regarding this "NDR" (Negative Differential Resistance) region is as follows.

In the n-body MSD SFET, the source-body junction is reverse-biased, as previously mentioned. As Vds increases, two events take place. First, the increasing reverse bias on the soruce-body junction causes the source-side depletion width to grow. Second, the increase in Vds causes a decrease in Vgd for a given gate bias, thus causing the drain end of the body region to become less accumulated (and eventually depleted as Vds surpasses Vgs). Therefore, with increasing Vds, the body region becomes increasingly depleted, thus increasing the body resistance. Since the NDR region occurs after saturation, which is after the point at which the source has reached its maximum carrier injection capacity for a given gate bias (and before the drain takes control via DIST), an increase in body resistance will decrease the current drive in this region (it is presumed that the increase in source injection capacity in the DIST region far outweighs the increase in body resistance), thus resulting in the observed phenomena.

Figs. 11 and 12 serve to not falsify the aforementioned NDR

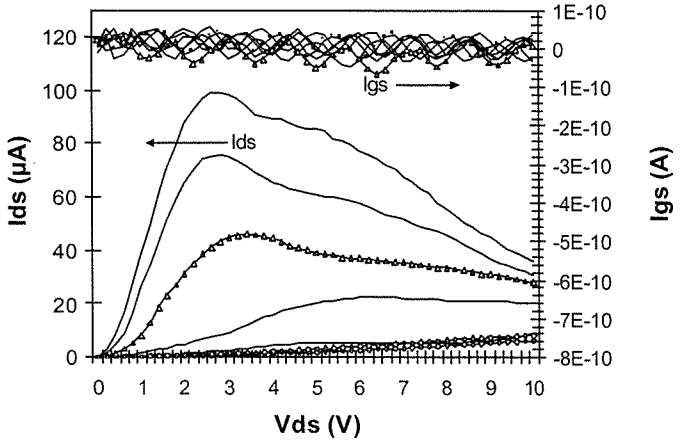


theory. Fig. 11 shows that the source and drain currents are almost exactly equal, and any difference is due to gate leakage, which is very small, as shown in Fig. 12. Therefore, there are no body current or gate current phenomena which are decreasing the drain current in this NDR region, suggesting that the effect is related to the behavior of the device itself.

Fig. 11: Ids and Is vs. Vds for 5μm x 10μm n-body SFET (n-channel). Square points are Is data, solid lines are Ids data. Equality of source and drain current indicate zero presence of body current which may subtract from Ids in the NDR region of operation.

Fig. 12: Ids and Igs vs. Vds for 5μm x 10μm n-body SFET (n-channel). Igs is very small (tens of pA), therefore, the NDR region is not influenced by gate leakage.

P-body SFET operation is demonstrated in Fig. 13. That there is a measured Ids at Vds = 0V suggests some form of gate leakage, and it turns out that the p-body SFET is dominated *entirely* by gate leakage current. This observed leakage is highly repeatable in the p-body devices, which is interesting considering the thickness (500Å) of the gate dielectric. Considering that gate leakage in the n-body devices is very low, as shown in Fig. 12, it becomes clear that the p-Si in the p-body devices is in some way facilitating current flow through



the gate dielectric. The exact mechanism/s behind this observation are, as of this writing, unkown.

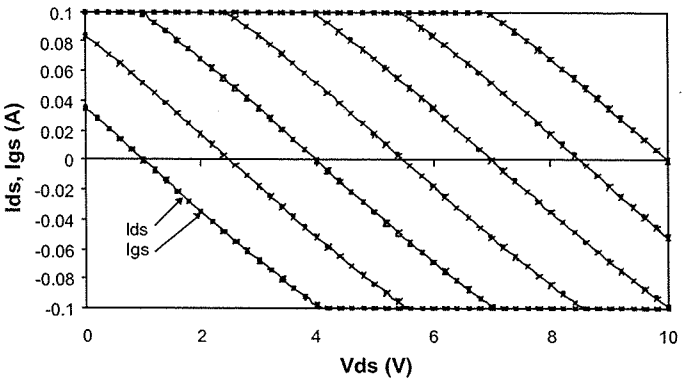


Fig. 13: Ids vs. Vds for 2μm x 5μm p-body SFET. Gate leakage current dominates device operation, and does now allow switching via gate-induced body depletion.

V. CONCLUSION

It was the purpose of this investigation to show that field effect transistors made of metal sources and drains can function via gate-modulated tunneling, thermionic emission, and body depletion. Gate-modulated tunneling and thermionic emission have been demonstrated in the n-body MSD SFET, and the results show potential for full CMOS operation. If it is possible to creatively utilize the dual-mode behavior of the n-body MSD SFET, it might be conceivable to realize CMOS operation with one type of transistor. P-body MSD SFET operation was shown to be dominated by gate leakage, and a higher quality gate dielectric would be necessary to demonstrate the device as it was intended to operate. Additional investigations must be performed regarding single metal CMOS, temperature dependence of operation, potential for 3D circuit integration, and potential for conventional 2D CMOS in future technology nodes.

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