

Gate Oxide Characterization for Non-Planar CMOS

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Abstract—The objective of this investigation was to characterize oxides grown on the sidewalls of etched silicon profiles. Conventional CMOS process technologies were used to fabricate vertical sidewall capacitors in addition to planar ones. Sidewall oxidation is a cornerstone in the development of non-planar CMOS devices such as the finFET and Vertical MOSFETs. The quality of this oxide is extremely important, even more so as devices are scaled such that oxide thicknesses are on the order of a few atomic layers. In order to obtain insight into the characteristics of these emerging devices, the effects of a non-planar gate oxidation must be completely characterized.

For this study optimum process conditions have been identified based on anisotropy of the silicon etch, repeatability, and the ability to extract the required information. Capacitance-voltage (CV) and current-voltage (IV) characterizations have been performed to electrically characterize the oxide as well as the associated oxide charges. Cross sectional SEM analysis was carried out to investigate the structural integrity of the silicon-oxide interface.

Index Terms—Vertical Capacitor, Gate Oxide, Oxide Charges, Emerging Devices.

I. INTRODUCTION

THE metal oxide semiconductor field effect transistor (MOSFET) has been in constant production, modification, and characterization since the 1960's. The technology has been driven to keep on pace with the observation made by Gordon Moore in 1965 which states that the number of transistors on an integrated circuit should double every 18 to 24 months, now known as Moore's law [1]. The reduction in device size to accommodate this mandate leads to increasingly smaller gate insulator thicknesses. The insulator, almost exclusively Silicon Dioxide SiO_2 has been extremely well characterized, even down to atomic thicknesses. This is necessary as almost every on-state parameter of the MOSFET is, in one-way or another, proportional to the oxide thickness and parasitic charges resident within the oxide [2].

The limits of the conventional, planar MOSFET are quickly becoming realized, and there is much research activity in the field of non-planar CMOS devices. Some emerging non-planar devices are the finFET and the Vertical MOSFET (VMOS). The 2001 edition of the ITRS roadmap [3] suggests that non-planar devices may be required as early as 2007. These two devices among other things feature a gate insulator that is grown or deposited on an etched profile. The ITRS also suggests that a high-k dielectric may be used in order to minimize gate current in the advanced devices. Current work on high-k dielectrics still uses an extremely thin thermally grown oxide for interfacial quality. It is important then to understand the oxidation kinetics as well as the resulting oxide charges that arise from this process technology.

Capacitance-Voltage (C-V) techniques as well as Current-Voltage (I-V) techniques are well suited to characterize a gate oxide. C-V techniques are particularly useful in determining oxide charges, which come in four varieties (see figure 1) [5]. Interface trapped charges reside at the oxide-semiconductor interface. These charges can be positive or negative in nature and usually arise from structural, oxidation induced, or radiation induced defects or metal impurities. Fixed charge is found within 2nm of the oxide-semiconductor interface and comes from silicon ions trapped interstitially within the oxide. Fixed charges are positive in nature. Oxide trapped charges are carriers, electrons or holes, trapped in the oxide as a result of radiation, avalanche injection, or fowler-nordheim tunneling. These charges are generally taken to be zero unless the oxide has been put under severe stress, or has been subjected to radiation such as can be found in a plasma. Oxide trapped charges can be negative or positive, but are more likely to be the latter. The final oxide charge is mobile charge. Mobile charges are generally metal ions introduced into the oxide by the processing environment. Generally these charges are positive in nature, mostly from Sodium and Lithium. Chlorine is a somewhat commonly found negative mobile ion, however negative ions are generally less mobile, and therefore often are not included in mobile charge.

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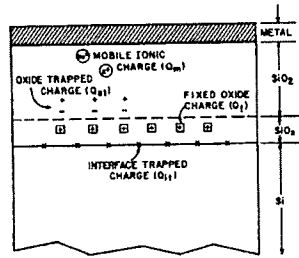


Fig. 1: Location of Oxide Charges

The incorporation of these charges within an oxide degrade the oxide's insulating ability, and can lead to early device failures. One metric used in qualifying the quality of an oxide is the critical field strength of the oxide. I-V stress tests are performed to extract this critical electric field of the oxide. This process is destructive and must be conducted on test structures.

Finally it is important to be able to observe the film under test. Cross sectional TEM analysis is best in viewing, on the molecular scale, an oxide. For the purposes of this study cross-sectional SEM analysis has been used to view the cross section of the capacitor test structures. EDAX analysis can also be used to perform a compositional analysis of a sample, also useful in classifying and qualifying an oxide.

II. PROCEDURE

A. Process Details

As this work will fuel research on a VMOS device, a highly doped substrate was chosen due to low series resistance. Unfortunately this limits the C-V measurement capabilities, as quasistatic measurements cannot be obtained if carriers cannot fully recombine. Antimony doped (100) orientation wafers with a resistivity specification of .025-.05 Ohm-cm were chosen due to type and availability.

Positive G-line photoresist (Arch 812) was spun-on using a SVG 88 track coating system. The process consists of a dehydration bake with gas phase introduction of HMDS. The resist is then spun on to a target thickness is 11,600Å. The resist is then soft baked for reflow.

The first level lithography defines the active area of VMOS devices as well as the "pillar" region of the test structure capacitors. The sidewall height and perimeter were eventually used to calculate electrical oxide thicknesses of the etch-profile oxide. The lithography was carried out on a GCA G-line stepper using a clear field quartz mask. Due to the large size of the devices the wafers were intentionally over-exposed to assure total thickness development.

Again the wafers were placed in the SVG 88 track coat system however on the develop track this time. The

resist is developed using a spin-puddle technique prior to hard bake.

The pillar must then be etched. As this study intends to recreate the processes associated with VMOS and finFET devices, a RIE etch is required for adequate sidewall angle. The Drytek 482 quad-chamber RIE system was used. Chamber 2 is used for silicon etching using a combination of SF₆ and CHF₃. This particular chemistry was used in order to obtain an anisotropic profile. The CHF₃ is used in order to create a sidewall polymer to aid in anisotropy. Due to this a substantial post-etch clean is required to remove the polymer. The crystalline silicon was etched to a depth of 2.25µm in order to produce a significant increase in capacitor area for electrical parameter extraction.

Following the etch a modified RCA clean is performed to clean the wafers surface, remove the sidewall polymer, and to create a hydrophobic surface for proper gate oxidation. A 50:1 HF solution was used last in order to remove any oxide grown by the hydrogen peroxide in the APM and HPM baths in order to assure a hydrophobic surface.

Immediately following the RCA clean, the gate oxide was grown using a Bruce horizontal furnace. The tube used was specified solely for dry oxidation, and a Trans-LC clean was performed within one week of the oxide growth. The standard 200Å "SMFL" recipe was used. The wafers were introduced into the furnace at 700°C, and ramped to the process temperature of 900°C. A diffuser was placed on the source side of the quartz wafer boat to aid uniformity.

As to prevent environmental defects from entering the oxide, the wafers were immediately placed in the ASM 6" LPCVD tool. Polysilicon was used as the top contact in order to eliminate the chance of spiking associated with metal top contacts. 3000Å of polysilicon were deposited using SiH₄ at a base pressure of roughly 180mTorr. Again a standard "SMFL" recipe was used with a modified deposition time. The deposition thickness was chosen to run in parallel with similar devices.

Following polysilicon deposition a phosphorous spin-on glass was used to dope the top gate. Phosphorous was chosen as the dopant due to availability and to eliminate the possibility of dopant segregation into the oxide. The phosphorous was spun-on using a manual hand spinner, calibrated with a strobe light at 4500rpm. The dopant was then driven in using the Bruce horizontal furnace n-type tube at 1000°C for 30 minutes.

A buffered oxide etch was then performed to remove the spin on glass. BOE etches thermal SiO₂ at a rate of roughly 1000Å per minute while deposited glass etches faster. The spin-on glass was etched for 12 minutes to assure removal.

A top metal contact of aluminum was then deposited

by sputtering. The CVC-601 upward sputter tool was used after a 3-hour pump down. The cold-cathode type pressure gauge was unable to detect the base pressure of the chamber prior to deposition. A 5 minute 1250W presputter was performed to remove any surface oxide and contamination from an 8 inch Al / 1% Si target. Aluminum was then deposited at 1250W for 15 minutes to a target thickness of 2000Å.

The SVG 88 track coating system was again for resist deposition and development. The second level lithography defines the capacitor top gate and subsequently the area of the capacitors in addition to the contact material for the vertical MOSFET devices. Again the GCA G-line stepper tool was used to expose the wafers.

Hot phosphoric acid at 50°C was used to etch the aluminum. The 2000Å was removed in approximately 2 minutes. A five minute deionized water rinse was performed prior to spin-rinse-drying.

Using the resist and aluminum as a mask, the polysilicon top electrode was then etched using the LAM 490 Autoetch tool. The LAM 490 is an isotropic plasma etching system. The etch was performed in SF₆ at a process pressure of 260mTorr. The etch was completed with endpoint detection with a 40% overetch. The overetch completes the polysilicon etch in addition to creating mesa-type isolation to reduce the overlap fringe capacitance of the test structures.

The resist was then removed in PRS-1000 resist strip at 90°C for 12 minutes. PRS-1000 is a chemical resist strip-removing 1000Å per minute.

Following C-V testing one wafer was sintered at 425°C for 20 minutes in the Bruce horizontal furnace using forming gas (5% H₂ in N₂).

B. Device Testing

The devices were tested using extensive C-V and I-V analysis. Due to the substrate doping level, only high frequency analysis could be performed. The C-V measurements were taken in accordance with the ASTM F1153-92 standard [4]. As with any C-V measurement extensive calibration and zeroing of the metrology system is required.

In order to determine the charge density, often the flatband capacitance and voltage are often required. In order to obtain this, high frequency C-V analysis is performed on all samples. The reciprocal of the square of the normalized capacitance was plotted versus the input voltage. The location knee of this curve occurs at the flatband voltage. Extracting back on a C-V plot the flatband capacitance can be determined [6] see Fig. 1.

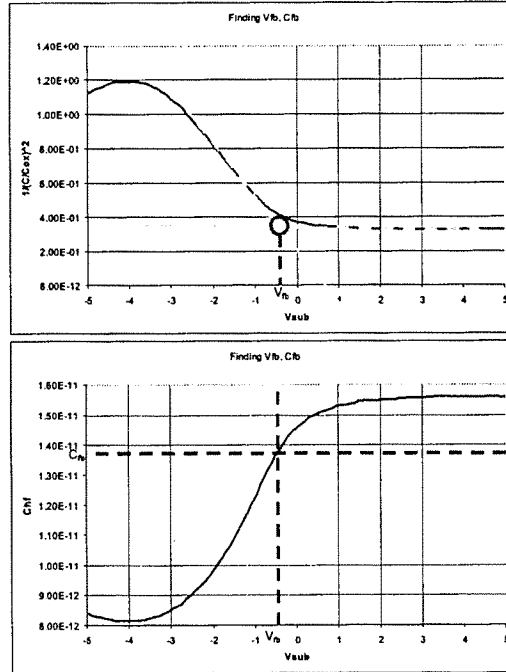


Fig. 2: Flatband extraction

Fixed charge is generally positive stemming from structural damages such as ionized silicon within 2nm of the oxide-semiconductor interface. In order to extract the fixed charge all other sources of flatband shift must be eliminated or reduced. Because of this, a sinter must be performed prior to extraction. The fixed charge can then be characterized by equation 1.

$$Q_f = (\phi_{ms} - V_{fb}) C_{ox} \quad (1)$$

The metal semiconductor workfunction must be known in order to extract data by this method. Using degenerately doped polysilicon as the top gate the metal-semiconductor workfunction can be determined by:

$$\phi_{ms} = \phi_f - 0.56V \quad (2)$$

Oxide trapped charge can be determined by using either the etch-off method or the photo I-V method. However oxide trapped charges are generally only a concern in devices subjected to radiation and electrical stresses.

Mobile charge is extracted using a temperature-bias test. The room temperature – post processing high frequency C-V curves are first obtained. The sample is then heated to 200°C for 15 minutes with a bias of 5V applied. The standard measurement technique requires an applied field of >1MV/cm. The sample is then cooled to room temperature with the bias continuously applied. A repeat of the C-V measurement is done and

the shift is noted. The mobile charge can be determined by equation 3.

$$Q_{ot} = -\Delta V_{fb} C_{ox} \quad (3)$$

Interface charge is often characterized by a change in minimum capacitance between low and high frequency C-V measurements. Due to the substrate doping of these capacitors, a high frequency method must be used. The Terman method is a suitable room temperature, high frequency test. A non-parallel shift in the C-V curve results from the presence of interface trapped charge. This charge can be extracted by the following equation. Unfortunately the Terman method of extraction is limited to interface charge energies away from the band edges. Many interface-trapped charges however reside at an energy state near the band edge.

$$Q_{it} = \frac{C_{ox}}{q} \frac{d(\Delta V_G)}{d\phi_s} \quad (4)$$

I-V analysis is useful in determining the critical field strength of an insulator. To extract the field strength the device under test is placed in series with a large resistance. The potential across the circuit is then ramped to a voltage significant enough to break through the oxide. Plotting current versus voltage a spike in current will be observed (see figure 3) at the point where this occurs. A second voltage sweep can be added to the plot. The difference in voltage between the breaking point and a comparable current on the appended plot is the critical potential drop across the oxide. This divided by the oxide thickness gives the field strength of the dielectric.

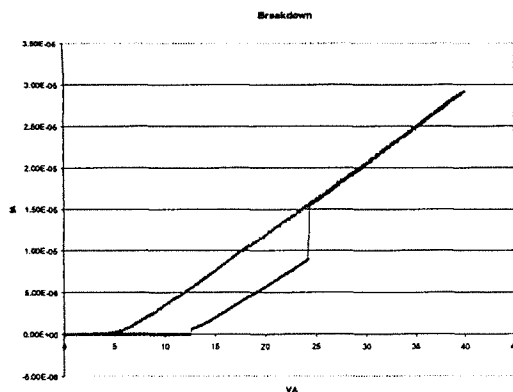


Fig. 3: critical field extraction

C. Cross Sectional Analysis

While electrical oxide thickness can be derived from the accumulation capacitance measured by C-V techniques, it is often beneficial to directly observe the

device under test. In order to view the dimensions of the devices in this study a cross sectional scanning electron microscope is required.

The wafers were cleaved along the <100> direction through the vertical capacitor devices. Cross sectional SEM images were acquired. EDAX analysis was then used to determine bulk as well as film compositions (see Fig. 4).

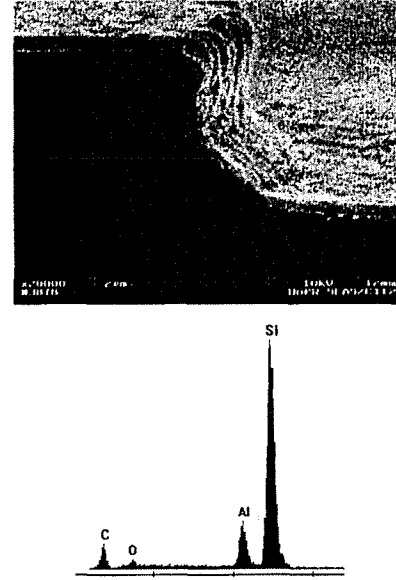


Fig. 4: Cross Sectional SEM and EDAX analysis

III. ANALYSIS

See appendix A for examples of plots obtained.

A formula was derived for extraction of electrical oxide thickness. The resulting thicknesses for multiple vertical shapes are summarized in table 1. The values given is the extracted oxide thickness of the vertical-only regions of the devices.

$$t_{ox} = \frac{k_{SiO_2} \epsilon_o A'}{C_{VMOS-C} - C_{MOS-C}} \quad (5)$$

Shape (perimeter [μm])	Average EOT [\AA]
Circle (200)	57.5
Square (200)	51.6
Diamond (226)	35.8
Square (226)	62.0

Table 1: Electrical Oxide Thickness of Vertical Oxide

Assuming the square-shaped devices are perfectly parallel and perpendicular to the wafer flat, oxidation kinetics suggest that these shapes should have the lowest oxidation rate while the diamond shape, 45° off from the square shapes should have a slightly higher oxidation rate. This is obviously not the case suggesting either a different crystal orientation for each. Notice in figure 4 the spacer-like profile at the bottom of the pillar, the

orientation of this profile could easily alter the extracted thicknesses.

Since all shapes were processed in parallel, on the same substrates, with only crystal orientation as a factor, the orientation must be the source of the electrical oxide thickness variations.

The mobile charge was extracted to be $5.779\text{E}11\text{cm}^{-2}$ which is smaller than reported previously [7]. This is most likely due to the use of a polysilicon top electrode as opposed to an aluminum top electrode used in [7]. The mobile charge was found to be positive suggesting an alkali metal contamination such as Sodium or Lithium. A non-parallel shift was observed during the temperature bias testing suggesting interface trapped charge was also present.

The Terman method of extracting interface-trapped charge yields a value of $2.88\text{E}12\text{cm}^{-2}$, which while high is not outside of the realm of reason. The interface-trapped charge was also found to be positive. As this value is an order of magnitude larger than that of the extracted mobile charge, it follows that metal contamination is not the root cause of interface trapped charge for the vertical capacitors.

Fixed charge was found to be $2.556\text{E}11\text{cm}^{-2}$ suggesting that this charge accounts for the least of the oxide charges. This stands to reason as fixed charge is confined to within 2nm of the silicon-oxide interface, and is generally due to interstitial silicon atoms. However, the sign of the fixed charge is negative. According to [6] fixed charge is always positive, suggesting an error in extraction. This is believable as the error associated with fixed charge extraction derives from error in the metal-semiconductor work function which was calculated based upon the assumption that the polysilicon was degenerately doped, and the substrate was doped at $1\text{E}18\text{cm}^{-3}$.

The field strength of all devices is summarized in table 2. The strength of each oxide is just below 4.0MV/cm . A high quality oxide has a field strength of 10MV/cm suggesting that the etched profile and the charges associated with the oxide weaken the dielectric. While the values reported are low, they may still be suitable for low voltage device operation.

Shape (perimeter)	Square (226 μm)	Diamond (226 μm)	Square (200 μm)	Circle (200 μm)
Avg. Field Strength	3.9MV/c m	3.4MV/c m	3.8MV/c m	3.5MV/c m

Table 2: Field Strength

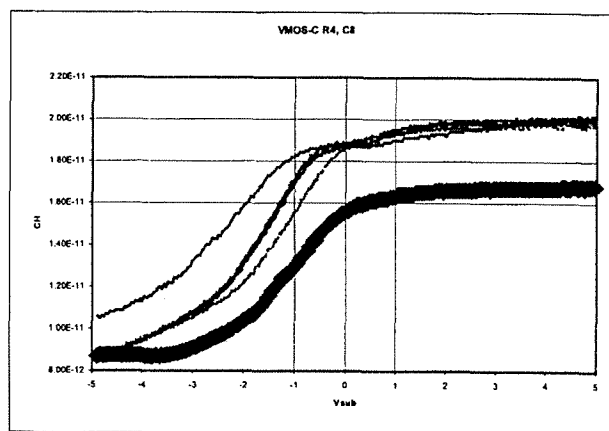
IV. CONCLUSION

Oxides grown on the sidewalls of etched silicon profiles were characterized. The devices showed degraded parameters and increased charge levels when

compared to conventional planar capacitors. The average breakdown strength of the thermally grown oxides are between 3.4MV/cm and 3.9MV/cm . The total oxide charge is on the order of $3\text{E}12\text{cm}^{-2}$. While these values are unacceptable for manufacturing robustness, they are acceptable for low voltage research on advanced structures.

Follow up studies should be conducted to minimize oxide charge and to maximize oxide field strength.

APPENDIX



C-V Comparing Shape

Thick = Flat

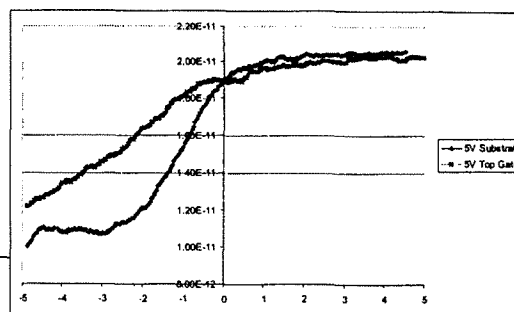
At Center:

Bottom = 200 μm Perimeter Circle

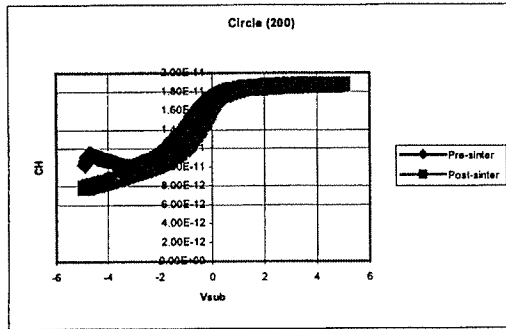
Mid-Bottom = 226 μm Perimeter Square

Mid-Top = 226 μm Perimeter Diamond

Top = 200 μm Perimeter Square



Fixed Charge Extraction



Mobile Charge Extraction

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