# Characterization of Epitaxial Layer Stacking Faults

Alexa M. Perry

*Abstract*—**As device geometries shrink and customer demands for more stringent zero-defect imagers increases, epitaxy growth is becoming an increasingly critical procedure in microelectronic processing. Therefore, the defects manifested by the epi growth are also an important concern. More specifically, epitaxial layer stacking faults can be detrimental to device performance and, in the case of image sensor devices, they have been shown to cause bright pixels and bright columns in the dark field. Assisting the Image Sensor Solutions Division of Eastman Kodak Company, the ability to screen and monitor incoming silicon has been accomplished and assessed using an unpatterned wafer particle inspection system, the Tencor 6220 Surfscan. A technique has been developed to review and characterize the defects mapped by the Tencor 6220. Initial evaluations show that 20% of the light-scattering defects are stacking faults on incoming silicon. Dialogue has improved with the vendors to better align incoming silicon qualification processes with the customer requirements. Incoming silicon qualification procedures have been improved and optimized to reduce any potential yield loss due to incoming silicon defects and stacking faults.**

*Index Terms*—**Epitaxial growth, Epitaxial layers, Incoming Silicon Defect, Stacking Fault**

## I. INTRODUCTION

As device geometries shrink and the need for a defect-free surface increases, epitaxy is becoming an increasingly critical step during microelectronic processing. Therefore, the defects manifested by the epi growth are also an important concern. More specifically, epitaxial layer stacking faults can be detrimental to device performance and the cause of many bright points and bright column failures in charged-coupled devices. Unlike conventional IC or memory circuits, imagers are not redundant, and it is critical from a customer's point of view that the entire image array is working at its full capability.

The purpose of this project is to investigate epitaxial layer stacking faults and methods that are successful in detecting them on image sensor devices. The investigation was completed for the Image Sensor Solutions Division at Eastman Kodak Company. The incoming silicon qualification procedures have been improved and an assessment of the capability of detecting the stacking faults was completed. It has been established that the stacking faults are incoming from the vendor and not process related. Incoming production-quality wafers were the focus of the investigation.

The stacking fault defectivity levels were determined and compared at several critical process steps throughout the process sequence to quantitatively define the defects. Also, the range of defect severity was captured to obtain a better visual understanding of the defects and to, ultimately, perform an electrical test correlation to find the stacking fault defect kill ratio.

One more remaining goal was to have the capability to understand and identify the defects as early on in the process as possible. This allows for proper disposition of lots, so the processing resources can be used to their full potential.

Detection of the stacking faults was first attempted with the KLA Tencor Automated Inspection Tool (AIT). The AIT is a patterned-wafer Surfscan inspection tool in which specific types of defects can be located, based on the tool settings. Certain scan levels are already set up in the process using the AIT, but they are designed to detect particular defects for a particular level. The AIT process scans cannot detect stacking fault defects very well, and the detection capability of the process scan levels was assessed to be very poor.

A better method of detection was verified using the Tencor 6220 Surfscan. The Tencor 6220 is the standard tool for mapping particle defects on bare silicon wafers. It is also the standard tool used by many epitaxial silicon vendors. A recipe was developed on the 6220 tool to detect stacking fault defects in epi layers. The recipe was designed to closely resemble vendor recipe sensitivities. The recipe has proven to be very useful in detecting incoming silicon defects and, more specifically, stacking faults. Characterization and classification of the 6220 particle map defects has been accomplished with an optical review station, the CRS1010. Attempts are underway at optimizing the

Manuscript received May 19, 2003. This work was supported in part by Eastman Kodak Company's Image Sensor Solutions Division.
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current 6220 recipe so that review of the detected bare silicon defects is not necessary. It is desired to have a recipe that yields a known distribution of defects so that the scan can be used for a yield loss predictor before the wafer processing even begins. Also, detecting and characterizing the defects early in the process can result in a measure of yield predictability for a process.

Eastman Kodak Company has opened dialogue with the silicon vendors in an attempt to align the incoming silicon inspection processes. Once conclusive data is collected and analyzed, it is reported back to the vendors. The vendors have, in turn, furnished Kodak with the results from their inspection. This allows the vendor to verify their inspection methods and ensures Kodak the high quality silicon that they desire. Vendors are given the opportunity to improve their process and detection methods to better meet their customer demands. Kodak will also have the ability to pick and choose their vendors of choice based the on defect-yield information.

## II. THEORY

### *A. The Need for Epitaxy*

Epitaxy is extensively used for a variety of semiconductor applications. An epitaxial, or epi, layer is a single poly crystalline layer, usually grown or deposited on a silicon or other substrate. The growth of a thin single crystal film on a crystalline substrate is referred to as epitaxy [1]. The exact meaning of the word "epitaxy" can be found by separating the word. "Epi" means "upon" and "taxis" means "ordered." Therefore, epitaxy is an ordered layer of polysilicon atoms on a single crystal substrate.

The two most common methods used for epitaxy growth are chemical vapor deposition, CVD, or molecular beam epitaxy (MBE). Differing from the Czochralski Si growth process, epitaxy can be grown below the melting point using CVD and MBE. The principle behind CVD is the use of a decomposed gaseous silicon compound vapor to yield elemental silicon and some gaseous byproducts. The epitaxy will grow in the same crystal orientation as the substrate, and the growth rate is a function of the epitaxial temperature as well as the concentration of the gaseous silicon. MBE is similar to CVD in that silicon in the gas phase is decomposed and deposited on the wafers, except the decomposition method is with a molecular beam, and the temperature has less control over the deposition rate. Also, it is more commonly used for the growth of III-V semiconductor compounds on substrates, such as gallium nitride.

Epitaxial film thicknesses can range from about 1 μm to 200 μm, depending on the device application. An epitaxial layer will allow a p-n junction device to be built, without the use of any diffusion properties, by the use of dopant species introduced into the epi layer. The epi layer dopant type and amount can be controlled allowing the resistivity of the film to differ from that of the substrate. This application is more desirable and utilized for special device applications. One such application is solar cells, which make use of the possibility for graded junctions and doping profiles with the epitaxial layer.

A second use of epitaxy is for isolation purposes. The epitaxy is used to totally enclose regions within the silicon substrate that possess a different resistivity than the surrounding regions or devices. Certain transistors and "buried process layers" are fabricated in the overlying epitaxial film, and this provides very efficient isolation between regions of differing conductivities.

Another application for epitaxy is the growth of epi on wafers of sapphire (alumina) and spinel substrates. The sapphire and spinel have similar crystal lattice structures to silicon and the growth of the epitaxy on their surfaces is very high quality. The epi is then used for device fabrication and the substrate acts as an insulating material. The term for growing epi on a foreign substrate is "heteroeptitaxy."

As discussed earlier, and more common for IC fabrication, is the homoepitaxy process. Homoepitaxy, or the growth of an ultra pure layer of crystalline silicon on a silicon substrate, has an important application in IC manufacturing, as device dimensions become smaller and smaller, and the need for defect-free silicon surfaces to build devices becomes more critical. Improved performance of many devices, including CMOS and DRAM, can be achieved by utilizing epitaxial wafers. For CMOS devices grown in epi, compared to bulk silicon, the possibility of latch-up is greatly minimized. DRAM performance is increased by its increased immunity against alpha particles that can wipe out memory cells in bulk substrate wafers by electron-hole pair migration.

Initially selected for its inherent ability to enhance device electrical properties, epi possesses well-controlled dopant concentrations and can achieve a near-perfect crystalline structure [2]. It is the near-perfect surface, free from pits and voids that has driven the popularity for epi wafers. As device geometries are shrinking, the benefits of the low-density killer defect surfaces are more desirable than ever.

Recent improvements and advancements in epitaxy have been in the areas of cost improvement, layer uniformity, and defect reduction [3]. Epitaxial defects will be discussed next.

### *B. Epitaxial Defects*

Because epitaxy has become an important IC and semiconductor process that requires further investigation, the quality and defect severity of the epitaxy is also being investigated. The types and

numbers of epitaxial defects is important for a fabrication laboratory to know and understand such that yield and quality control can be continued during device manufacturing. There are numerous types of defects that manifest and grow during the epitaxy deposition. Epi defects are induced by three methods: crystal imperfections at the substrate epi interface, chemical contamination in the silicon substrate, or by irregular processing conditions within the epitaxial deposition reactor.

The figure below shows five epitaxial defects. Some of the defects manifest in the substrate layer and continue up fault planes during the epitaxial growth, while others result during the epi growth. Of those defects seen in the figure below, the dislocations and stacking faults are the most common that occur during CVD. Most epi defects appear as three-dimensional defects, and they can be attributed to mechanical stress.

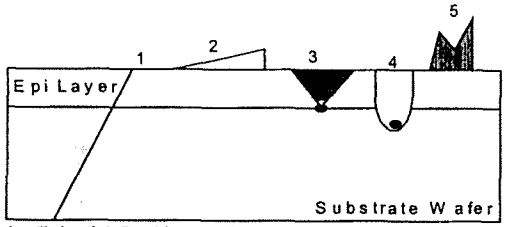


Fig. 1: Epitaxial Stacking Faults. 1. dislocation (continuous from substrate), 2. growth hillock, 3. epitaxial stacking fault, 4. stacking fault (continuous from substrate). 5. epi spike.

The growth hillocks seen above are usually regularly shaped pyramids that grow on the epi surface. They are a result of nucleations at the substrate interface due to various imperfections. Their shape and size are strongly dependent on the off-orientation of the substrate and on the epitaxy process conditions.

An epi spike is often described as a mound or protrusion of irregular shape with a large height but is not correlated with the thickness of the epi layer. The height can be equal to a few micrometers up to more than 100 micrometers.

The substrate stacking fault is a stacking fault in the epi layer that is a continuation of a stacking fault in the bulk substrate material. The final size of the defect depends largely on the epi layer thickness.

*1) Epi Dislocation Defects:* Dislocations in the epi layer are usually the result of the propagation of a preexisting dislocation in the bulk substrate into the epitaxial layer. This process can be influenced by the epi growth conditions, as well as by the thickness of the epitaxial films [1]. Dislocations in the substrate can be terminated by other dislocations and can also change directions to avoid propagating to the epitaxial layer. This is the reason why they are so common. Not as common, dislocations can occur during the process of the epi growth due to the high thermal stresses placed on the substrate and thin film during the epitaxy process. The temperatures in epitaxial reactors can reach up to 1200°C.

*2) Epi Stacking Faults:* Epitaxial stacking faults can come in a variety of shapes and sizes. Typically, they do not grow under thermal treatment and they cannot be removed using conventional semiconductor cleaning methodologies. They are often nucleated at the film-substrate interface and then they propagate in the direction of the growing film. More specifically the nucleation is often a result of a defect or particle on the substrate surface that facilitates the growth of a perturbation during the epi crystal growth process. Four subsequent faults spread in the direction of the four lattice planes of type (111). Thus this is why epi stacking faults appear more commonly as squares, or four faults forming a closed square, on (100) surfaces, but they appear also as triangles on (111) surfaces. Shown below is a three-dimensional picture of a square stacking fault on a (100) surface demonstrating how the stacking fault spreads in the lattice a distance equal to the epi thickness from the initial defect point. Also shown below are top down pictures of a square and triangle shaped stacking faults[4].

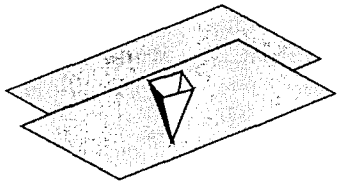

Fig. 2. (100) Silicon epitaxial stacking fault propagating from Si/Epi interface into a closed square shape.

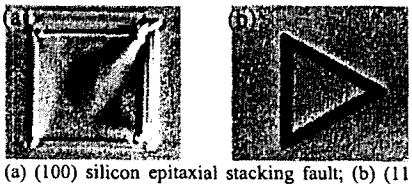


Fig. 3. (a) (100) silicon epitaxial stacking fault; (b) (111) silicon epitaxial stacking fault.[4]

The size of the epi stacking faults is determined by the epi layer thickness above the site of nucleation, and the stacking fault size is proportionally related to the thickness of the epi layer. The equation seen in the figure below is a display of the dependence of the stacking fault size on the epi layer thickness [5]. Not seen in the equation is the dependence of the stacking fault defect topography and height on the size of the initial silicon/epi interface defect. There is a direct relationship between the initial defect size and the amount or height of the stacking fault as it protrudes off of the epi surface. Also as already discussed the shape is determined by the orientation of the crystalline lattice. Epi stacking faults are intrinsic in nature. Although the most often the nucleation site originates at the epi-substrate interface, as will be described next, nucleation

can occur in the middle of an epi layer due to an impurity defect landing on the wafer during the growth process, but this formation is much less common.

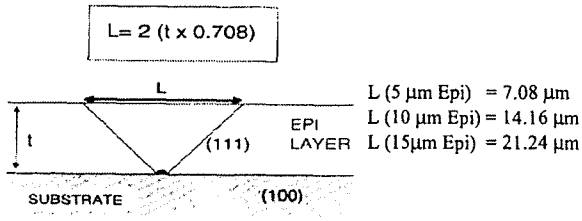


Fig. 4. (100) Silicon epitaxial stacking fault size equation and example calculations. [5]

## III. Experimental

### *A. Defining the Stacking Faults Quantitatively*

Once the possible problem was detected, some work was completed to initially attempt to understand the nature of the stacking faults. It has been verified that the epi layer stacking faults are a specific defect mechanism causing functional failures in the dark field and image failures. There are numerous examples of correlations that Kodak has found between image test review and dark field current maps shown in the Appendix. Shown in the figures below, are examples of an epi stacking fault image failure (bright column) and the corresponding dark field map at that location. The characteristic square nature of the defects was an inherent epitaxial layer stacking fault from a (100) silicon trait. The particular defect seen below had 10 micrometers of epitaxy, and the image defect spans three pixels. The pixel size is 6.8 micrometers so, if the stacking fault is theoretically about 14 micrometers with 10 micrometers of epi then, the number of pixels affected by the defect do correlate to the size of the defect. That is in theory a little more than two pixels should be affected and the figure below shows three bright pixels in a row, which makes perfect sense, because pixels are discrete in nature.

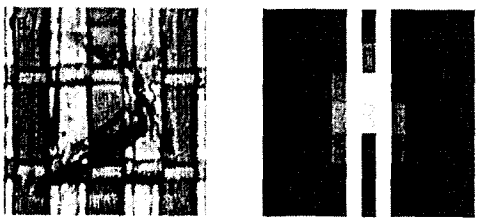

Fig. 5. (a) (100) Silicon epitaxial stacking fault image failure at end of the process; (b) epi stacking fault dark field map of the image failure

To quantitatively characterize the stacking faults an experimental lot was started and initial incoming silicon defects characterized on the CRS1010 after the particles on the bare silicon wafers were mapped on the 6220. Next processing of the lot was started using a standard process flow. The lot was traced through the process characterizing the defects that were detected with the in-line KLA Tencor Automated Inspection Tool, AIT. All of the inherent AIT scan levels were investigated. Also the stacking fault defects that were initially mapped and characterized with the 6220 were inspected and images captured at the various process scan levels. This was accomplished by loading the old 6220 defects maps into the CRS1010 review station, and then the old defect locations were driven to and pictures of the defects captured. The inspections yielded important information on the sensitivity of the inherent process levels scans at detecting stacking fault defects. Also the capability of the 6220 in detecting all of the incoming silicon stacking faults was assessed by overlaying comparing in-line scan defect maps to initial scan maps.

The inspection tools that were used to accomplish the objectives on this experiment are described below. They are the only inspection tools that will be available for use for this project so the 6220 was the tool of choice that was optimized for detecting the epi stacking faults based. The decision was based on tool detection capabilities and sensitivities.

*1) Tencor AIT Scans:* The KLA Tencor is a surface inspection tool that uses a grazing angle laser incident to the wafer surface at about 20° to scan patterned wafers for defects. The tool uses the principle of light scattering to detect and try to classify the size of the defects on the wafer's surface. The laser scans the surface of the wafer and a detector nearby detects any scattered light. Calculating the angle of the incident beam and relating it to the angle of the scattered light determines the size of the epi fault.

The detector sensitivity and beam scan parameters can be modified. This will allow the settings to be optimized for the detection and close monitoring of the epi stacking faults only. Some of the faults are detected in process scans now. Certain in-line process scans are more capable of identifying the faults. Thus incoming silicon inspection capability will be assessed and defect density levels determined.

*2) Tencor 6220 Surfscan:* The Tencor 6220 Surfscan is also a surface inspection tool similar to the AIT and manufactured by the same company, but it is only capable of accurately detecting particles on bare substrates. The difference between the AIT and 6220 is the incident laser light angle. The incident laser on the

6220 tool is perpendicular or 90° to the surface of the wafer. That is why the AIT is incapable of detecting the same defects that the 6220 is on bare silicon wafers. Kodak vendors use 6220 tools for their inspection processes and that seems to be a standard tool used by many incoming silicon qualifiers.

*3) Tencor CRS1010:* The CRS1010 is a confocal microscope inspection system. It is a very powerful confocal microscope that can be loaded with inspection software called Quest. Quest allows one to transfer the wafer particle maps generated by the AIT or the 6220 to the inspection station. The inspection station was thought to only work for patterned wafers with alignment marks, and that is the reason why Kodak was so interested in detection of the faults on patterned wafers at first. Then it become common knowledge that the vendor detection method uses the 6220 so a recipe was developed and a software program wrote to link the 6220 defect map results to the Quest electronic software database. The 6220 and CRS1010 are linked through Quest. With the CRS1010 pictures and true defect sizes can be determined. More accurate defect characterization can be accomplished, not just the defect density. With the current 6220 recipe set up not all of the defects detected are stacking faults, so it is necessary to distinguish and differentiate the epi stacking faults. The CRS1010 makes that possible.

### *B. Develop a Range of Defect Severity*

It is important when trying to understand and characterize the stacking faults that they are quantitatively and qualitatively described. The quantitative and qualitative inspections occurred simultaneously. The severity of the stacking fault defects was correlated using three analytical techniques. Those techniques include the surface inspection using the Tencor 6220 and the AIT, optical inspection using the Tencor CRS1010 system, and electrical and functional test data comparisons. The defect was characterized by defining not only the number of defects and their locations as with the AIT and 6220, but the types and size of defects were also determined. This allowed for both the physical and electrical correlations to be completed. It is important that the incoming silicon is physically compared to the functional test results to determine the detection capability of the defects throughout the process sequence and allow for optimization of the detection methods. With information about the range of defect severity an accurate yield impact analysis comparing both physical and electrical defect results could be completed and the epi stacking faults were thoroughly characterized.

### *C. Identify optimum detection method*

Nearly all wafer inspection methods discussed in section A of the Experimental are accomplished by means of laser and the measurement of the light scattered by the defects. The method of detection that was focused on the most was the laser inspection of the bare silicon image sensors. As already discussed the Tencor 6220 Surfscan, was used to try to detect the epitaxial layer stacking faults for this experiment. A recipe was created and stacking fault defects detection. A remaining problem with the recipe and tool is that not all of the defects detected and mapped are stacking faults or harmful to device performance. The challenge is to optimize the 6220scan recipe for detection of only stacking fault and device "killer" defects as to eliminate the need for the defect review when qualifying incoming production silicon. The optimum detection method and recipe is one that is determined after an electrical correlation is complete comparing end line results with initial 6220 defect results.

## IV. DATA

A large amount of in-process scan data as well as initial defect data has been collected on an experimental lot. The lot is only labeled experimental because the in process inspections are being completed and the lot was stopped at various process steps and thoroughly inspected. Otherwise, the lot is processes using a standard process flow.

Shown in the table below are the 6220 results from the initial bare silicon particle scan. There are eight bin sizes of differing size increments that tries to detect defects between the sizes of 0.16 micrometers to 1.6 micrometers.

TABLE I
TOTAL DEFECTS FROM SURFSCAN 6220 SCAN – LOT 1

| Defect Code | Wafer #3 | Wafer #6 | Wafer #9 | Wafer #12 | Total | % of Tot | Ave. per wf |
|---|---|---|---|---|---|---|---|
| Tiny | 21 | 51 | 18 | 21 | 111 | 64.53% | 27.75 |
| SF | 9 | 4 | 1 | 25 | 39 | 22.67% | 9.75 |
| NVD | 4 | 2 | 9 | 0 | 15 | 8.72% | 3.75 |
| Other | 3 | 2 | 0 | 2 | 7 | 4.07% | 1.75 |
| Total | 37 | 59 | 28 | 48 | 172 | --- | 43 |

Next shown below is the data collected from a composite lot of various vendor lot codes. The wafers were initially scanned and characterized on the 6220 using the first revision of the stacking fault detection recipe. Next the same wafers were scanned and characterized again using two different recipes each of differing sensitivities. The purpose of this attempt was to try and optimize and tailor the 6220 recipe to only detect stacking fault defects. The initial 6220 recipe size bins were broken down into two recipes. The first

recipe trying to detect only particles that were less than 0.21 micrometers and the second recipe wad designed to hopefully only detect defects greater than 0.20 micrometers. There is a slight size overlap, but this was unavoidable because the 6220 tool settings wouldn't allow certain size bins with certain gain sizes. Some of the parameters are interdependent and correlated. This effort was attempted because it was thought that the tiny defects are not killer defects and are detected in the smaller size bins where as the stacking faults are large defects and scatter the laser light intensity differently.

TABLE II
INITIAL TENCOR 6220 STACKING FAULT SCAN RESULTS – LOT 2

| | Total Defects | SFs |
|---|---|---|
| Wafer #2 | 36 | 20 |
| wafer #4 | 18 | 13 |
| wafer #5 | 146 | 19 |
| wafer #6 | 115 | 12 |
| wafer #7 | 59 | 6 |
| wafer #8 | 41 | 10 |
| wafer #9 | 105 | 15 |
| wafer #10 | 85 | 5 |
| wafer #11 | 70 | 14 |
| wafer #12 | 25 | 16 |
| SUM | 700 | 130 |
| Defect Density | 70 | 13 |
| % of Total | | 18.57% |

TABLE III
REVISED TENCOR 6220 SCAN RESULTS – LOT 2

| Lot 2 | SPM5BIN4UP | | | | SPM5BIN3DWN | | | |
|---|---|---|---|---|---|---|---|---|
| | Total Defects | Carry Overs to 3DWN | Not found by 3DWN | SFs | Total defects | new defects | new SFs found | Total SFs |
| wafer #1 | 41 | 41 | 0 | 20 | 80 | 39 | 11 | 31 |
| wafer #2 | 32 | 32 | 0 | 16 | 76 | 44 | 17 | 33 |
| wafer #3 | 75 | 75 | 0 | 21 | 186 | 111 | 12 | 33 |
| wafer #4 | 17 | 17 | 0 | 12 | 43 | 26 | 6 | 18 |
| wafer #5 | 119 | 107 | 12 | 18 | 223 | 116 | 10 | 28 |
| wafer #6 | 97 | 91 | 6 | 8 | 200 | 109 | 13 | 21 |
| wafer #7 | 44 | 42 | 2 | 3 | 95 | 53 | 15 | 18 |
| wafer #8 | 29 | 29 | 0 | 6 | 74 | 45 | 11 | 17 |
| wafer #9 | 80 | 80 | 0 | 10 | 172 | 82 | 11 | 21 |
| wafer #10 | 46 | 44 | 2 | 5 | 164 | 120 | 8 | 13 |
| wafer #11 | 51 | 47 | 4 | 8 | 114 | 67 | 11 | 19 |
| wafer #12 | 17 | 17 | 0 | 10 | 39 | 22 | 15 | 25 |
| SUM | 648 | 622 | 26 | 137 | 1466 | 834 | 140 | 277 |
| Defect Density | 54.00 | 51.83 | 2.17 | 11.42 | 122.17 | 69.50 | 11.67 | 23.08 |
| % of Total | | | | 21.14% | | | | 18.89% |

The next set of data shown below is the initial attempt to align and verify that Kodak inspections methods match and detect the same amount of defects as the vendor. So wafers that the vendor characterized were characterized again using Kodak improved incoming-silicon qualification methods and the results compared.

TABLE IV
CORRELATION OF WAFERS OBTAINED FROM VENDOR

| Wafer | Vendor 2: SF's/Total Defects | Kodak: SF's/Total Defects |
|---|---|---|
| 1 | 13/13 | 12/17 |
| 2 | 3/3 | 3/7 |
| 3 | 9/10 | 8/13 |

Lastly, data was collected to compare two vendor facilities. A vendor recently established a new facility with differently designed epi reactors and wanted Kodak to compare their current facility, facility 1, with the new expected "cleaner" facility, facility 2. The results of the 6220 scan and defect classifications are shown in the figure below.

TABLE V
VENDOR FACILITY SPLIT DATA AFTER CLASSIFICATION – LOT 3

| Facility 1 | | | | | |
|---|---|---|---|---|---|
| Slot # | Tiny | SF | NVD | Other | Totals |
| 9 | 1 | 3 | 0 | 0 | 4 |
| 10 | 2 | 4 | 0 | 1 | 7 |
| 11 | 0 | 4 | 0 | 0 | 4 |
| 12 | 1 | 10 | 0 | 0 | 11 |
| 13 | 0 | 5 | 0 | 0 | 5 |
| 14 | 0 | 4 | 0 | 0 | 4 |
| 15 | 5 | 9 | 0 | 0 | 14 |
| Totals | 9 | 39 | 0 | 1 | 49 |
| Defect Density | 1.29 | 5.57 | 0.00 | 0.14 | 7.00 |
| % of Tot Defects | 18.37% | 79.59% | 0.00% | 2.04% | --- |

| Facility 2 | | | | | |
|---|---|---|---|---|---|
| Slot # | Tiny | SF | NVD | Other | Totals |
| 16 | 0 | 0 | 9 | 1 | 10 |
| 17 | 0 | 2 | 0 | 0 | 2 |
| 18 | 0 | 0 | 0 | 0 | 0 |
| 19 | 0 | 0 | 1 | 0 | 1 |
| 20 | 0 | 1 | 2 | 0 | 3 |
| 21 | 23 | 1 | 3 | 2 | 29 |
| 22 | 0 | 0 | 3 | 1 | 4 |
| 23 | 0 | 0 | 1 | 0 | 1 |
| 24 | 13 | 0 | 3 | 7 | 23 |
| 25 | 2 | 0 | 14 | 0 | 16 |
| Totals | 38 | 4 | 36 | 11 | 89 |
| Defect Density | 3.80 | 0.40 | 3.60 | 1.10 | 8.90 |
| % of Tot Defects | 42.70% | 4.49% | 40.45% | 12.36% | --- |

Next for completeness, a scanning electron microscope was used to image two different stacking fault defects detected at different points in the process by the in-line AIT scans. The resulting SEM images are shown below. One notices the difference in topography between the two defects. The topography difference can be accounted for by the size of the initial particle defect on the silicon substrate/epi interface that causes the stacking faults. The right most stacking fault probably propagated from a much larger diameter defect than the stacking fault defect on the left.

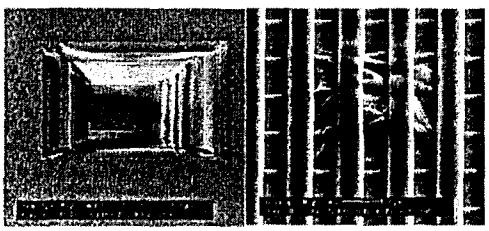

Fig. 6. SEM pictures of stacking faults.

## V. Results Analysis

Shown below is a graphical analysis of the resulting AIT in process scan results. The data being represented in the bar graph is only stacking fault defects detected at the various scan levels and comparing those numbers to the number of initial stacking fault defects detected with the 6220. The raw data is shown in the appendix, Table VII. Interpreting the graph one can see the 6220 scan yields the greatest sensitivity to the stacking fault defects. The same information is broken out in Table I above, where all of the 12 wafers were characterized on the optical review station. From the initial 6220 scan results about 22% of the total initial defects detected were stacking faults or nearly 10 per wafer. This is very close to the present vendor specification, so the incoming silicon is nearing the upper specification limit for non-removable light scattering defects. Looking at the individual process scan levels, no one scan level detects 100% of the stacking faults initially detected with the 6220. The best scans, scan 5 or scan 6, only detected ½ of the initial defects.

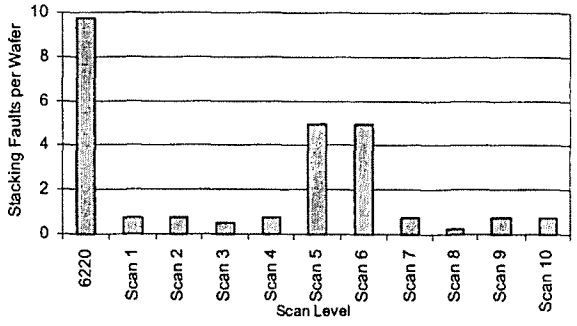


Fig. 7. Stacking fault defect density for AIT process scan levels.

Fig.s 8, 9, and 10 below are examples of stacking fault defects that were traced through the process. Most but not all of the pictures were taken in a 200 micrometer by 200 micrometer field of view. The defects seen in Figs. 8 and 10 were detected at all of the process scan levels shown. This differs from the defect in Fig. 9, which was only detected with the 6220 Surfscan. The remaining scan level pictures in Fig. 9 were obtained by locating the defect at the scan level using the old 6220 scan x, y coordinates. The defect didn't scatter enough laser light in the AIT to be detected like the defect seen in Fig. 8 or Fig. 10.

One other point to make is the size discrepancy between the defects in Figs. 8 and 9 compared to the defect in Fig. 10. This size difference is due to the fact that Kodak sent wafers with 10 micrometers of epi to the vendor to grow an additional 5 micrometers of epi based on a design need. So, the defect in Fig. 10 manifested from the additional epi growth, but the other two defects seen below propagated form the first epi growth.

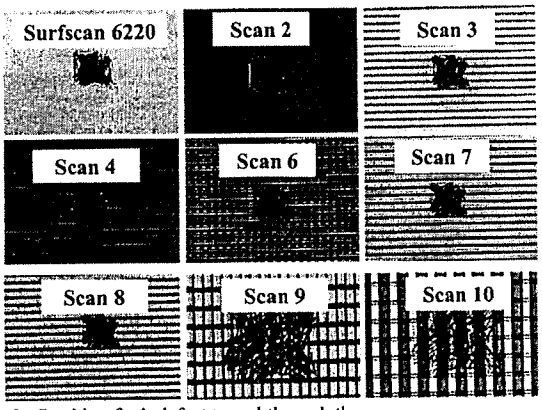


Fig. 8. Stacking fault defect traced through the process.

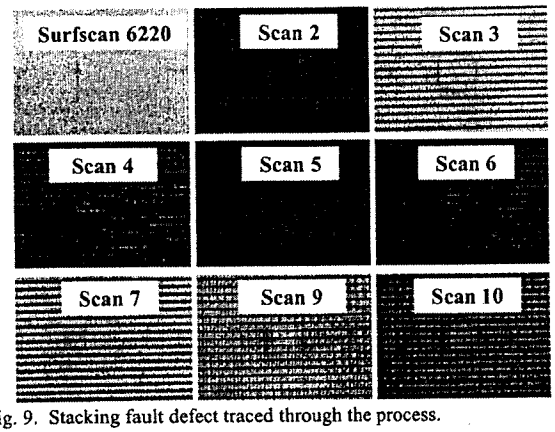


Fig. 9. Stacking fault defect traced through the process.

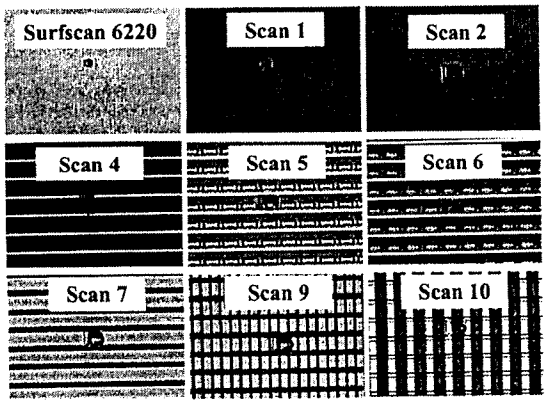


Fig. 10. Stacking fault defect traced through the process.

The next tables shown in the data section above represent the attempts made on lot 2 to optimize the 6220 scan. Table II is a display of the classification results from the standard stacking fault recipe designed, and again only about 20% of the total defects detected were stacking faults. Table III is a break down of the results after modifying the original 6220 scan. Neither of the new scans proved to be more efficient at only detecting the stacking faults and not detecting any of the smaller tiny defects that are known to not be harmful to device performance. For either scan iteration only about 20% of the total defects were stacking faults. Tailoring the scan will be attempted again in the near future.

The data seen in Table IV is an example of Kodak trying to align their inspection system with the vendor inspection system. On each of the three wafers seen, Kodak's scan picked up slightly more total defects than the vendor. All but two of the stacking faults that the vendor found were detected using Kodak's inspection technique. Kodak's 6220 scan may be slightly more sensitive to smaller particles on incoming wafers, because particles down to 0.16 micrometers are attempted to be detected, versus the vendors scan that only detects down to 0.18 micrometers.

The most impressive set of data to the vendor and even Kodak is seen in Table V above. This data is from a vendor lot split between facilities. The number of stacking fault defects per wafer for the facility one and facility two is 5.4 and 0.4, respectively. That was good news to the vendor when they received feedback from this data, because it proved to them that their facility 2, with the newly designed reactors was "cleaner" with lower stacking fault defects than their standard facility, facility 1. The vendor has expressed a willingness to upgrade the equipment in their older facilities to match the improved performance.

## VI. Conclusion

It has been established that the stacking faults are incoming and not process related. The first attempt at detecting the stacking faults on bare silicon wafers was ineffective using the KLA Tencor Automated Inspection Tool (AIT), designed for patterned wafer inspections. The standard vendor particle inspection system for bare silicon wafers, the Tencor 6220 Surfscan, is capable of detecting the stacking faults, and a recipe and scan method has been developed and implemented. Initial evaluations show that 20% of the light scattering defects on incoming silicon are stacking faults.

Once the initial bare silicon scans were completed the 6220 wafer maps were inspected and defects classified using techniques developed for the optical review station. Sensitivity of the inherent process scans has also been assessed. None of the current process scans detect 100% of initial stacking fault defects. The best scan detected only ½ of the initial defects. There are a few outstanding issues including the electrical test correlation with initial scan results, and optimization of the 6220 scan recipe. Improved communication with the vendors has helped in aligning vendor and customer incoming silicon inspection processes, all in an effort to aid the vendors in better serving Kodak's Image Sensor Solutions Division.

## APPENDIX

- Capable of 2" -8" wafers.
- Patterned surface Inspection System.
- 0.09 micron Defect Sensitivity @ 80% capture, based on PSL Standards. 0.02 ppm Haze Sensitivity, 0.002 ppm Haze Resolution.
- Accuracy within 1%.
- XY coordinates.
- Argon Ion laser.

Fig. 11. Tencor 6220 Surfscan tool specifications.

TABLE VI
WAFER SPECIFICATIONS

| PROPERTY/ CHARACTERISTIC | SPECIFICATION |
|---|---|
| SUBSTRATE | |
| Dopant Type | p-Type |
| | The amount of dopant of the opposite type to the specified dopant must be less than 1% of the specified dopant level, and never exceed $10^{12}$/cm3. |
| Dopant | Boron |
| Resistivity | 0.01 - 0.02 -cm |
| Orientation | <100> |
| EPI LAYER | |
| Thickness | 14.0 - 16.0 μm |
| Dopant Type | p-Type |
| Dopant | Boron |
| Resistivity | 5.0 - 6.0 -cm |

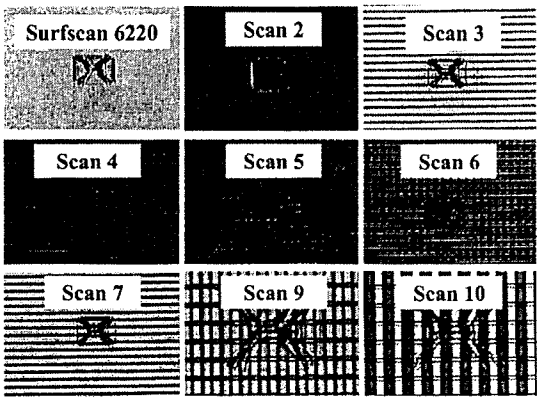


Fig. 12. Stacking fault defect traced through the process.

TABLE VII
STACKING DEFECTS A ALL SCAN LEVELS

| Scan Level | Wafer #3 | Wafer #6 | Wafer #9 | Wafer #12 | Total | Total per wf | Scan Visibility % of Initial Tot (39 defects) |
|---|---|---|---|---|---|---|---|
| 6220 | 9 | 4 | 1 | 25# | 39 | 9.75 | --- |
| Scan 1 | 0 | 2 | 0 | 1 | 3 | 0.75 | 7.69% |
| Scan 2 | 0 | 2 | 0 | 1 | 3 | 0.75 | 7.69% |
| Scan 3 | 0 | 2 | 0 | 0 | 2 | 0.5 | 5.13% |
| Scan 4 | 0 | 2 | 0 | 1 | 3 | 0.75 | 7.69% |
| Scan 5 | 2* | 2 | 0 | 16** | 20 | 5 | 51.28% |
| Scan 6 | 2* | 2 | 0 | 16** | 20 | 5 | 51.28% |
| Scan 7 | 0 | 2 | 0 | 1 | 3 | 0.75 | 7.69% |
| Scan 8 | 0 | 1 | 0 | 0 | 1 | 0.25 | 2.56% |
| Scan 9 | 0 | 2 | 0 | 1 | 3 | 0.75 | 7.69% |
| Scan 10 | 0 | 2 | 0 | 1 | 3 | 0.75 | 7.69% |

*new SF defects not picked up by 6220

**14 SF defects overlay (picked up) to 6220,
2 new SF defects not picked up by 6220

# 6 SF in streets so won't be picked up by future scan levels

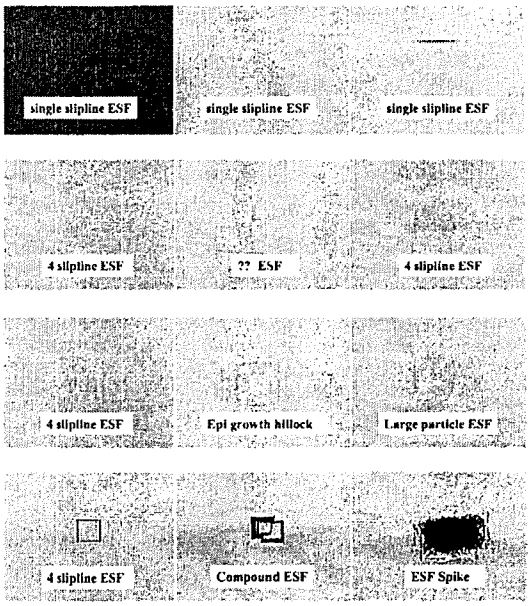


Fig. 13. Range of stacking fault of progressive severity.

## ACKNOWLEGMENTS

A. M. Perry would like to thank Mr. Dean Seidler, Dr. Marc Hunt, Mr. Justin Winter, Dr. Wesley Miller, Mr. Scott Walton, Dr. William McColgin, and Mr. Mike Hanrahan all from the Image Sensor Solutions Division at Eastman Kodak Company. Thanks also go to Dr. Richard Laneand Dr. Santosh Kurinec of the Department of Microelectronic Engineering at the Rochester Institute of Technology.

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