Simulation and Modeling of a Vertical PMOS Transistor

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Abstract— **Conventional planar CMOS scaling is able to achieve the traditional 17% performance gain for generation to generation. Planar CMOS scaling will soon encounter a "red-zone" at 65nm node or lower as we proceed towards the road map. As a result, the industry is likely to adopt a non-planar, fully depleted structure of various geometries including finFET, double-gate planar MOSFETs and vertical MOSFETs that are being investigated. This study focuses on Silvaco simulation and modeling of vertical P-type MOSFETs. The goal of this project was to determine whether Silvaco adequately, models degenerate doping levels (e.g. delta doped region) to minimize the antipunch through effect in short channeling. Preliminary results show that the mesh sizing in the localized highly doped regions is critical for successful simulation. Specifically it is important to generate a localized mesh of approximately 10 points per Debye length. Results indicate the Silvaco software in not able incorporate exact modeling for delta-doped region.**

Index Terms—**Device Modeling, Vertical MOSFETs**

I. Introduction

THE objective of the project was to design and model the vertical MOS transistor. The project was involved in simulation and modeling of vertical MOSFET (V-MOS) transistor for investigating the device structure and its properties. These are new type of devices that show better overall performance gain when scaling is done bellow 65nm nodes. It also offers lower cost and ease of fabrication by elimination of several masking steps from the fabrication standpoint. The layers of the device structure in Athena model were stacked on the silicon substrate using regular deposition instead of layer grown using molecular beam epitaxy. The temperature for such epitaxial layer was not accounted for diffusion in the Athena model.

The project was not successful for complete modeling of device as initially planned as we encountered difficulties with the Silvaco when modeling the delta-doped region.

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Without the incorporation of delta doping, we experienced large leakage due to punch through that caused failure in measuring important device properties such as threshold, substhreshold swing, Drain Induced Barrier Lowering DIBL. One of the challenges that are expected is how accurate the theoretical model will present the real model and if that model will be able to manufacture in current state of the art facilities.

II. Theory

The device structure for the VMOS is shown in Figure 1. The structure was assumed ideal for the simulation purposes. This is the Athena model did not assume the growth of the layer from epithaxial growth; instead the layers were stacked directly on the silicon substrate followed by dry etching. The channel length was set to be 65 nm, lightly doped N-type (phosphorous) at 10^{15} cm^3. The source and drain were set to 10^{20} $cm^{3,}$ with the extension at 10^{18} cm^3. The delta-doped regions were set to 10^{20} cm^3 with 3nm thickness. The gate material used was Aluminum with oxide of 3 nm. The device structure is shown in Fig.1.

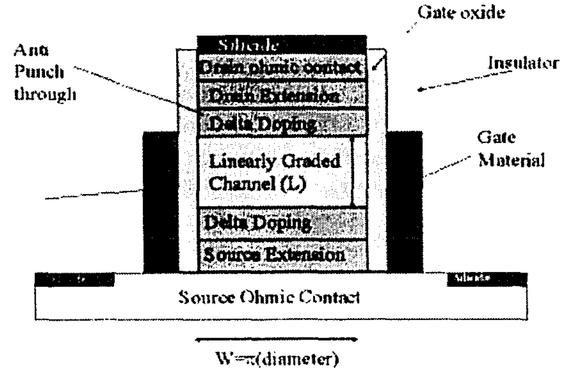


Fig. 1. Schematic representation of VMOS Device Structure

Simulation will reveal if the Silvaco software gis capable of giving accurate results and its limitation.

Tabakman and Rommel [6] reported complementary work for a vertical N-MOS transistor. After the individual devices (Vertical N and P MOS) will yield promising device performance, the work will be extended to vertical CMOS.

II. EXPERIMENTAL

Initially, the model for Athena could not make the device structure. The Athena model for the vertical NMOS prepared by Tabakman and Rommel was used. We chose three device properties for simulation to characterize the doping concentration in the channel and the source and drain. These properties were threshold, DIBL, and the family curves I-V curves for subthreshold slope and subthreshold swing measurements.

Simulations were done using different device width varying from 200 nm to 45 nm width. The channel length was set constant to 65 nm. The target was to find the doping concentration in the channel to obtain a threshold as low as –0.5 V. The other two parameters, DIBL and family curves were calculated with different doping at the channel doping and corresponding width of the device structure (pillar).

III. ANALYSIS

Result from the simulations indicate that the Silvaco was not able to model delta doped region accurately. In varying the channel doping from 10^{14} cm^3 to 5×10^{17} cm^3, we observe very minimal changes in threshold voltage for devices with the delta doping in the device structure. The threshold for these device structures was as high as –2 V and would increase even higher close to –3 V when meshes were shrinked to the smallest sizes of ~ 3 A. This infers that the Silvaco is not modeling the delta-doped region. There could be a possibility that the Silvaco tool is not considering the delta doped region as a tunneling barrier but instead a part of the channel region that is highly doped; therefore larger threshold accounts for inverting highly doped region.

The comparison for threshold voltages extracted from the simulation for device structure with and without delta doping regions is shown below.

Fig. 2 Simulated I_{DS}-V_{GS} characteristics for a P-VMOS device with d-doped regions.

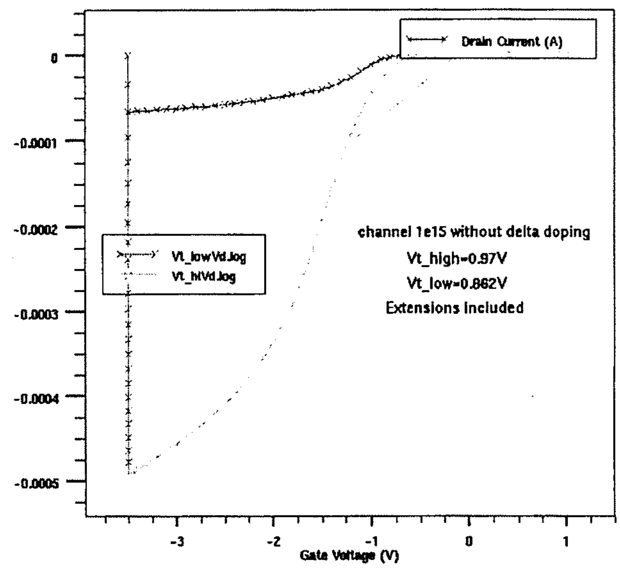
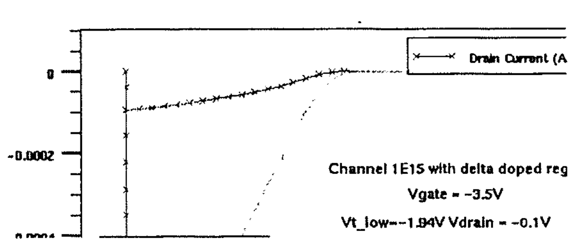


Fig.3. Simulated I_{DS}-V_{GS} characteristics for a P-VMOS device without δ -doped regions.



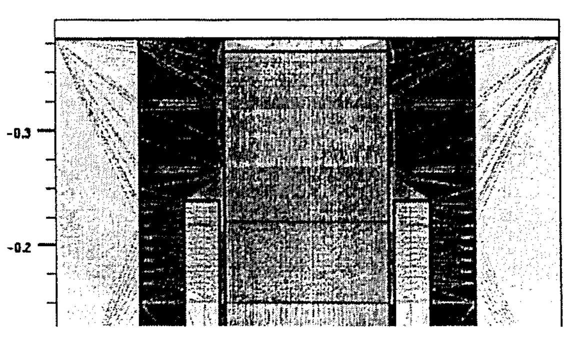


Fig. 4. Mesh distribution for a P-VMOS device. Note an increase in the node density at the δ-doping regions.

The definition of nodes was very critical in modeling the device particularly the delta-doped region. The mesh distribution was densely concentrated at the channel region and delta-doped region where the device characteristics such as threshold were modeled. The rest of the device structure near the gate, and isolation oxide had minimal distribution of mesh since theses were the areas in the device structure where no device properties were calculated. The diagram below shows how the mesh distributions were distributed.

Comparison for devices with and without delta doping, at different channel doping and width of device indicate huge difference in device properties such as threshold, DIBL.

The lack of modulation in drain current with respect to gate bias suggests (i) high leakage due to punch through (ii) improper definition of mesh conditions. Due to the fact that a similar designed model by K.Tabakman show successful simulation for vertical NMOS. We theorize that meshing distribution needs to be redesigned in this study.

Specifically the mesh should be set to 1/10 of the Debye length of the delta doping; we may accurately model the delta doping and the rest of the devices. With the doping concentration of channel and delta doped region, The Debye length for channel and delta doped region is $750A^{o}$ and $3A^{o}$. The smallest mesh in our simulation in Silvaco was $5A^{o}$ that was successful in Athena and Atlas tool. Beyond that, the tool did not support smaller meshes because Silvaco tool have definite amount of nodes it can allow (~3000 nodes) in each Athena model. This necessitates to carefully understand the manual and look for other option Silvaco offers that can model the delta-doped regions. One of the possible options is to look at the Quantum Mechanics option in Silvaco tool, which may able to realize the delta-doped region as a tunnel barrier instead of a highly doped channel region. This may remove the constraints for smaller meshes. The other is to use the Devedit tool, which allows localizing meshes that Athena does not allow.

IV. CONCLUSIONS

Preliminary simulation indicate the delta-doped region were not successfully modeled the by Silvaco. There is a need to look other options Silvaco can offer to model the delta-doped regions, that are very important for the device to perform successfully. Without the delta-doping region, the complete modeling of the device may not be possible due to large leakage induced by punch through. These leakages is high enough for the device not to function normally.

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