

Development of a Polycrystalline $\text{Si}_{1-x}\text{Ge}_x$ Gate Material by LPCVD/PVD

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Abstract— Polycrystalline $\text{Si}_{1-x}\text{Ge}_x$ (poly Si-Ge) was explored as a process compatible alternative gate material for PMOS transistors at RIT. This material has been previously shown to exhibit several favorable characteristics when used as a gate material for PMOS transistors. Benefits include the ability to engineer the workfunction, improved dopant activation for reduced gate depletion effects, and reduced boron encroachment.

A process by which poly Si-Ge could be integrated as a gate material into the RIT submicron CMOS process was developed by alternating polycrystalline silicon deposition by LPCVD and the application of germanium by PVD. The effects on physical composition of the gate stack and an attempt to understand germanium diffusion through polysilicon was also explored.

Index Terms—Poly Si-Ge, germanium, diffusion, gate depletion, boron

I. INTRODUCTION

WITH the ever decreasing geometries of today's modern CMOS devices it has become necessary to engineer the gate electrode characteristics to ensure reliable and desirable transistor electrical performance. It is desirable for a CMOS process to have threshold voltages (V_T) that are equivalent in magnitude for both NMOS and PMOS transistors. This is known as a balanced V_T design and simplifies inverter operation, the basic building block of digital logic. The use of dual gate polysilicon CMOS processes has allowed for better metal-semiconductor workfunction (Φ_{ms}) matching for the respective NMOS and PMOS transistor V_T [1]. By doping NMOS gates as n+ and PMOS gates as p+ balanced threshold voltages can be achieved. The incorporation of p+ doped polysilicon for PMOS transistors also results in a reduced need to perform p-type dopant threshold adjust implants, reducing process complexity. The use of a p+ poly gate in PMOS technology enables operation as a surface channel transistor as opposed to buried channel operation allowing for improved performance as the gate can

retain more control over the channel region [2]. Introduction of dual gate technology does increase the process complexity of CMOS by requiring separate doping of the gates, usually accomplished by masking of either NMOS or PMOS using a lithography process, which in turn introduces an additional mask level. As RIT's Semiconductor & Microsystems Fabrication Lab (SMFL) continues to scale devices into the submicron regime it is desired to eventually move to a dual gate process. To this end poly Si-Ge is investigated as a material that could be used in a future RIT dual gate process. Poly Si-Ge has been shown to be easily formed in a LPCVD reaction by mixing SiH_4 and GeH_4 gases [3]. Since GeH_4 gas is not available in RIT's SMFL facility and alternative approach of producing the film by germanium PVD is explored.

II. BACKGROUND

MOSFET gate electrodes have been traditionally composed of highly doped polycrystalline silicon [4]. Polycrystalline silicon gates have the advantage of being compatible with existing process steps, the ability to be easily doped, and provide a good interface with silicon dioxide, the dominant MOS dielectric material. Poly Si-Ge material has been shown to share many of these properties [5]. At the sub 250nm node there could be benefits to moving from a polysilicon based dual gate process to one using poly Si-Ge. These benefits include improved resistance to gate depletion effects, reduction of boron penetration of the gate oxide, as well as offering some degree of work function engineering and remaining fairly process compatible.

A. Gate Depletion Effects

As effective gate lengths shrink to dimensions where short channel effects (SCE) begin to become significant doping in the channel regions must be increased in order to counteract these effects [6]. SCE can lower the effective V_T of the transistor, known as V_T roll-off, leading to higher off-state leakage (I_{OFF}). For a PMOS device this could be offset by decreasing the doping of the gate in order to increase the magnitude of the V_T . Decreasing the gate doping level has subsequent effect of reducing the amount of dopant available for activation within the gate. If an insufficient level of

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dopant becomes active in the gate then the formation of a strong inversion region in the channel can act to deplete carriers from the gate-insulator interface. This depletion acts to increase the inversion capacitance. This increase results in a reduced level of control over the channel by the gate electrode and effective drive current is reduced. This is known as the gate depletion effect (GDE). Poly Si-Ge has been empirically shown to have a higher level of dopant activation for p-type dopants, such as boron, due to increased grain size and a lower number of trapping states which allows for a lower potential barrier for carriers within the gate [7].

B. Boron Penetration

In order to reduce possible gate depletion effects it is necessary to increase gate doping with each subsequent generation of CMOS. Boron is the dominant p-type dopant species and has the tendency to diffuse quickly through polysilicon as well as easily through thin oxides such as the underlying gate oxide. This diffusion can lead to reliability and performance degradation as trapped boron in the oxide causes defect sites, leading to accelerated dielectric failure. The additional boron in the channel region leads to V_T variations along the channel length. These variations in V_T result in undesirable shifts in drive current and transconductance, thus reducing overall transistor performance [8]. P+ polysilicon also has a limit to the practical level of boron activation. Poly Si-Ge has a higher boron activation rate allowing for reduced gate doping levels which will result in reduced boron penetration.

C. Work Function Engineering

Silicon and germanium exhibit similar electron affinity values, 4.05eV vs. 4.00eV respectively. There exists however a significant bandgap difference between the two materials, 1.12eV vs. 0.66eV at room temperature. A fractional solution of these two elements as investigated in this paper will result in a bandgap that lies between these two values [9]. Several models have been put forth on the exact representation of this bandgap but it can be safely assumed that the bandgap of poly Si-Ge is greater than pure germanium and less than pure silicon. The result of this delta is the ability to change the overall effective bandgap of the gate material by altering the fractional amount of germanium [10]. Thereby the work function becomes a function of germanium concentration. The work function (Φ_{MS}) of a material is defined as the distance from the vacuum energy level to the Fermi level [11]. As seen in fig. 1 due to the similarity in electron affinity the Φ_{MS} for a n-type gate will shift very little by the substitution of poly Si-Ge. However the Fermi level of a degenerately doped p-type poly Si-Ge gate will lie within the forbidden region of polysilicon allowing it to be a mid-gap gate material for PMOS.

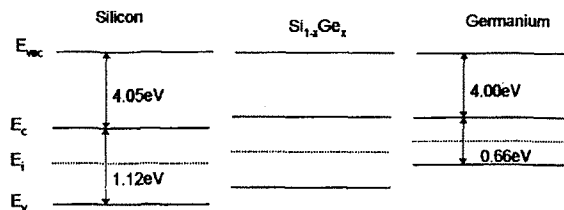


Fig. 1. Work function differences between Si, Ge, and Si-Ge. The material retains a similar electron affinity to polysilicon while shifting the valence band resulting in a shift in Φ_{MS} for p-type gates.

D. Process Compatibility

The successful inclusion of any material into the relatively complicated process of an integrated circuit manufacturing environment lies in its ability to remain compatible with existing process steps. Poly Si-Ge in this regard retains many of the qualities of polysilicon. There are some important differences however that should be considered from a process engineering perspective. The effective RIE etch rate of poly Si-Ge has been shown to be faster than that of polysilicon using the same etch chemistry and is a function of germanium concentration [12]. Care must be taken during wet clean operations as oxidizing agents such as peroxides are reactive with poly Si-Ge and result in its removal. Therefore a standard RCA clean operation can not be performed on a wafer with exposed poly Si-Ge. The effective melting temperature of poly Si-Ge is also reduced compared to that of polysilicon [13]. Due to the increased dopant activation rates this is likely not a significant issues as the thermal budget can be reduced accordingly and still result in increased activation levels.

III. EXPERIMENT

A. Process Overview

In order to fulfill this experiment several (100) n-type device grade wafers were obtained along with several dummy wafers of various doping types and concentrations. In an effort to prepare the device wafers for eventual use as C-V test vehicles a backside doping of P₃₁ was performed to facilitate a better ohmic contact to the backside. To this end a 1000Å screen oxide was grown in Dry O₂ at 1000C. A software package was used to identify and simulate an appropriate ion implantation acceleration voltage, determined to be 100keV with a targeted dose of $1 \times 10^{15} \text{ cm}^{-2}$. After implantation the wafers were annealed for 15 minutes in N₂. A subsequent 2 minute dip in HF served to remove the screening oxide. A standard RCA clean was used to prepare the device wafers surface for thin gate oxide growth. Immediately after completion of the RCA clean process the device wafers were inserted into a Bruce furnace system with a targeted dry O₂ oxide growth of

100Å. The actual oxide thickness as measured by an automated ellipsometer was 130Å.

Polysilicon was deposited on both device and dummy wafers in an LPCVD system with a targeted thickness of 1500Å. This was followed by a layer of germanium intended to be 1316Å deposited by PVD. Finally wafers were inserted into the LPCVD system again for an additional deposition of polysilicon in an attempt to bring the total stack height to 6000Å. Using the respective atomic volumes of silicon and germanium this was calculated to result in a film composition of $\text{Si}_{0.8}\text{Ge}_{0.2}$, shown to be an optimal fractional solution [14]. Due to an anomaly on the tool during the second polysilicon deposition was only measured 1470Å rather than the desired 3100Å. A portion of the wafers with the full stack of polysilicon-germanium-polysilicon was then annealed at 900C in a N_2 ambient to promote diffusion of the Germanium into the polysilicon.

B. Germanium Deposition Detail

Experience in RIT's SMFL facility was fairly limited in regards to germanium sputtering [15]. As little data existed on expected deposition rates it was desired to determine this parameter for future use in the facility. Previous experience with germanium targets had shown them to be fragile at DC power of greater than 75W. Therefore initial sputter depositions were attempted at 15 and 50 watts of DC power. It was decided that the rate at 15W was lower than desired for the eventual thickness of the film that needed to be put down on the wafers. At a pressure of 5.3mTorr and 50W of power a deposition rate of approximately 40Å/min was achieved. This rate was found by measuring the step height profile of 15 minutes of deposited germanium. The step was defined by a stripe of resist coated onto a dummy wafer and hard baked at 120C. An acetone lift off process allowed for superior edge definition compared to earlier attempts at step height measurements using Teflon tape. The original germanium target on hand for this experiment was destroyed after the application of 1000W of DC power in an event outside the scope of this paper. A replacement target was sourced and acquired for the completion of this project.

IV. RESULTS

Two method of analysis were attempted in order to determine the success of forming poly Si-Ge. This included Auger surface analysis and XRD. Time did not permit the inclusion of a more detailed RBS/SIMS compositional analysis of the film stack. Pre and post-anneal wafers were submitted for Auger on the toolset present at RIT. A pre-anneal wafer was examined and compared to a standard polysilicon wafer by XRD in RIT's Advanced Materials Laboratory. The Auger spectra can be found in fig. 2 & 3.

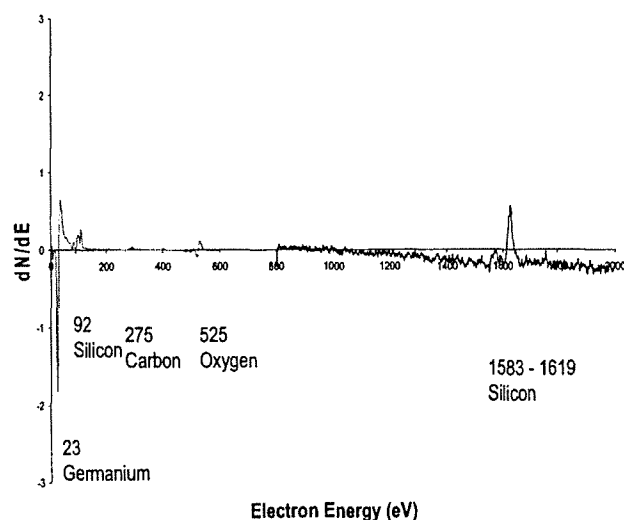


Fig. 2. Pre-Anneal surface Auger results. Appearance of germanium signal shows some fraction of germanium was able to diffuse from center of film stack to surface at LPCVD temperatures.

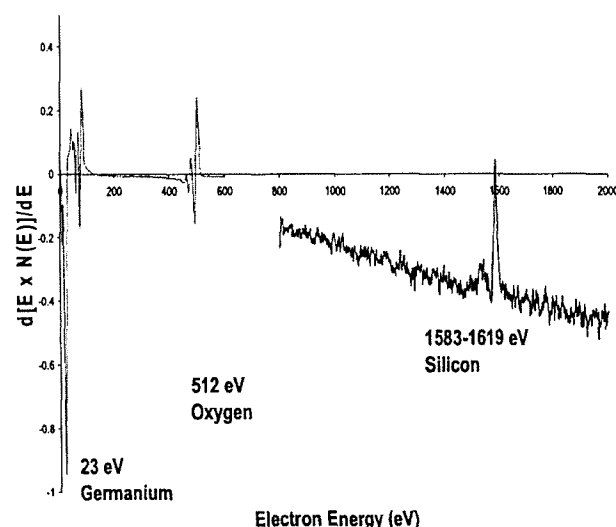


Fig. 3. Post-Anneal surface Auger results. Germanium remains present at surface, increase in oxygen signal could suggest oxidation of poly Si-Ge in spite of N_2 ambient.

The XRD phase scan for a pre-anneal sample showed a single intensity peak at approximately 70 degrees which corresponds to a (004) orientation. A similar scan on a 4200Å showed no intensity peaks through a range of angles varying from 20 to 160 degrees.

V. DISCUSSION

Alternating layers of polysilicon and germanium were deposited by a combination of LPCVD and PVD. Although limited results are available there is indication that the germanium was able to diffuse through the polysilicon film as its presence was detected by surface auger analysis. Small amounts of oxygen and carbon

were also detected and most likely represent contamination of the surface by organics and a native oxide film. XRD scans obtained at RIT do not appear to be able to resolve the thickness of films used in this study. The scan for polysilicon showed none of the characteristic peaks expected for this film but rather showed it to be a completely amorphous film. There was a clear peak present on the poly Si-Ge sample which corresponds to the (004) orientation. Previous work on these materials have shown that the orientation of polycrystalline Si-Ge when deposited solely by LPCVD is highly temperature dependent [16]. Salm showed that at temperatures approaching those used in the RIT SMFL LPCVD the (004) orientation dominates the XRD scan results. This gives some credence to the claim that poly Si-Ge was formed during this experiment. Additional analysis by SIMS and/or RBS will be required to show the exact positional concentrations of silicon and germanium within the gate stack.

Future work besides the additional material analysis outlined above includes completion of the device wafers by boron implantation, boron activation, and lithography to form capacitor structures. C-V testing of these devices could then be used to show shifts in flatband voltage and inversion capacitance which could give some gauge as to shifts in work function and gate depletion due to use of poly Si-Ge respectively. SIMS analysis of the film would allow for a measure of boron penetration through the film and into the gate oxide. Eventually a feasibility study could be performed by attempting to integrate this poly Si-Ge film into one of RIT's submicron CMOS processes.

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REFERENCES

- [1] G. J. Hu *et al.*, "Design tradeoffs between surface and buried-channel FET's" *IEEE Trans. Elec. Dev.*, Vol. ED-32, 1985, p. 584.
- [2] S. J. Hillenius *et al.*, "A symmetric submicron CMOS technology" *IEDM Tech. Dig.*, 1986, p.252.
- [3] Kovalgin *et al.*, "LPCVD of Ge_xSi_{1-x} Films Using SiH₄ and GeH₄ Source Gases" *Proceedings Semiconductor advances for future electronics meeting*, p. 311-317, 1998.
- [4] S. Wolf and R.N. Tauber, *Silicon Processing for the VLSI Era.*, 2nd ed. vol. 1, Sunset Beach, CA: Lattice Press, 2000, pp. 821-822.
- [5] T.-J. King, J.R. Pfister, J.D. Shott, J.P. McVittie, and K.C. Saraswat, "A polycrystalline-Si_{1-x}Ge_x-gate CMOS technology" *IEEE Trans. Elec. Dev.*, vol. 4, pp. 570-578, July 1993.
- [6] Y. V. Ponomarev *et al.*, "High-Performance Deep SubMicron CMOS Technologies with Polycrystalline-SiGe Gates," *IEEE Trans. Elec. Dev.*, vol.47(4), pp. 848-865. 2000.
- [7] C. Salm, *Polycrystalline Germanium-Silicon for Advanced CMOS Technologies*, Universiteit Twente, Netherlands, pp. 38-39, 1997.
- [8] M. Buchanan, "Scaling the gate dielectric: Materials, integration and reliability" *IBM J. of R&D*, vol. 42 no. 3, 1999.
- [9] T.-J. King *et al.*, "Electrical Properties of Heavily Doped Polycrystalline Silicon-Germanium Films," *IEEE Trans. Elec. Dev.*, Vol. 41, 1994, pp. 229-231.
- [10] Y. V. Ponomarev *et al.*, "Gate-Workfunction Engineering Using Poly-(Si,Ge) for High Performance 0.18 μ m CMOS Technology," *IEDM Tech Dig.* 97. pp. 829-832. 1997.
- [11] R. F. Pierret, *Semiconductor Device Fundamentals*, Addison-Wesley, 1996, pp. 477-481.
- [12] T.-J. King *et al.*, "Properties of Phosphorus-Doped Poly-SiGe Films for Microelectromechanical System Applications" *J. Electrochem. Soc.* 150, H1, 2003.
- [13] M. H. Jones and S. H. Jones, "The General Properties of Si, Ge, SiGe, SiO₂, and Si₃N₄" Virginia Semiconductor, June 2002. <http://www.virginiasemi.com/pdf/generalpropertiesSi62002.pdf>
- [14] W.-C. Lee *et al.*, "Optimized Poly-Si_{1-x}Ge_x-Gate Technology for Dual Gate CMOS Application," *Proc. Symp. VLSI Technology*, pp. 190-191. 1998.
- [15] J. L. Medina, "Polysilicon-Germanium Films Fabricated by Ge Sputtering," RIT Microelectronic Engineering Conference. pp. 39-41. May 2001.
- [16] C. Salm, *Polycrystalline Germanium-Silicon for Advanced CMOS Technologies*, Universiteit Twente, Netherlands, pp. 21-27, 1997.

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