Study of Nickel Silicide Processes for Advanced CMOS Applications

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***Abstract*—A study has been performed to determine critical mechanisms involved in formation of nickel silicides. The process parameters under investigation were silicidation temperature, presilicide N_2^+ implant, and the presence of a titanium capping layer. Contact sheet resistance phosphorous-implanted silicon was measured and determined to degrade with high silicidation temperature. Titanium capping was found to improve contact resistance and compensate for the effects of high temperature treatment for polycides. The nitrogen incorporation via implant shows a degradation in resistivity for both silicides and polycides.**

***Index Terms*—Ni silicidation, nitrogen implant, RTP**

I. Introduction

SILICIDES have been used for many years in the microelectronic industry to circumvent the high resistivity seen when contacting metal to poly gates and source/drain regions of conventional MOSFET structures. The silicide process involves incorporation of metal into silicon being contacted to reduce the resistivity of the contact. Different metals are chosen to create silicides based on their properties such as processing temperature, dry etch capabilities, wet etch chemicals necessary, resistivity, dominant diffuser species, etc.

The use of silicides on polysilicon gates (resulting in "polycides") and S/D contacts (self-aligned silicides – "salicides") has shown to be necessary in small (sub-micrometer) devices that eventually become limited in their performance by the resistance seen at the source/drain and the delay seen at the gate. Other very important potential uses of silicides have presented themselves when considering dual-gate devices, when contact between n+ and p+ polysilicon gates is necessary. Silicides are essentially an enabling technology in this case, as their use prevents the formation of weak diodes between the NMOS and PMOS transistors. In general, today's CMOS processes have many uses for silicides, and are predicted by the International Technology Roadmap for Semiconductors (ITRS) [1] to be very important and relevant for several years into the future.

The choice of metals for silicide formation is becoming crucial, as certain metals have started to approach physical limits associated with their properties. There are three metals that are most frequently used in modern silicide formation: titanium, cobalt, and nickel.

Titanium silicide ($TiSi_2$) has been a long-time dominant silicide technology, but has reached extinction in modern deep sub-micrometer CMOS applications. Although it offers low resistivity when properly formed, $TiSi_2$ exhibits several critical failures. One such failure is the silicon-diffusion dominated formation of silicides that can lead to problems of bridging. Secondly, $TiSi_2$ exhibits a strong narrow-line effect due to incomplete transition from a high-resistivity C49 phase to the low-resistivity C50 phase. The narrow-line effect has necessitated the elimination of $TiSi_2$ from sub-0.25μm CMOS technology. Cobalt silicide ($CoSi_2$) has replaced $TiSi_2$ as the pre-eminent contact technology in most advanced CMOS applications. Cobalt silicide offers many advantages over TiSi2, most importantly avoiding narrow-line effects and bridging problems. However, CoSi2 is also highly sensitive to ambient contamination during silicidation, and exhibits a high consumption rate of silicon.

To remedy deficiencies of CoSi2, nickel silicide (NiSi) has emerged as a candidate for most advanced silicide applications. Nickel silicide offers a lower consumption rate of silicon, no narrow-line effects, and generally low resistivity (often reported in ~15-18 $\mu\Omega cm^2$ range) [2]. However, the detriments of NiSi include high sensitivity to ambient contamination and poor thermal stability [3]. These problems must be investigated in order to advance the science

This study investigates the properties and mechanisms of NiSi formation. Silicidation is performed on doped crystalline silicon and doped polysilicon to simulate the effects of silicidation on source/drain (S/D) and gate CMOS regions, respectively. Silicide formed on crystalline silicon is used to determine the specific contact resistivity (ρ_c) using the transfer length method (TLM). Polycide is formed on a blanket polysilicon

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film, and its sheet resistance is measured using 4-point probe methods. Experiment parameters are a presilicide N2+ implant (expected to improve silicide thermal stability), anneal temperature (expected to affect resistivity), and presence of a capping layer during silicide formation (expected to decrease the sensitivity to ambient contamination).

II. THEORY

A. Nickel

Properties of nickel are shown in Table I:

TABLE I
GENERAL NICKEL PROPERTIES

Property	Value
Atomic number	28
Atomic weight	58.6934 amu
Density of bulk solid	8.908 g cm^{-3}
Melting point	1455 °C
Boiling point	2913 °C
Thermal conductivity @ 25 °C	91 W m^{-1} K^{-1}
Electrical resistivity @ 25 °C	7 μΩ cm
Pauling electronegativity	1.88 Pauling units

B. Nickel Silicide (NiSi) Formation

Silicides in general are formed by placing metals (such as tungsten, tantalum, titanium, cobalt, nickel) in direct contact with silicon, followed by a high-temperature heat treatment. Often performed as rapid thermal processing (RTP), the heat treatment creates a metal/semiconductor compound of varying physical properties.

The properties of a silicide film are heavily dependent on processing conditions. As such, there are several important aspects to formation of nickel silicides:

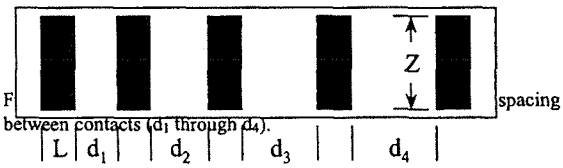
1) Temperature of Silicidation: Nickel monosilicide (NiSi) has been identified [4] to form at temperatures as low as ~400 °C. This relatively low temperature of formation is beneficial in decreasing the thermal budget of a CMOS process. However, the distinction of nickel silicide *phase* being formed is crucial – at approximately 750 °C and above, a higher-resistivity (~50 μΩcm^2) nickel disilicide ($NiSi_2$) phase forms. The precursor to formation of $NiSi_2$ is silicon agglomeration in the NiSi film, occurring at temperatures of ~700 °C. Both silicon agglomeration and formation of disilicide result in increased resistivity and degraded device performance. Because of this problem, thermal stability of nickel monosilicide is regarded as a primary roadblock in adaptation of NiSi to modern CMOS devices.

2) Surface and Ambient Contamination: Silicide formation is slowed down or even blocked by any silicon oxides (SiO_2) located at the metal/silicon interface. These interface oxides are often films native to the substrate, or are formed by chemical means (during cleans, for example). During silicidation, the diffusing metal ions may penetrate the interfacial oxide and begin silicide formation below the oxide layer. However, presence of ambient contaminants (most notably oxygen and steam) during silicidation encourages growth of SiO_2 on top of the silicide, eventually blocking the silicide process and leading to formation of metal oxides. To combat this process, capping layers such as titanium (Ti) or titanium nitride (TiN) are employed. These capping layers are deposited immediately following the metal used in silicidation (Ni) and are removed following the silicide formation. The cap acts to either react with oxygen in the ambient (as Ti) or to passively block oxygen diffusion (as TiN). Capping layers are commonly used in $CoSi_2$ formation, and do not greatly complicate processing.

3) Self-aligned Silicidation: As is the case with other metals, nickel will only react with silicon, leaving materials such as SiO_2 or silicon nitride (Si_3N_4) intact. This allows formation of *nickel salicides* – self-aligned silicides, formed only in the regions where nickel and silicon (single-crystal or polycrystalline) are in direct contact. Nickel, along with any capping layers, can be removed from regions where silicide is not formed (such as transistor isolation) by an etch in H_2SO_4:H_2O_2 1:2 mixture (also known as Piranha etch). The Piranha etch does not remove any silicides formed, and properties of the silicide remain unchanged.

C. Resistivity Measurements

The relative success of silicidation can be determined by measuring the sheet resistance (R_S) of polycided gates and the specific contact resistivity of contact regions. The measurements techniques used in this study are the transfer length method (TLM) for contact resistivity and four-point probe method for sheet resistance.



1) Transfer Length Method: Originally proposed by Shockley [5], a TLM test structure (Fig. 1) consists of several contacts of unequal spacing.

By applying a voltage bias across the contact pads and the resulting current, the total resistance is used to determine contact resistance (R_C), as shown in Fig. 2:

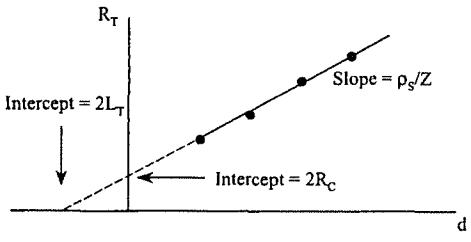


Fig. 2. The TLM method of contact resistance extraction

Using the slope of the best-fit line [6] and the contact pad dimensions, the contact specific sheet resistance ρ_S can be determined. The same plot can be used to indirectly determine the specific contact resistivity, ρ_C, by multiplying the contact area with contact resistance R_C. The TLM method exhibits acceptable accuracy for purposes of this study.

2) The Four-point Probe: Sheet resistance of shallow diffused or metallized layers can be determined by four-point probe measurements. A basic probe system is shown in Fig. 3.

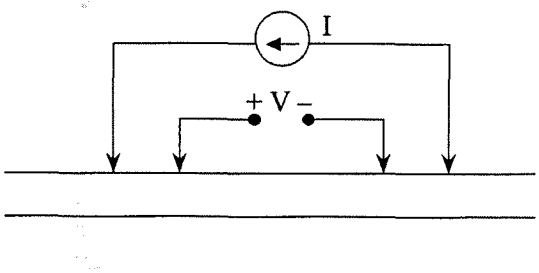


Fig. 3. A standard four-point probe setup.

The four closely-spaced probes act to inject a fixed current between the two outer probes and measure the resulting voltage between the two inner probes. Automated resistivity mappers such as the one by Creative Design Engineering (CDE) used in this study, employ four-point probes to determine sheet resistance of full-wafer samples.

III. Experiment

The experiment required parallel processing of crystalline (source/drain approximation) and polysilicon (gate approximation) samples.

A. RTP System Calibration

Since rapid thermal processing is necessary for best silicide formation, a short experiment was performed to test the accuracy of the AG 410 RTP system being used. The experiment used the established eutectic temperature of aluminum (577 °C) [7] to test the system temperature monitors. Aluminum (1% silicon) was evaporated to a thickness of 4434 Å onto a silicon substrate using a shadow mask. The silicon wafer was then cleaved into six pieces that were individually RTP-annealed in an N_2 ambient at different temperatures.

To ensure that the theoretical eutectic temperature is included in the experiment, the samples were processed at 502 °C, 527 °C, 552 °C, 577 °C, 602 °C, and 627 °C for 60 seconds. At lower temperatures, there is no indication of eutectic transition. The first signs of eutectic transition can be observed on the 577 °C sample (see Fig. 4), with the transition becoming obvious at higher temperatures. Thus, the system accuracy is deemed adequate for the purposes of this study.

B. Crystalline Silicon Silicidation

Experiment was performed on n-type (5-15 Ωcm) 100mm diameter wafers of <100> crystal orientation. Following an RCA clean, the wafers were blanket-implanted with 4×10^{15} cm^{-2} phosphorous (P_{31}) at 90 keV. This implant simulates the source/drain NMOS implant for standard RIT Sub-μm CMOS

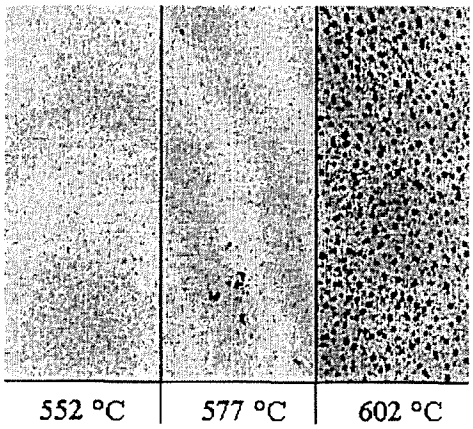


Fig. 4. Eutectic transition of aluminum. As predicted by published values, the first signs of eutectic transition can be observed on the sample that saw a 577 °C treatment. The observations also confirm that the incorporation of 1% silicon does not significantly shift the eutectic temperature

process. The implant is followed by a thermal furnace anneal at 1000 °C for 20 minutes in N_2 and 10 minutes in steam ambient. The oxide grown is removed by a BOE etch.

A low-temperature oxide (LTO) is deposited by Low Pressure Chemical Vapour Deposition (LPCVD) in order to form TLM structures. Following the deposition, LTO was densified with a furnace anneal (30-minute N_2 soak at 900 °C) to better approximate thermal oxide properties. Following the densification, the LTO was found to have an average thickness of 4443.2 Å with close to 16% thickness deviation across the wafer.

First-level lithography was performed on a g-line stepper to define etch holes for TLM structure openings. The LTO etch was performed using a plasma etch (SF_6/CHF_3 mixture). To ensure complete oxide removal in openings, and to account for oxide nonuniformity, the

dry etch was followed by a 45-second BOE etch. One half (flat-side) of each wafer is then covered by photoresist (approximately 1 μm thick) using broadband lithography and development. The resist serves to protect one half of the wafer from the upcoming nitrogen implant, essentially creating the first lot split (implant vs. no implant). The nitrogen (N_2^+) implant dose was 6×10^{14} cm^{-2}, performed at 15 keV after Lee et. al [8]. The resist was stripped and the wafers annealed at 950 °C for 60 seconds.

Prior to silicide metal deposition, wafers had an additional oxide etch (30 seconds in 50:1 deionized H_2O:HF, dried in N_2) performed to remove any native oxides that may block silicidation. Nickel was sputtered in an argon ambient to a resulting thickness of approximately 400 Å (wafers BXC3871#1 and BXC3871#3). As part of the second lot split (wafers BXC3871#4 and BXC3871#5), an identical nickel deposition was followed by a titanium layer deposition (~500 Å thick) without breaking vacuum. Note that wafer BXC3871#4 was slightly out of specification and too large in diameter for the sputterer holders. The wafer broke while being removed from the sputterer, and could not be tested. Silicidation was possible, but any further processing could not be performed.

The silicidation was performed for 60 seconds in N_2 ambient at different RTP temperatures (third and final lot split). Wafers BXC3871#3 and BXC3871#4 were treated at 600 °C, while wafers BXC3871#1 and BXC3871#5 saw 750 °C. All wafers were individually placed in a Piranha etch (H_2SO_4:H_2O_2 1:2 @ ~80 °C) for approximately 2 minutes to remove any unreacted nickel and/or titanium.

To create good contacts to the nickel silicide layers, aluminum (1% silicon) was sputter deposited on all wafers (except BXC3871#4) to an approximate thickness of 1 μm. The aluminum was patterned using g-line lithography and Jay Cabacungan's image reversal process. The aluminum contacts were etched for 2 minutes in wet aluminum etchant. At this point, all samples were ready for testing.

C. Polysilicon Silicidation

Experiment was performed on n-type (5-15 Ωcm) 100mm diameter wafers of <100> crystal orientation. Following an RCA clean, a dry oxide growth (487.6 Å average thickness) was performed. Polysilicon was deposited by LPCVD to an average thickness of 3409 Å. In order to fully simulate the gate structure of RIT's Sub-μm CMOS, the polysilicon was doped with a spin-on phosphorus source, pre-baked at 200 °C for 15 minutes and dopant was driven-in over 15 minutes at 1000 °C in N_2 ambient. Following the drive-in, the remaining spin-on glass was etched in BOE for 4 minutes. The flat-side half of each wafer was covered by a 1 μm thick photoresist film, protecting against a N_2^+ implant (6×10^{14} cm^{-2} @ 15 keV). Following the implant, resist was stripped, and wafers annealed (950 °C for 60 seconds in N_2). The wafers were etched in 50:1 deionized H_2O:HF in order to remove any native or chemical oxides. Nickel was sputtered in Ar to a thickness of approximately 400 Å (wafers BXC3871#6 and BXC3871#7). In the second polysilicon lot split (wafers BXC3871#8 and BXC3871#9), the nickel deposition was followed by a titanium layer deposition (~500 Å thick) without breaking vacuum.

TABLE II
CRYSTALLINE (S/D) CONTACT REGIONS

Capping layer	RTP Temperature [°C]	N_2^+ implant	ρ_C [Ωcm^2]
Titanium	600	yes	n/a
Titanium	600	no	n/a
Titanium	750	yes	5.1×10^{-4}
Titanium	750	no	2.1×10^{-4}
none	600	yes	9.5×10^{-4}
none	600	no	5.5×10^{-4}
none	750	yes	1.2×10^{-3}
none	750	no	1.1×10^{-3}

Similar to the crystalline Si part of the experiment, the lot was split once again to create silicide over 60 seconds in N_2 ambient at 600 °C (wafers BXC3871#6 and BXC3871#8) or 750 °C (wafers BXC3871#7 and BXC3871#9). Note that wafer BXC3871#6 was actually processed in two 30-second intervals due to accidental use of an old RTP system recipe. Following a 2-minute Piranha etch (at ~80 °C) of unreacted metals, the wafers were ready for testing.

IV. Results and Discussion

A. Crystalline Silicon Silicides

Using the previously outlined TLM approach, specific contact resistivity is determined for each sample. Results are summarized in Table II. Standard RIT Sub-μm process specific contact resistivity is in the 2×10^{-6} Ωcm^2 range. As such, the silicidation actually increased contact resistivity in all cases. The analysis of results has several aspects:

1) Effect of Titanium Capping: A clear trend shows that the use of titanium capping layers improves specific contact resistivity. Unfortunately, not all data could be collected due to broken wafer BXC3871#4. However, the measurements that could be made clearly indicate an order-of-magnitude improvement in specific contact resistivity when using the titanium capping layer. This result was expected, as research has shown [9] that capping layers in general have a beneficial impact on silicide formation.

2) Effect of RTP Temperature: As discussed earlier, high silicidation temperature (750 °C) is expected to have a detrimental effect on contact resistivity. Table II

shows that for *comparable* cases (wafers with no capping layers), the higher temperature anneal shows a clear increase in ρ_C.

3) Effect of N_2^+ Implant: The nitrogen implant has an effect opposite that observed in literature for nickel [8] and other silicides [10], [11]. The resistivity degradation in nitrogen-implanted regions is most likely due to an incomplete anneal of crystalline damage caused by N_2^+ ions. The nitrogen introduced was expected to improve thermal stability by reducing interfacial energies at the Si/Ni interface. However, any high-dose implant, if not properly annealed, has the potential of creating *more* surface energy states, along with increased surface roughness. Although the anneal conditions were identical to that suggested by literature, further annealing may have been necessary to gain any advantage from the nitrogen implant.

A sample from wafer BXC3871#5 was analyzed using a Scanning Electron Microscope (SEM) and the integrated Energy Dispersive X-Ray Spectroscopy (EDX) system. The analysis was performed on a cross-section of the silicide film (Fig. 5). The EDX analysis of the cross-section sample shows clear incorporation of ambient oxygen into the silicide film (Fig. 6). Additionally, the strength of the silicon peak suggests that nickel disilicide (NiSi2) has also been formed. Since BXC3871#5 was processed at 750 °C, the formation of disilicide is expected. The combined effects of oxygen incorporation (likely leading to formation of nickel oxides) and NiSi2 formation result in high specific resistivity.

Additional analysis was performed on the "isolation" region of the TLM structure. The SiO_2 regions are not expected to form silicides. However, applying a bias across isolation regions resulted in a small but observable current.

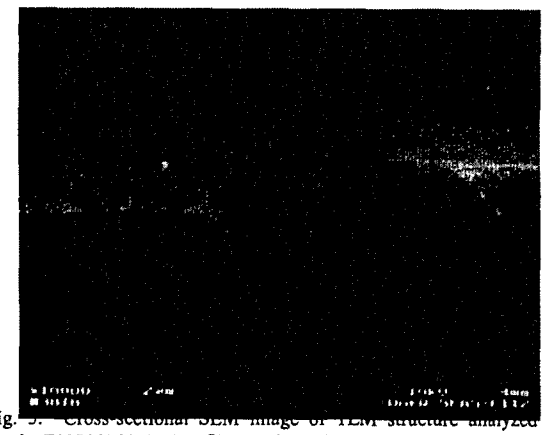


Fig. 5. Cross-sectional SEM image of TLM structure analyzed (wafer BXC3871#5). Top film on the right is aluminum. The mesa structure on the left is silicon dioxide isolation. EDX analysis is performed on exposed nickel silicide in the middle..

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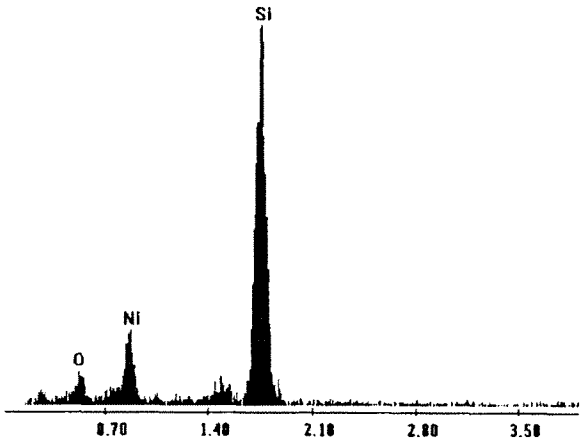


Fig. 6. Cross-sectional EDX analysis of nickel silicide region of sample obtained from wafer BXC3871#5.

The thin conducting layer was theorized to be nickel and/or titanium that did not react with SiO_2, but was not completely removed by the Piranha etch. The sample was thus also analyzed using SEM/EDX techniques (Figures 7 and 8) to investigate the conducting film in isolation regions. EDX analysis clearly shows that, in addition to strong silicon and oxygen signals, nickel is present. Similar top-down EDX analysis performed on the bare nickel silicide area (not shown) showed a faint titanium signal, indicating that some of the capping layer remained after the Piranha etch. The presence of nickel explains conductivity of the isolation region and along with the Ti signal indicates that a longer and/or higher-temperature Piranha etch may be necessary for best results.

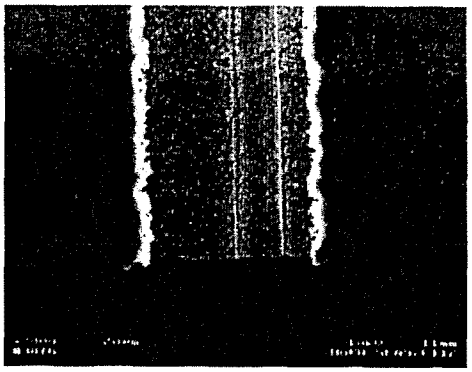
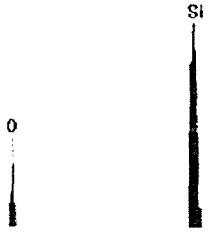


Fig. 7. Top-down SEM view of structure analyzed (wafer BXC3871#5). The five distinct regions are, left to right: aluminum contact, nickel silicide, silicon dioxide, nickel silicide, and aluminum contact.



B. Polysilicon Silicides

The sheet resistance of polycide wafers was measured on a CDE ResMap tool, and results are presented in Table III. Standard RIT Sub-μm CMOS gate R_S values are in the ~30-40 Ω/sq. range. As can be seen from results obtained, the formation of nickel silicide results in a large improvement in poly sheet resistance. Once again, there are trends that should be noted:

1) Effect of Titanium Capping: Unlike the case with crystalline silicon, Ti capping does not appear to have a significant effect on silicide performance. A surprising result, this phenomenon should be investigated further to ensure that titanium capping indeed has no effect on polycide formation.

2) Effect of RTP Temperature: Consistent with earlier observations, although not as obvious, a comparison of appropriate samples shows that higher silicidation temperatures generally result in higher sheet resistance. The agglomeration of silicon and formation of $NiSi_2$ appears to affect polycides as well as silicides based on single-crystal silicon.

3) Effect of N_2^+ Implant: As observed earlier, the nitrogen implant has a generally detrimental effect on silicide performance. Once again, the high level of implant damage likely led to a poor silicide film. An improved N_2^+ implant anneal may result in improved thermal stability of the silicides.

TABLE III
POLYSILICON (GATE) SHEET RESISTANCE

Capping layer	RTP Temperature [°C]	N_2^+ implant	R_S [Ω/sq.]
Titanium	600	yes	4.9
Titanium	600	no	4.3
Titanium	750	yes	5.0
Titanium	750	no	4.1
none	600	yes	3.0
none	600	no	3.0
none	750	yes	6.5
none	750	no	6.2

V. Conclusion

This study identified critical mechanisms involved in formation of nickel silicide. Thermal instability of nickel monosilicide and its transition to nickel disilicide was demonstrated. EDX analysis of TLM structures and surrounding films has further confirmed formation of $NiSi_2$ and the susceptibility of nickel silicide processes to ambient contamination. Titanium capping has shown to be either an improvement (in case of crystalline Si silicide formation) or have no effect (in case of polycide formation). Finally, the N_2^+ implant had a detrimental impact, attributed to a high level of crystal lattice damage that was not fully annealed. Future work should include a detailed study of the nitrogen implant, improved annealing ambient conditions, and a study of high-temperature Piranha etching.

Acknowledgments

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