Optically Injected Circuits in a 0.18 μm CMOS

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Abstract—**Power consumption and power conversion efficiency have been two key parameters characterizing the performance of electronic circuits since their dawn. With the increasing demand of miniaturization, mobility and portability of electronic industrial and consumer equipment, low-power and high-efficiency circuits are in high demand.**
Possible energy sources to enable mobility and/or portability are chemical (e.g. batteries, accumulators, micro gas, engine, fuel cells), mechanical (e.g. elastic energy in springs, vibrations, oscillations, ultrasound), thermal (e.g. body heat), EM-Field (e.g. inductive coupling, capacitive coupling, RF) and optical (photovoltaic cells).
They are a great number of applications for which low-power operation can be replaced with remote-powered operation. For optically remote powered operation, we propose the use of optically injected circuits. This has the following advantages: no need for off-chip photovoltaic cells, i.e., reduced package complexity, no need for DC-to-DC converters, i.e., improved conversion efficiency, no need for a power distribution grid, i.e., no Joules losses, and reduced interconnection complexity.
This paper studies the concept of optically injected logic circuits and proposes their implementation in deep-submicron and beyond CMOS technologies. This paper includes all the calculations and all the processes to fabricate the digital logic circuits. These logic circuits can be used in embedded micro-controllers where very low power operation can be replaced by remote powered operation. No local power source of any kind is necessary. Specific areas of application are data acquisition and control systems in bio-medical implants, space applications, wireless fabrication facilities and wafer-scale robots.

Index Terms— **CMOS, logic, low power, Optical injection, remote power.**

I. NTRODUCTION

POWER consumption and power conversion efficiency have been two key parameters characterizing the performance of electronic circuits since their dawn. With the increasing demand of miniaturization, mobility and portability of electronic industrial and consumer equipment, low-power and high-efficiency circuits are in high demand. Possible energy sources to enable mobility and/or portability are chemical (e.g. batteries, accumulators, micro gas, engine, fuel cells), mechanical (e.g. elastic energy in springs, vibrations, oscillations, ultrasound), thermal (e.g. body heat), EM-Field (e.g. inductive coupling, capacitive coupling, RF) and optical (photovoltaic cells).Each of these power sources has advantages and disadvantages, depending on the application's specific environment in which they are embedded.

They are a great number of applications for which low-power operation can be replaced with remote-powered operation. Remote-powered operation requires an external device, commonly called an interrogator, to provide the power. EM-Field, ultrasound and optical energy are generally employed. We will further call the interrogated equipment/device the target. At the target, the incoming energy is converted to electrical energy using a transducer, sensor or detector. Then a DC-to-DC converter is used to generate the necessary supply voltages.

For optically remote powered operation, we propose the use of optically injected circuits in the target (Fig. 1.). This has the following advantages: no need for off-chip photovoltaic cells, i.e., reduced package complexity, no need for DC-to-DC converters, i.e., improved conversion efficiency, no need for a power distribution grid, i.e., no Joules losses, and reduced interconnection complexity.

Manuscript received on May 20, 2003. Gregory Ardault is an exchange student at RIT from National Institute of Applied Science (INSA), Rennes, France

II. OPTICALLY INJECTED LOGIC CIRCUITS

Injection logic circuits use basically a current source to inject charge into the gate's output node. Based on this concept, an injected inverter would have the general schematic diagram described in Fig.2. The current source injects current into the node circuit continuously. In a current-mode logic the switch is current controlled. This can be accomplished using a NPN BJT for the switch. In a voltage-mode logic the switch is voltage controlled. This can be accomplished using an NMOS for the switch.

In the current-mode logic let's assume the switch is off when it sources current and on when it sinks current. When the switch is off the current source is sourcing

current into the output node. The switch in the input of the next gate is sinking this current and turns on. Thus a logic value inversion occurs.
In the voltage-mode logic let us assume the switch is off when the voltage at its input is low and on when it is high. If the switch is off then, as before, the current source is sourcing current into the output node. During the switching phase this current charges the input (gate) capacitor of the next switch. During the holding phase (no switching) it holds the charge on this capacitor by compensating for leakage currents. Note that in a real voltage controlled switch this capacitor always exists. Further, the switch in the input of the next gate is turned on, and overall a logic value inversion occurs.
References [2] and [3] have simultaneously proposed injection using a forward biased diode or BJT connected in a diode configuration. Both circuit realizations are in BJT technologies. These implementations have been extensively developed and used in the past under the generic name of I^2L (Integrated Injection Logic) circuits.
Reference [2] further proposed optical injection and showed the successful implementation of a digital block using such circuits. Optical injection is achieved by building the current source in silicon using a large area diode junction as a photovoltaic cell. Injection logic has been applied in CMOS circuits in [4]. The injection current source was there a diode connected PMOS.
In our work we have developed optically injected logic circuits in a 0.18 μm CMOS technology. In the next paragraphs we describe gate topologies, component sizing criteria and performance limits.

III. OPTICALLY INJECTED LOGIC CIRCUITS IN CMOS

A. Gate topologies.

The basic building blocks of an optically injected logic gate is shown in Fig.3. It is derived from the generic topology presented in Fig.2. The injection current source (ICS) is realized using a p+/n- well diode as a photovoltaic cell. Also shown are the input node capacitance and the output node capacitance. Both are the sum of intrinsic transistor, diode and interconnects parasitic capacitances.
Based on this building block, the topology and operation of the inverter and the two-input nor gates (Fig.4.) are straightforward. All other gates are then built from these two gates.

B. Component Sizing.

In the basic building block (Fig.3.), the transistor W/L ratio is chosen to be the minimum size the target CMOS technology can offer. In our case $W / L = 0.27\mu m / 0.18\mu m$. The reason for this size is to minimize the parasitic capacitances that add to the input and output node. These are directly proportional to the drain and source layout areas and perimeters.
With the NMOS turned off, the diode working as a photovoltaic cell can create at the output node no more than about 0.5V. This is because beyond this forward biasing point the forward current exceeds the reverse photo generated current. The threshold voltage of the transistor is also about 0.5 V. Still, as we will be seen later, the drain to source courant I_D' is sufficient to consider the transistor on for our purposes. Observe that future, smaller-size technologies target lower threshold voltages and because the 0.5 V limit of the current generating diode will not change, the circuits will scale down with increased performance.
As already mentioned, the diode is built within an n-well island as a p+/n-well diode. Assuming a constant incident optical power, the photo-generated current is proportional to its area. A large photo-generated current has a positive impact on driving the output node from low to high. On the other hand, increasing its area has two drawbacks. First, a too large area can create an unacceptable large parasitic capacitance added to the output node with negative impact on the gate's switching characteristics. Second, a large area means an increased cost per gate. This can decrease the value of these circuits when compared to others.

1. Determination of the gate oxide:

For high performance (and consequently high power) CMOS, we may take 1.2MV/cm as the upper limit of the gate oxide field:

$$t_{ox\min} = \frac{V_{ss}}{E_{\max}} = \frac{1.5}{1.2\times10^{6}} = 25.0\times10^{-8} cm = 100\mathring{A}$$

$$C_{ox}' = \frac{\varepsilon_{ox}}{t_{ox\min}} = \frac{3.45\times10^{-13}}{100\times10^{-8}} = 2.76\times10^{-7} F.cm^{-1}$$

2. Determination of the p-type doping in the substrate:

Educated guess of the long channel threshold voltage:

The long channel threshold voltage V_{TLC} needs to be:

$$\frac{Vss}{5} \le V_{TLC} \le \frac{Vss}{4}$$

With: $Vss = 1.5V$
So $0.3V \le V_{TLC} \le 0.375V$

$$V_{TLC} = V_{FB} + \phi_0 + \gamma\sqrt{\phi_0}$$

Where - V_{FB} is the Flatband voltage.
- ϕ_0 is the surface potential of mos in strong inversion.
- γ is the body effect.

$$V_{FB} \approx \phi_{MS} = \phi_{bulk} - \phi_{gate}$$
$$V_{FB} \approx \phi_{MS} = -\phi_{F_{Si}} + \phi_{F_{Poly}}$$

Where: - ϕ_{MS} is the contact potential of body material to gate material.

The Polysilicon gate is doped N+ so:
$\phi_{F_{Poly}}$=-0.56V

$$V_{FB} \approx \phi_{MS} = -\phi_t \times \ln\left(\frac{N_A}{n_i}\right) - 0.56V$$

Where: - N_A is the acceptor concentration in the P-well;

- ϕ_t is the thermal voltage (0.0259V at 300K);

And - n_i is the intrinsic carrier concentration ($1\times10^{10}.cm^{-3}$ at 300 K).

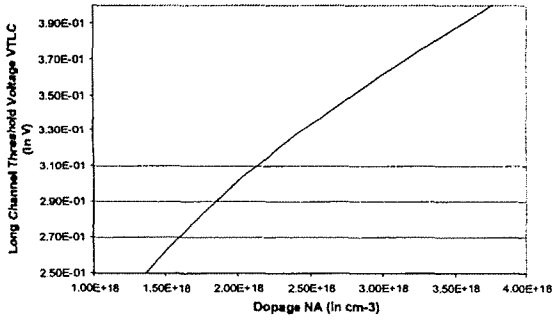
$$\phi_0 = 2\times\phi_{F_{Si}} + n\times\phi_t$$
$$\phi_0 = 2\times\phi_t\times\ln\left(\frac{N_A}{n_i}\right) + n.\phi_t$$
$$\gamma = \frac{\sqrt{2.q.\varepsilon_S.N_A}}{C_{ox}'}$$

So

$$V_{TLC} = \phi_t\times\ln\left(\frac{n_i}{N_A}\right) + 0.56V + 2\times\phi_t\times\ln\left(\frac{N_A}{n_i}\right) + n.\phi_t + \frac{\sqrt{2q\varepsilon_S.N_A}}{C_{ox}'}\times\sqrt{2\times\phi_t\times\ln\left(\frac{N_A}{n_i}\right) + n.\phi_t}$$

$$\Psi_{SA} = \left(-\frac{\gamma}{2} + \sqrt{\frac{\gamma^2}{4} + V_{GB}}\right)^2$$

Long channel Threshold voltage vs.p-well dopage



We need $0.3V \le V_{TLC} \le 0.375V$, so we need a doping of$3\times10^{18}.cm^{-3}$.

$V_{TLC} = 0.369V$
$\phi_0 = 1.17V$
$\phi_{F_{Si}} = 0.506V$
$\Psi_{SA} = 0.356V$
$\gamma = 0.241V^{1/2}$
And $\phi_{MS} = -1.07V$

3. Determination of the junction depth:

On the one hand we want a junction depth X_j which has to be as small as possible to achieve high performance device (minimize leakage current). But on the other hand a shallow junction involves cutting edge process. Consequently it will dramatically raise the cost associated with the NMOS. Here there is a trade off.
The cost is given by:

$$F = A\times e^{\frac{300-X_j}{B}}$$
(X_j in Å, A=100 and B=300)

Where $F=0$ represents the smallest cost and $F=100$ the highest cost. We can not choose X_j<300Å. We decided that $F\approx50$ is an acceptable value. With $X_j = 500\text{Å}$ we have $F=51.3$.

Determination of the short channel saturated threshold voltage $V_{TLC_{MIN}}$:

$$V_{TLC_{MIN}} = 4\times S$$

Where S is the subthreshold swing.
$S = 2.3\times n\times\phi_t$
Where

$$n = 1 + \frac{\gamma}{\sqrt{\psi_{SA}}}$$

So:

- $n = 1.405$
- $S = 0.08367V = 83.67mV$
- $V_{TLC_{MIN}} = 0.335V$

4. Determination of the effective threshold voltage $\hat{V}$:

$$\hat{V} = V_{TLC} + \Delta V_{TLC}$$

Where:

$$\Delta V_{TLC} = V_{TLC} - V_{TLC_{MIN}}$$

$\Delta V_{TLC} = 0.0273V = 27.33mV$
So $\hat{V} = V_{TLC} + \Delta V_{TLC} = 0.369 + 0.0273 = 0.396V$

5. Determination of the target value for the scaling parameter l:

$$l = 0.1\times(t_{OX}.X_j.\chi_d{}^2)^{\frac{1}{2}}$$

Where

$$\chi_d = \sqrt{\frac{2\times\varepsilon_s\times2\times\phi_{F_{Si}}}{q.N_A}}$$

$\chi_d = 2.1\times10-6.cm^{-1}$
So $l = 2.34\times10^{-13}$

6. Determination of the full drive current:

$$I_D' = W \times \frac{C_{OX} \times V_l \times [V_{GS} - V_T]^2}{[(V_{GS} - V_T) + L \times E_{SAT}]}$$

With:

$$E_{SAT} = \frac{2 \times V_l}{\mu_n}$$

$$\mu_n = \frac{\mu_0}{1 + \theta \times (V_{GS} - V_{TLC})}$$

$$\theta = \frac{2 \times 10^{-7}}{t_{OX}}$$

$V_l = 1 \times 10^7 V$

$\mu_0 = 600 cm^2 .s^{-1}$

$V_{GS} = V_{SS} = 1.5V$

So:

- $\theta = 0.8$
- $\mu_n = 314.99 cm^2 .s^{-1}$
- $E_{SAT} = 63493 V.cm^{-1} = 63.493 kV.cm^{-1}$
- $I_D' = 9.15 \times 10^{-5} A = 0.0915 mA$

The longitudinal field under full drive is very small compared to the maximum allowed longitudinal field (taken to be 650 kV/cm).

7. Determination of the full drive current for the ultimate NMOS (L→0):

$$I_D' = W \times C_{OX} \times V_l \times [V_{GS} - V_T]$$

$I_D' = 2.485 \times 10 - 4A = 0.2485 mA$

8. Determination of the Early Voltage V_A:

$$V_A = B_2 \times L \times \sqrt{N_A}$$

With

$B_2 = 2 \times 10^{-3}$

$V_A = 93.53V$

9. Determination of the maximum die operating frequency: die performance.

$$\text{Die operating frequency} = \frac{1}{3 \times T_f}$$

With

$$T_f = 12 \times Fall - time$$

$$Fall - time \approx \frac{Q}{I_D'} = \frac{C.Vss}{I_D'} = \frac{(2 \times C_{OX} + C_{PAR}) \times Vss}{I_D'}$$

With

$$C_{OX} = C_{OX} \times L \times W$$

We suppose $C_{PAR} = 3.5 fF$

So

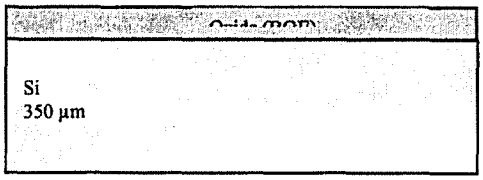
- $C_{OX} = 6.71 \times 10^{-16} F = 0.671 fF$
- $Fall - time \approx 7.94 \times 10^{-11} s = 79.94 ps$
- $T_f = 9.52 \times 10^{-10} s = 0.952 ns$
- Die operating frequency $= 3.5 \times 108 Hz = 0.35 GHZ$

IV. PROCESSES OF FABRICATION

The starting material for deep submicron NMOS is 6" n-type (5-10 Ohm.cm) wafers.

1st step: Alignment oxide.

We grow a 500 Å silicon dioxide, in wet O_2, using bruce furnace 04 (Recipe # 250).



2nd step: 1st Level photolithography: P well

We use the automatic coat SVG Track with Shipley 812 resist.

Process:

- Dehydrate bake (200°C during 120sec);
- Coat HMDS (3000rpm during 30 sec) and then Shipley 812 resist (4500 rpm during 60 sec);
- Soft bake at 90°C during 60 sec.
-

We expose the wafer using Canon stepper (g-line: 365 nm).The resist needs an exposure dose (E) of about $75 mJ/cm^2$ .The intensity is measured and found to be $15 mW/cm^2$. So using the equation:

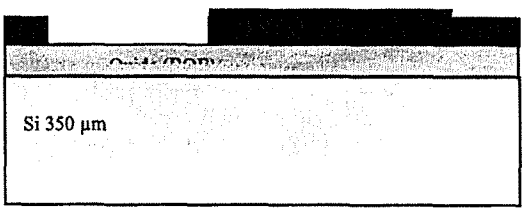
$E = I.t$

We find an exposure time of 5 seconds.

We develop the wafers on the SVG Track with Shipley CD-26 developer.

Process:

- Post exposure bake (115°C during 60 sec);
- Develop using Shipley CD-26 developer during 50 sec (puddle rinse, spin dry);
- Hard bake at 125°C during 60sec.

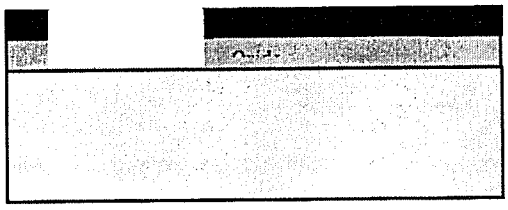


3rd step: oxide etch.

We open a window for the implantation.
We use (B.O.E) to etch the alignment oxide.
Termal SiO2 BOE: Si (7:1) 1,000 Å/min *

* RIT data, Dr. Fuller, et.al.

So we need a etch time of 30 seconds to remove the oxide.



We finish by a Photoresist Ash and RCA clean.

4th step: P-well implant.

The well-formation process is begun by growing a layer of scarified oxide on the wafer. A high-energy B implant is then carried out (450-500 keV, dose 1E13 /cm²).

$$N(x) = N_{Rp} \times \exp\left[\frac{-(x-Rp)^2}{2\times\Delta Rp^2}\right]$$

Where:

- Rp is the projected range;
- ΔRp is the projected straggle;
- N_{Rp} is the maximum concentration at $x = Rp$

$$N_{Rp} = \frac{\phi}{\sqrt{2\times\pi}\times\Delta Rp}$$

ϕ is the dose of the implant

$$N(2.5\times10^{-6}) = 1\times10^{15}.cm^{-3}$$

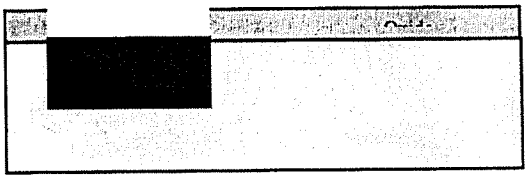
$$N(0) = 5\times10^{17}.cm^{-3}$$

If we assume that $\Delta Rp \cong 0.3\times Rp$, we found:

$N_{Rp} = 1.3\times10^{20}\,cm^{-3}$

And $Rp = 1.02\times10^{-6}\,cm$

Then $\Delta Rp = 3.05\times10^{-7}\,cm$ and $\phi = 9.9\times10^{13}\,cm^{-2}$



We finish by etch the oxide using B.O.E.
Termal SiO_2 BOE: Si (7:1) 1,000 Å/min. *

* RIT data, Dr. Fuller, et.al.

→30 seconds etching.

5th step: Pad oxide and LPCVD Nitride:

We grow a 250Å oxide using wet oxide at 900°C:
Wet Oxidation: $Si + 2H_2O\,(g) \longrightarrow SiO_2 + 2H_2\,(g)$

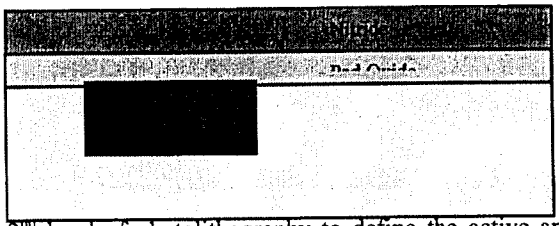
Using the Wet Oxide Growth Chart (Appendix 1), we need a time of oxidation equal to5 minute in the furnace.

After the growth oxide, we growth the nitride oxide using LPCVD:

DETAILS FOR RIT 6" LPCVD SYSTEM:

Silicon Nitride (Si_3N_4) (normal - stociometric):
Temperature = 790-800-810 °C Ramp from (door to pump)
Pressure = 375 mTorr
$3SiH_2Cl_2 + 4NH_3 = Si_3N_4 + 9H_2 + 3Cl_2$
Dichlorosilane (SiH_2Cl_2) Flow = 60 sccm
Ammonia (NH_3) Flow = 150 sccm
Rate = 60 Å/min +/- 10 Å/min

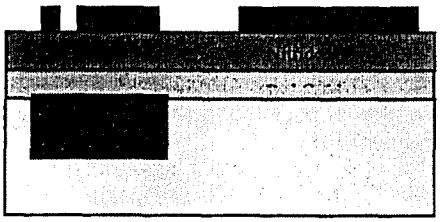
We need a layer of 1 000Å so we need a time deposition of 16min 40 s.
At the end of the deposition, the wafers appear blue.



2nd level of photolithography to define the active area (we use the same process than in the second step).
We etch nitride using BOE:
Nitride BOE 7:1 120 Å/min #
From Madou Text
We have a 1000Å nitride thickness so we need an etching time equal to 8min20sec.

We etch oxide using the same product:
Thermal SiO_2 BOE (7:1) 1,000 Å/min *

* RIT data, Dr. Fuller, et.al.
We have a 250Å nitride thickness so we need an etching time equal to 15sec.

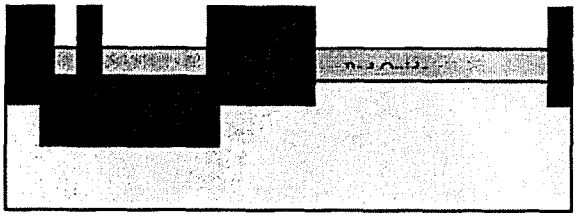


7th step: Field oxide:

We grow a 7500Å oxide using steam oxide at 950°C:
Using the Wet Oxide Growth Chart (Appendix 1), we need a time of oxidation equal to 6 hours in the furnace.
We finish by a photoresist Ash/RCA clean

8th step: Nitride etch, VT adjustment and oxide etch.

Using exactly the same recipe that describe in step number 6, we etch the nitride using B.O.E.



VT adjustment
We adjust the VT using B11 implantation: 2E12/cm2 @ 35 keV.

At the end we etch the oxide using the same recipe than in the 6th step

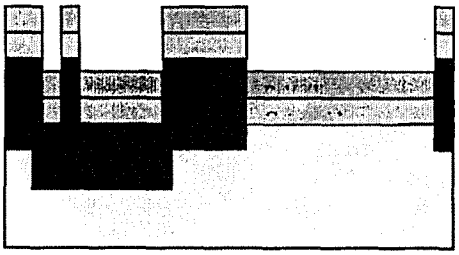
9th step: Gate oxide and LPVCD Polysilicon:

The next step consists to growth a 100Å dry oxide at 900°C.
Using the Dry Oxide Growth Chart, we need a time of oxidation equal to 15 minutes in the furnace.

For the Polysilicon we use the LPVCD Tools.

Polysilicon Deposition:
Temperature = 610 °C SiH4 = Si + 2H2
Pressure = 300 mTorr
Gas = Silane (SiH4) Flow = 90 sccm
Rate = 77 Å/min

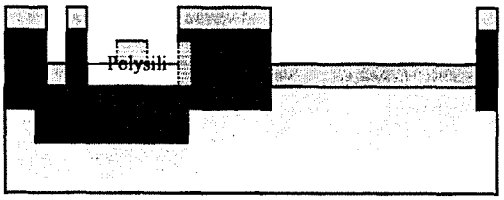
The growth rate is 77 Å/min and we need a layer of 1000Å so the time deposition is 13 minutes.



10th step: N+ poly dope and Polysilicon R.I.E.

We dope the polysilicon oxide using Emitter Diffusion Source N250 spin-on dopant (Emulsitone Co.).And we put the wafer in the furnace at 1000 °C for 20 min to make the dopant diffuse in the polysilicon.

The 4th level of photolithography will permit us to etch the polysilicon using the Drytech Quad RIE tool.



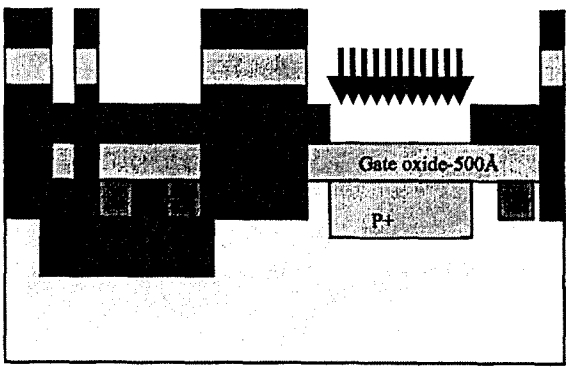
11th step: N+implant and P+ implant:

The 5th level of photolithography will permit us to create the N-implant of the NMOS.

N+ implant: P31 1E15cm-2 @35keV

The 6th level of photolithography will permit us to implant the P-well of the Diode.

P+ implant: BF2 1 E15 cm-2 @ 55keV



We finish this step by a Photoresist strip/RCA clean.

12th step: LTO oxide and contact etch.

We want to growth a 1000 Å layer of LPCVD oxide (LTO)-1000 Å
Low Temperature Silicon Oxide:
Temperature: 400 °C
$SiH_4 + O_2 = SiO_2 + 2H_2$
Pressure = 250 mTorr
Silane (SiH_4) Flow = 40 sccm
Oxygen (O_2) Flow =48 sccm
Rate = 70 Å/min +/- 10 Å/min

Wafers are loaded back to back in caged boat. The boat is filled with dummy wafer to total 25 wafers.

The growth rate is 70 Å/min and we need a layer of 1000Å so the time deposition is 15 minutes.

LT densification-source/drain activation anneal-900°C steam 30 min.

The 7th level of photolithography will permit us to etch the contact

We etch the contact using B.O.E.

SiO_2 (LTO) BOE (7:1) 3,300 Å/min #
From Madou Text

So the time etching is 18 seconds.
We finish by a Photoresist strip/ RCA clean.

13th step: Aluminium sputter and aluminum etch:

We depose aluminum using the CVC 601.

Material	Power (watts)	Rate
Aluminum	2000	240 Å/min.

The last level of photolithography will permit us to etch the aluminum.

We etch it using "Aluminum Etchant Type A" from Transene Co.
Then we do a Photoresist strip/RCA clean. And we finish by an Aluminum sinter-425°C 20 min H2/N2

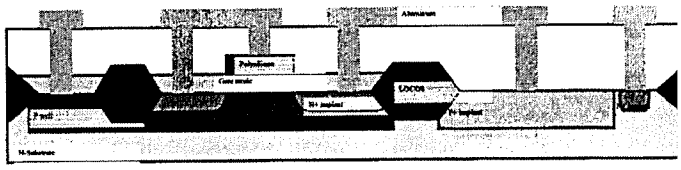


Fig.4. Realization of the inverter in Sub-CMOS.