On the Influence of Surface Treatment on Electrical Characteristics of Schottky Diodes

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Abstract— **The effect of surface treatment on electrical characteristics of aluminum-silicon contacts has been observed. It has been shown that the electrical characteristics of the contacts are affected by the quality of the interfacial oxide and sintering conditions. Four different surface treatments were performed on the silicon prior to metal deposition to vary the thickness and quality of the interfacial oxide. Four different sintering conditions were performed on the wafers to determine the effect of temperature and ramp-down rates. Three methods of calculating barrier height were used: current-voltage, current-temperature, and capacitance-voltage. Some results correlated well with previous reported work, however other results demonstrated inconsistencies that require further investigation.**

Index Terms—**Schottky, Diode, Surface Treatments, Electrical Characteristics**

I. Introduction

Metal-semiconductor diodes, also known as Schottky Barrier Diodes, find numerous applications in integrated circuits. These devices are typically used where a low turn-on voltage or high switching speed is needed. Bringing a metal in intimate contact with a low-doped (less than 10^{17} impurity atoms per cubic centimeter) semiconductor may form a Schottky diode. The difference in workfunction between the metal and semiconductor forms a potential barrier for the electrons (holes) to pass. The current flow is due to the majority carrier injection over the potential barrier, or thermionic emission, with an applied forward bias. The Schottky diode achieves its high speed because of the majority carrier flow, compared to the PN junction diode, in which the current is dependent on the diffusion of minority carriers. In the Schottky diode there are no minority carrier storage effects, allowing the diode to operate much faster. One application where these devices may prove to be useful is in electrically-injected optical modulators, which is part of an active research effort between RIT Microelectronic Engineering and University of Rochester Institute of Optics.

Most metal-semiconductor contacts have non-idealities such as: image force induced barrier height lowering, impurities in the silicon, the native oxide that forms almost instantly on the surface, and surface damage [2]. The non-idealities make the electrical characteristics hard to predict. Effects were investigated through an experiment that was designed to give a variety of surface conditions. The following behavior has been shown by aluminum on n-type silicon Schottky diodes in previous work [1].

1) The initial barrier decreases with increasing oxide thickness (suspected to be due to positive charge in the oxide)

2) The barrier height of a freshly fabricated contact is about 0.45eV, but changes to 0.7eV over time (greater than 100days) if no heat treatments are applied. Sintering the device allows the contact to reach a 0.7eV barrier height immediately.

3) The barrier height will vary with varying sinter temperature.

4) The ramp-down rate of the sinter will affect the barrier height due to dissolution of silicon in the aluminum. The silicon comes out of solution and deposits at the interface as a p-type doped layer. A fast ramp-down will cause less silicon to deposit.

Aluminum on n-type silicon Schottky diodes were fabricated and tested. The forward bias I-V curve and reverse leakage were used as the initial indicators of the metal-semiconductor junction performance; further testing was used to extract the barrier height of the devices. The effect of sintering on device performance was also investigated. The silicon surface conditions included a near-perfect surface with a minimal amount of native oxide and little contamination, a surface with native oxide, a surface with a very thin thermal oxide, and a chemically oxidized surface.

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II. THEORY

A. Ideal MS contacts

The Schottky barrier diode is formed by bringing a metal in direct contact with a moderately to low doped semiconductor. The difference in workfunction between the metal and semiconductor ideally gives the junction its rectifying characteristics if the metal has a higher workfunction than the semiconductor. Figure 1 shows the energy band diagrams of the two materials and the effect of bringing them together.

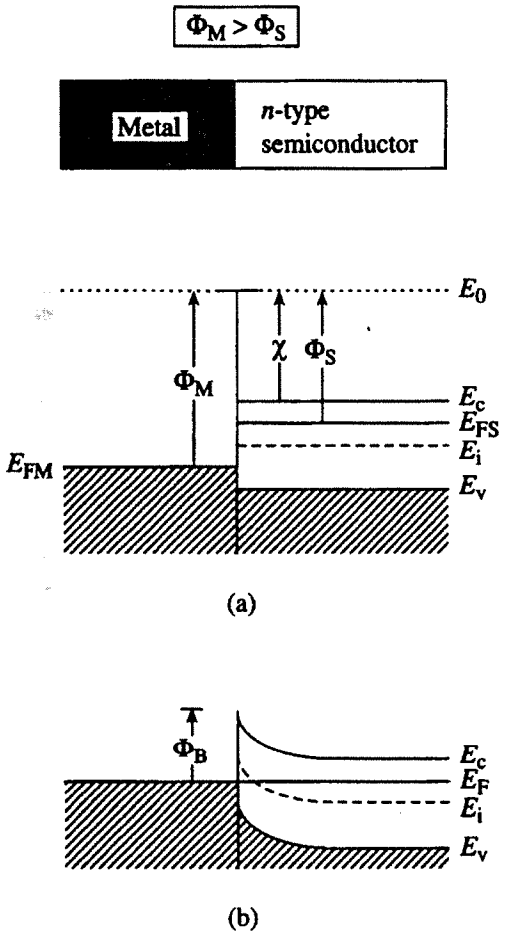


Figure 1: Energy Band Diagrams for the ideal metal-semiconductor junction (a) before equilibrium conditions are observed (no interaction) and (b) under equilibrium conditions (source: Robert F. Pierret, *Semiconductor Device Fundamentals*, 479)

The workfunction, Φ, of the material is the energy difference between the Fermi level energy and the vacuum level energy, as shown by Fig. 1a. The metal workfunction, Φ_M, remains constant for the given metal, while the semiconductor workfunction, Φ_S, varies with the doping of the substrate, and is given by the equation:

$$\Phi_S = X + (E_C - E_F) \quad \text{(Eq. 1)}$$

at flat band, where X is the electron affinity, a constant of the given semiconductor (4.03eV for silicon). The variation due to doping is given by $(E_C - E_F)_{FB}$ which is given by the following equation:

$$(E_C - E_F) = (E_C - E_I) - (E_F - E_I) \quad \text{(Eq. 2)}$$

Where $(E_C - E_I)$ is approximately half the band gap of the silicon, or 0.56eV, and $(E_F - E_I)$ is given by the equation:

$$(E_F - E_I) = kT \ln(N_D/n_i) \quad \text{(Eq. 3)}$$

The diagrams in Fig 1a show the energy band diagrams before reaching an equilibrium condition. Fig 1b shows the energy band diagrams shortly after the metal contacts the semiconductor, when equilibrium conditions are met. In order to bring the Fermi levels of the two materials to the same level, electrons transfer from the semiconductor to the metal. This creates a depletion region of ionized donor locations in the semiconductor near the metal-semiconductor junction and a delta function of electrons on the metal surface at the interface. This situation sets up an electric field that repels the transfer of additional electrons, and the transfer of electrons stops when equilibrium conditions are met. This sets up a surface potential energy barrier, Φ_B, given by:

$$\Phi_B = \Phi_M - X \quad \text{(Eq. 4)}$$

This is illustrated in Fig 1b.

The built-in potential of the Schottky diode is given by the difference in the semiconductor energy level of the conduction band at flat-band conditions and at the interface, or simply:

$$\Phi_{bi} = \Phi_B - (E_C - E_F)_{FB} \quad \text{(Eq. 5)}$$

or

$$\Phi_{bi} = \Phi_M - \Phi_S \quad \text{(Eq. 6)}$$

using Equations 1, 4, and 5. This gives the built-in voltage of the device to be:

$$V_{bi} = q(\Phi_M - \Phi_S)$$

(Eq. 7)

B. Nonidealities of the MS contact

The ideal aluminum-n-type silicon junction should not produce a Schottky contact. The workfunction of aluminum is 4.23eV, and the electron affinity of the silicon is 4.05eV. This gives an ideal barrier height of only 0.18eV. The saturation current for barrier heights of less than 0.3eV is greater than 100 A/cm^2 and cannot be distinguished from an ohmic contact at room temperature [1]. Therefore the aluminum-n-type silicon Schottky diode is dependent on the non-idealities for its operation.

The equations given in Part A of this section are based on an ideal metal-semiconductor junction. Most metal-semiconductor contacts are not ideal due to several reasons, which include: image force induced barrier height lowering, impurities in the silicon, the native oxide that forms almost instantly on the surface, and surface damage. The impurities in the silicon may act as charge centers at the junction and will affect the barrier height by "pinning" the equilibrium Fermi level [2]. This makes the barrier height hard to predict in the best case, and a non-functioning device in the worst. This may also result in increased leakage in the device. Native oxide on the silicon surface prevents the metal and semiconductor from forming a perfect contact. It is assumed that the oxide layer will be transparent to electrons flowing through it, but can support a potential difference. Metal deposition, especially sputtering, may cause additional surface damage to the crystal structure, making the junction less ideal and may cause additional leakage or other electrical performance degradation. If high temperatures are used in the process, diffusion of the metal may occur (or diffusion of the silicon into the metal), severely affecting the junction and electrical characteristics. Figure 2 shows what the band diagram may look like including the nonidealities of the junction.

There are three basic non-idealities that have a significant influence the effective barrier height. The Schottky Effect is a lowering of the barrier height ($\Delta\phi$) due to the induced image force formed when an electron in a dielectric (depleted silicon) is in proximity to a metal. Surface states related to a native oxide interface can influence the semiconductor surface potential, and thus alter the effective barrier height. Lastly, the barrier height may have some temperature dependence. In this work, only the influence of surface states is considered to be significant in altering the effective barrier height determined from experimental measurements.

There are some acceptor-like states at the surface of the semiconductor. If we take the density of the states, D_s ($cm^{-2}eV^{-1}$), to be a constant over the energy range from $q\phi_0$ to the Fermi level, the surface state charge density, Qss, is given by [8]:

$$Q_{ss} = -qD_s(E_g - q\phi_o - q\phi_{Bn} - q\Delta\phi)$$

Coul/cm^2

(Eq. 8)

where symbols are consistent with the definitions in figure 2. The space charge density is given by the equation:

$$Q_{sc} = \sqrt{2q\varepsilon_s N_D\left(\phi_{Bn} - V_n + \Delta\phi - \frac{kT}{q}\right)}$$

Coul/cm^2

(Eq. 9)

The potential, Δ, across the interfacial native oxide layer of thickness δ is given by the equation:

$$\Delta = -\delta\frac{-Q_{ss} - Q_{sc}}{\varepsilon_i}$$

(Eq. 10)

Where ε_i is the permittivity of the oxide layer. The energy band diagram gives an alternate equation for the potential across the oxide layer:

$$\Delta = \phi_m - (\chi + \phi_{Bn} + \Delta\phi)$$

(Eq. 11)

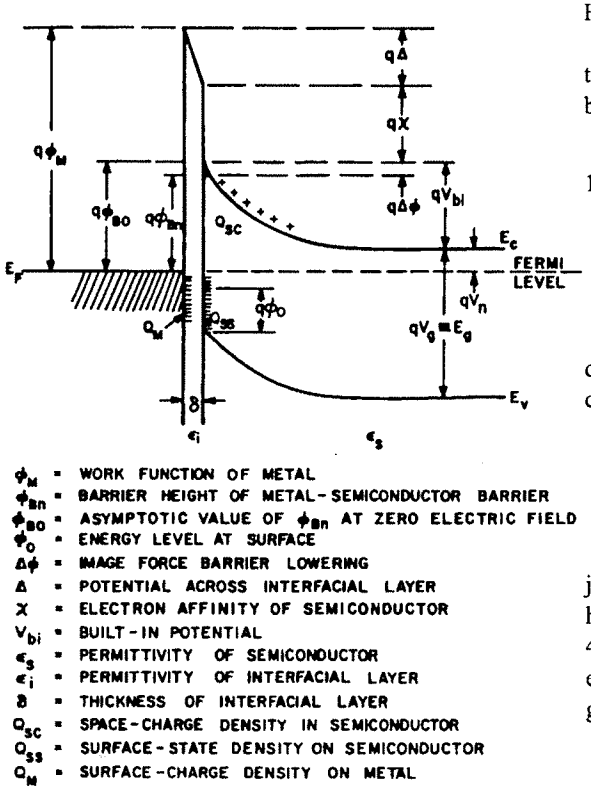


Figure 2: Energy Band Diagram for the non-ideal metal-semiconductor junction, including oxide interface layer, Schottky barrier lowering, and surface states.
(source: S. M. Sze, *Physics of Semiconductor Devices, 2nd Ed.*, 271)

Combining Equations 8-11 gives the equation:

$$(\phi_m - \chi) - (\phi_{Bn} + \Delta\phi) = \sqrt{\frac{2q\varepsilon_s N_D \delta^2}{\varepsilon_i^2}\left(\phi_{Bn} + \Delta\phi - V_n - \frac{kT}{q}\right)} - \frac{qD_s\delta}{\varepsilon_i}(E_g - q\phi_o - q\phi_{Bn} - q\Delta\phi)$$

(Eq. 12)

Using Equation 12, it can be shown that as the surface state density goes to infinity and solving for ϕ_{Bn} gives:

$$\phi_{Bn} = \frac{1}{q}(E_g - q\phi_o) - \Delta\phi$$ (Eq. 13)

This shows that as Qss becomes large, the barrier height becomes dependent on the band gap energy and surface potential, and independent of the metal workfunction and semiconductor electron affinity. The Fermi level is pinned at the surface potential, ϕ_o.

It can be shown that as the surface state density goes to zero Equation 12 returns the ideal expression for the barrier height with the Schottky effect term:

$$\phi_{Bn} = (\phi_m - \chi) - \Delta\phi$$ (Eq. 14)

III. Measurement of Barrier Height

A. Current-Voltage Method

The barrier height of the Schottky diode can be derived from the forward biased current-voltage characteristics using the equation:

$$J = A^{**}T^2 \exp\left(-\frac{q\phi_{Bn}}{kT}\right)\exp\left[\frac{q(\Delta\phi + V)}{kT}\right]$$

(Eq. 15)

where A^{**} is the effective Richardson constant of the junction and V is the applied voltage. This equation holds true if the forward bias voltage is greater than 4kT/q. The saturation current, J_S, is found by extrapolating the current density at zero voltage. This gives the equation:

$$J_S = A^{**}T^2 \exp\left(-\frac{q\phi_{Bn}}{kT}\right)$$

(Eq. 16)

This equation can be rearranged to find the barrier height:

$$\phi_{Bn} = \frac{kT}{q}\ln\left(\frac{A^{**}T^2}{J_S}\right)$$

(Eq. 17)

The value for A^{**} doesn't effect the calculation of ϕ_{Bn} considerably, if the value is changed by a factor of two, the resulting barrier height is only changed by 0.018eV. The published values for this variable are accurate enough for barrier height calculations.

The ideality factor, an indication of how the real data deviates from the ideal contact, is need due to the dependence of A** and $\Delta\phi$ on the applied voltage. Replacing kT by nkT, the ideality factor, n, can be calculated from the current-voltage data as well. The slope of the plot is now:

$$m = \frac{q}{nkT}$$

(Eq. 18)

and can be re-arranged to give n:

$$n = \frac{1}{m}\frac{q}{kT}$$

(Eq. 19)

The ideality factor is also needed for the barrier height calculation using the current-temperature method.

B. Current-Temperature Method

The current-temperature method of extracting barrier height has the advantage that it isn't affected by electrically active area, which may vary from the device area. The calculation assumes that the barrier height is not dependent on temperature. The temperature of the contact is varied as the current is measured for a given forward bias voltage above turn-on. The barrier height is extracted from the equation:

$$\phi_{Bn} = \frac{V_1}{n} - \frac{k}{q}\frac{\Delta(\ln(I/T^2))}{\Delta(1/T)}$$

(Eq. 20)

Where V_1 is the applied bias and n is the ideality constant that is extracted from the I-V characteristics.

C. Capacitance-Voltage Method

The barrier height may also be calculated from the capacitance-voltage relationship. The equation for the capacitance per unit area is given by:

$$\frac{C}{A} = \sqrt{\frac{q\varepsilon_s\varepsilon_0 N_D}{2(-V_{bi} - V - kT/q)}}$$

(Eq. 21)

where V is the reverse bias voltage. The barrier height is related to the built in potential following the equation:

$$\phi_{Bn} = V_{bi} + V_0$$

(Eq. 22)

Where Vo is given by the equation

$$V_0 = \frac{kT}{q}\ln\left(\frac{N_c}{N_D}\right)$$

(Eq. 23)

given the effective density of states, N_c.

Plotting $(A/C)^2$ versus the reverse bias voltage gives a line with a slope of

$$m = \frac{2}{q\varepsilon_s\varepsilon_0 N_D}$$

(Eq. 24)

from which the doping concentration can be extracted, and an x-intercept of

$$V_i = -V_{bi} + \frac{kT}{q}$$

(Eq. 25)

This gives the barrier height to be

$$\phi_{Bn} = -V_i + V_0 + \frac{kT}{q}$$

(Eq. 26)

IV. Experimental Details

The contacts were fabricated on 4 inch 15 ohm-cm n-type silicon wafers. The backside was heavily doped n-type using spin-on dopant and driving it in using a furnace to create an ohmic backside contact. Prior to metal deposition, the surface was treated as given in Table 1. After surface treatment, the aluminum was deposited by evaporation to a thickness of 5000Å. A base pressure of $4x10^{-6}$ torr was achieved. The "Minimal Oxide" wafers were transported to the evaporator and were under vacuum in less than 5 minutes after drying them to reduce the amount of native oxide grown. The other wafer splits were exposed to atmosphere for up to an hour before being loaded into the evaporator and achieving vacuum, possibly increasing the amount of native oxide formed.

The wafers were then patterned and the aluminum was etched to give diodes of varying size. The smallest feature size, $0.001cm^2$, was used for testing. The backside aluminum was then deposited to a thickness of 5000Å. After metal deposition, the wafers were cleaved into four quadrants. Each quadrant received a unique sinter, as shown in Table 1. The ramp-down conditions are shown in Table 2. The sintering was done in forming gas (H_2/N_2) for 15minutes.

V. Experimental Results

A. Current-Voltage

Current-Voltage (I-V) plots can be used to extract the barrier heights of Schottky diodes. The forward and reverse bias current was plotted for all experimental conditions. A value of 112 ($A{\cdot}cm^{-2}K^{-2}$) was used for the Richardson constant [2]. Representative forward bias plots of the minimal oxide and chemical oxide conditions are shown in Figures 3 and 4, respectively. The results extracted from these plots are shown in Tables 3 and 4, respectively. The figures show a "hump" in the plot between 0 and 0.1V. The current is higher than expected, due to recombination current. Where the ideality is close to 1, thermionic current dominates. The trend shows that the current in the non-sintered device is higher than the others, and is an ohmic contact for the chemical oxide surface treatment. This can be observed on a linear scale plot, as shown in Figure 4a. It is also noted that the barrier height of the non-sintered devices is much lower than the sintered devices. The two 450C splits are nearly identical, with the slow ramp-down sinter having slightly less current. The 350C sinter plot does not show a repeatable trend between splits, but is clearly different than the non-sintered sample in each case.

The native oxide surface condition split, shown in Figure 5, closely resembles the minimal oxide surface condition split. The one obvious difference is that the

Wafer	Surface Treatment	Quad	Sinter
1	Quick Clean: BOE 1min Rinse 1min Blow dry with N2	A	450C, Fast ramp-down
		B	450C, Slow ramp-down
		C	350C, slow ramp-down
		D	None
2	Quick Clean: BOE 1min Rinse 1min Blow dry with N2	A	450C, Fast ramp-down
		B	450C, Slow ramp-down
		C	350C, slow ramp-down
		D	None
3	Native: BOE 1min Rinse 10min SRD	A	450C, Fast ramp-down
		B	450C, Slow ramp-down
		C	350C, slow ramp-down
		D	None
4	Native: BOE 1min Rinse 10min SRD	A	450C, Fast ramp-down
		B	450C, Slow ramp-down
		C	350C, slow ramp-down
		D	None
5	Low Temp Oxide Push in at 400C, N2 Ramp to 700C, O2 Ramp down in N2 (no soak)	A	450C, Fast ramp-down
		B	450C, Slow ramp-down
		C	350C, slow ramp-down
		D	None
6	Low Temp Oxide Push in at 400C, N2 Ramp to 700C, O2 Ramp down in N2 (no soak)	A	450C, Fast ramp-down
		B	450C, Slow ramp-down
		C	350C, slow ramp-down
		D	None
7	Chemical Oxide: HPM bath for 5min Rinse 5min SRD	A	450C, Fast ramp-down
		B	450C, Slow ramp-down
		C	350C, slow ramp-down
		D	None
8	Chemical Oxide: HPM bath for 5min Rinse 5min SRD	A	450C, Fast ramp-down
		B	450C, Slow ramp-down
		C	350C, slow ramp-down
		D	None

TABLE 1
EXPERIMENTAL CONDITIONS

TABLE 2
RAMP-DOWN PROCEDURES FOR SINTER

Ramp-down	Conditions
Fast	Pull out of furnace tube quickly and place wafer quadrants on cool plate immediately
Normal	Pull out of tube slowly and allow wafer quadrants to cool to room temperature while remaining in wafer boat
Slow	Let wafers cool to <100C in furnace tube over several hours before pulling and allowing to cool to room temperature while remaining in wafer boat

350C sinter curve matches the 450C sinter curves for the native oxide condition.

The low-temperature thermal oxide wafers showed different results, shown in Figure 6. Wafer 5 (plot not shown) resulted in an open circuit on all die tested. Wafer 6 had curves for the two 450C that resembled the curves for the other surface conditions, but the no-sinter and 350C sinter showed much less current. The reverse bias current for each split, Figures 7-11, show that the 450C slow ramp-down spit has lower leakage for every surface condition, while the no-sinter split continually has higher leakage. The ohmic nature of the chemical oxide, no-sinter split is shown again in Figure 11.

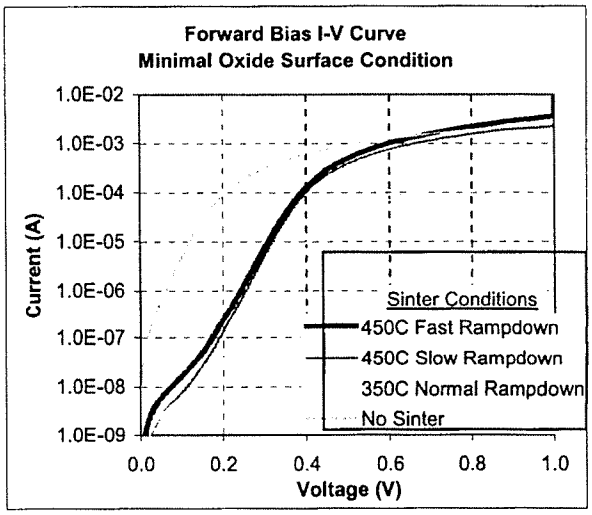


Figure 3: Forward I-V characteristic for minimal oxide surface treatment for various sinter conditions

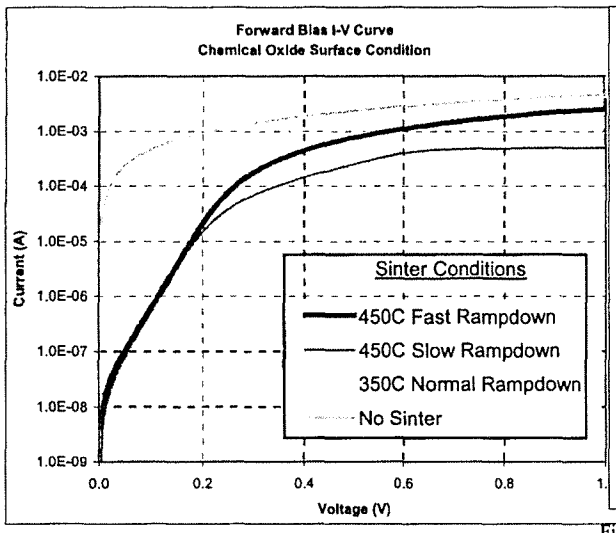


Figure 4: Forward bias I-V curve for chemical oxide surface treatment for various sinter conditions

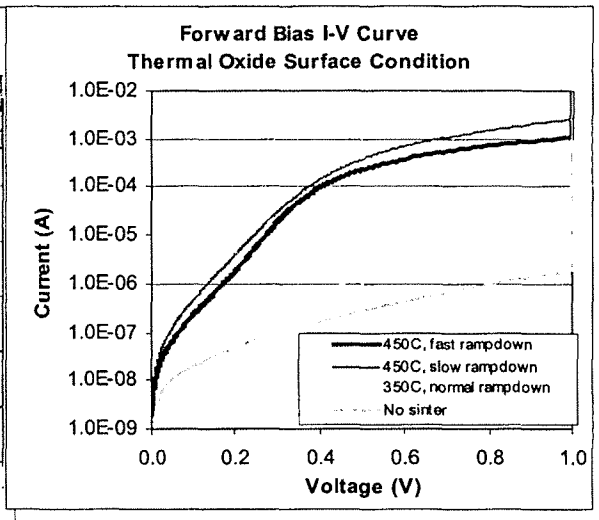


Figure 6: Forward bias I-V curve for low temperature thermal oxide surface treatment for various sinter conditions

TABLE 3
RESULTS FOR MINIMAL OXIDE SURFACE TREATMENT

Parameter	450C Fast Ramp down	450C Slow Ramp down	350C, Normal Ramp down	No Sinter
n	1.170	1.113	1.233	0.953
ϕ_B (eV)	0.803	0.827	0.851	0.662

TABLE 4
RESULTS FOR CHEMICAL OXIDE

Parameter	450C Fast Ramp down	450C Slow Ramp down	350C, Normal ramp down	No Sinter
n	1.088	1.090	1.709	4.152
ϕ_B (eV)	0.703	0.704	0.579	0.465

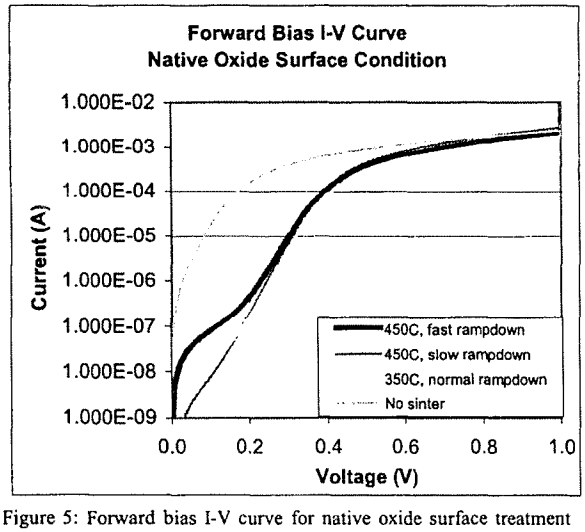


Figure 5: Forward bias I-V curve for native oxide surface treatment for various sinter conditions

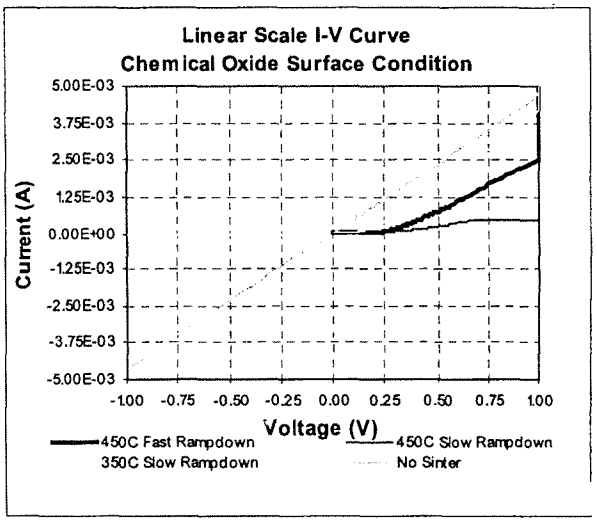


Figure 4a: Linear scale I-V curve for chemical oxide surface treatment for various sinter conditions.

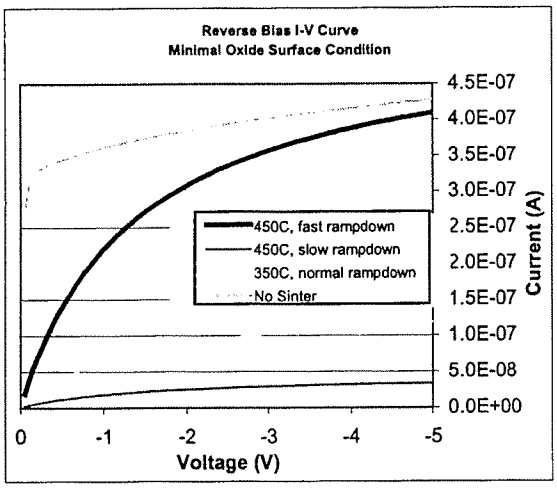


Figure 7: Reverse bias I-V characteristic for minimal oxide surface treatment for various sinter conditions.

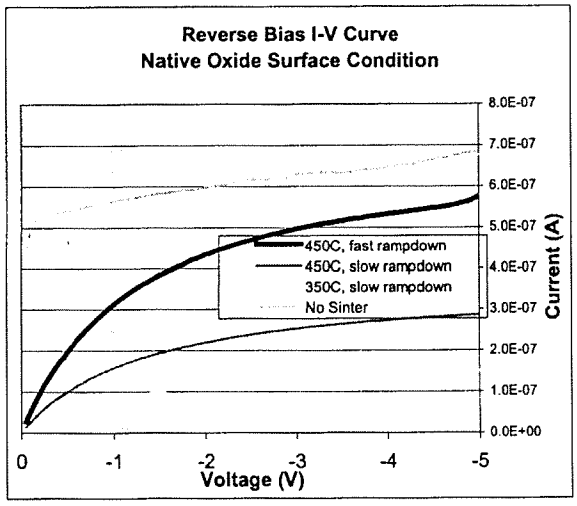
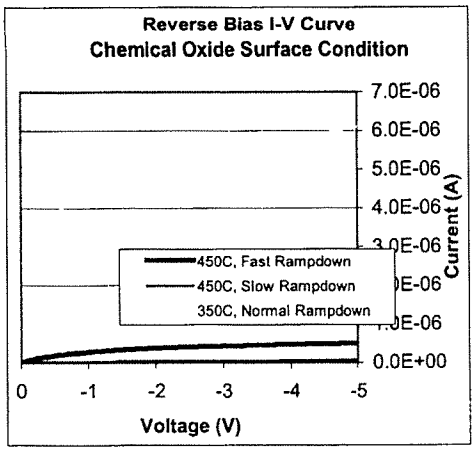


Figure 8: Reverse bias I-V characteristic for native oxide surface



treatment for various sinter conditions.

Figure 9: Reverse bias I-V characteristic for chemical oxide surface treatment for various sinter conditions.

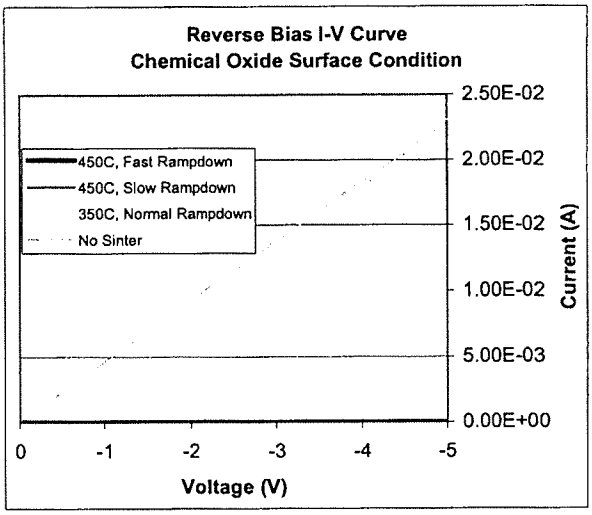


Figure 10: Reverse bias I-V characteristic for native oxide surface treatment for the non-sintered split

B. Current-Temperature

Current-temperature (I-T) measurements can also be used to determine the barrier height of a Schottky diode. The plot of the data collected for the minimal oxide, native oxide, and chemical oxide surface condition splits are shown in Figures 11-13. The calculated barrier height for each split is summarized in Table 5.

The values were calculated using the ideality factor from the I-V calculations. The barrier height values are significantly lower than the values calculated using the I-V method. The plot of the minimal oxide and native oxide surface conditions show that the sintered splits, regardless of temperature and ramp-down, are nearly identical, while the no-sinter split shows significantly different behavior. The plots of the two 450C sinter splits for the chemical oxide surface condition also show less of a slope, making the calculated barrier height much lower. The plots are also non-linear, showing a lot of curvature.

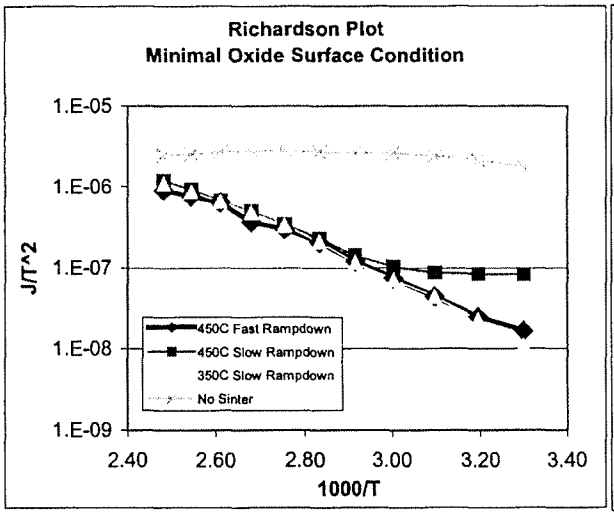


Figure 11: I-T characteristic for minimal oxide surface treatment for the various sinter conditions

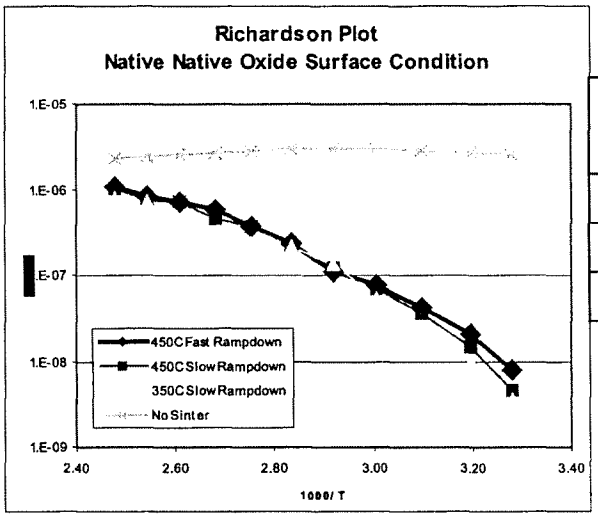


Figure 12: I-T characteristic for native oxide surface treatment for the various sinter conditions

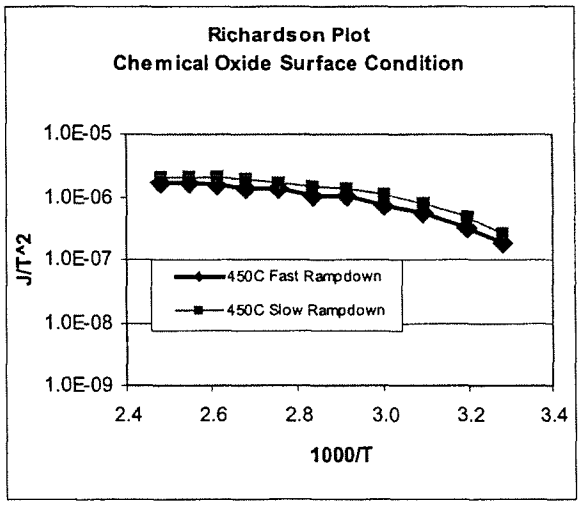


Figure 13: I-T characteristic for chemical oxide surface treatment for the various sinter conditions.

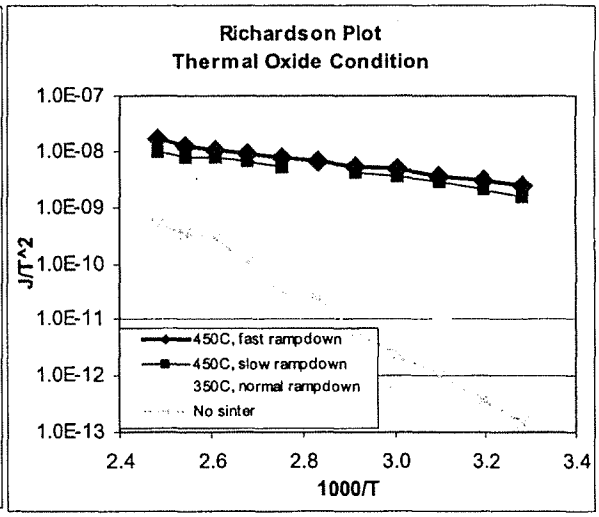


Figure 14: I-T characteristic for thermal oxide surface treatment for the various sinter conditions

TABLE 5
SUMMARY OF CURRENT-TEMPERATURE CALCULATED BARRIER HEIGHT

Surface Condition	450C Fast Ramp down	450C Slow Ramp down	350C, Normal Ramp down	No Sinter
Minimal Oxide	0.612	0.598	0.649	0.239 (ohmic)
Native Oxide	0.672	0.703	0.745	0.183 (ohmic)
Chemical Oxide	0.308	0.310	--	--

C. *Capacitance-Voltage*

The plot of the results for the minimal oxide surface treatment for various sinter conditions is shown in Figure 15. A linear fit to the data has a negative intercept for the 450C fast ramp-down and 350C splits, giving a negative barrier height for the 350C split, which isn't feasible. The nature of the plot requires the intercept to be greater than zero. No calculations were made using the data for any split due to the measurement noise.

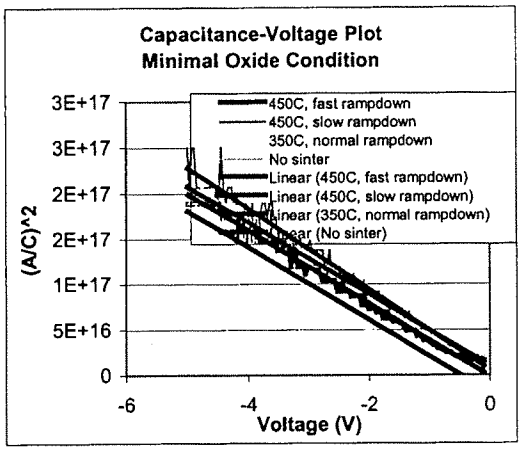


Figure 15: C-V characteristic for minimal oxide surface treatment for the various sinter conditions.

VI. Discussion of Results

The recombination current can double the ideality factor [3], increasing the forward bias current at low bias. This is shown in the forward bias I-V characteristic plots for all sinter conditions except the no-sinter split. Taking sample calculations in this area on the minimal oxide give an ideality factor of about double that measured at higher bias voltages, concurring with the suggestion that it is recombination current that is increasing the current. The two 450C sinter splits (fast and slow ramp-down) are nearly identical for all surface treatment conditions, except the slow ramp-down has slightly less current. This shows that the re-crystallized silicon has little effect on the barrier height, but the additional interfacial layer may decrease the current flowing through the device.

There is little difference between the plots for the minimal oxide and the native oxide surface treatments. This is an indicator that the relative thickness of the oxide has little effect on the barrier height in comparison to the quality of the oxide (for thin oxides, <20Å). The difference shown in the chemical and thermal oxide splits re-affirms this argument.

Comparing the different splits on Wafer 6, and taking into consideration Wafer 5 has oxide thick enough to create an open circuit; it shows that the 450C sinter was effective at consuming the native oxide. The 450C sinter, for both slow and fast ramp-downs, matches the characteristic of the other plots while the no-sinter and 350C sinter had much less current, this may be due to the remaining oxide.

The above explanations show that sintering the devices is important to maintain control over the electrical characteristics of the device. Sintering is important to "age" the device and maintain the same barrier height over time, reduce the charge at the interface that may, in the extreme case, cause an ohmic contact, and consume the native oxide.

The data presented for the I-T measurements show values for the barrier height that are much lower than the I-V calculations, however there is a greater lack of confidence in the I-V results. Since the I-V method depends on the y-axis intercept for the barrier height, and the I-T method uses the slope of the plot over a range of temperatures, the I-T method is expected to be more reliable.

The results for the no-sinter split for the minimal oxide and native oxide do not follow the same linear relationship as the other splits. The barrier height calculated for these splits is 0.18eV to 0.24eV, which can be considered an ohmic contact [1]. The barrier height for the no-sinter split is lower in both I-V and I-T calculations. Although the calculations to determine the effective barrier height are assumed to be incorrect, this may indicate the time-dependent nature of the metal-semiconductor contact. Since the devices were not sintered, and they were tested only seven days after fabrication, the barrier height has not aged and therefore is much lower than the sintered splits.

There is a slight curvature to the I-T plots for the chemical oxide surface condition. This could be explained by two different mechanisms. The first mechanism is that the barrier height may be temperature dependent. As the wafer is heated or cooled, the barrier height changes, making the data from this type of measurement useless without further in-depth analysis and calculations. The second possible mechanism is the increased series resistance as the wafer is heated. The mobility of the carriers, especially the highly doped backside contact, will decrease rapidly with temperature, increasing the resistance to current flow.

The data from the C-V measurements can quickly be discarded due to the intercept of one of the linear-fit lines being less than zero, making the barrier height negative. The measurement tool should be checked and the measurements retaken. This method of barrier height extraction needs to be investigated further.

VII. Conclusion

It was shown that sintering the device is crucial to proper operation. This speeds up the aging process and reduces the interfacial charge. It has been shown that a 450C sinter with slow cool-down will produce a device with a repeatable electrical characteristics and minimal leakage current.

It was also shown that the relative thickness of the oxide had less to do with the electrical characteristics than the quality of the oxide. The native and minimal oxide splits showed very close results despite the oxide thickness difference, but the lesser-quality chemical and

thermal oxides showed poor device performance in comparison. Sintering helped to bring the poor-oxide-quality (chemical and thermal) contacts close to the operation of the higher-quality-oxide contacts through the removal of interface states. The thermal oxide split also showed the importance of reduction in interfacial oxide; where the difference between the no-sinter, low temperature sinter, and high temperature sinter was very significant.

The importance of using more than one method to measure barrier height was strained during this experiment. The lack of correlation between measurement techniques shows that there is a definite issue with one or more of the methods, possibly due to the measurement tools. Poor results may be taken as fact if only one measurement technique is used.

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