Design and Fabrication of FinFETs on SOI Substrates

Steven D. Kirby

Abstract—**A Fin Field Effect Transistor (FinFET) is one of several novel devices that may be used in the future to minimize short channel effects. The FinFET is fabricated on silicon on insulator (SOI) substrate and uses basic integrated circuit processing techniques to obtain a double gate structure. The double gate structure helps to improve subthreshold characteristics and provides low leakage current. The objective of this project was to improve the FinFET device built at RIT. Functioning FinFETs were designed and fabricated previously at RIT. The new design and process changes will help in the understanding of issues found in previous test results. The design includes FinFET structures, fin resistors to determine series resistance, and contact structures. The process flow was based on the flow used previously at RIT. One processing change is the use of rapid thermal anneal (RTA) as opposed to furnace anneals. The fabrication of FinFETs was completed. The testing showed that there was a contact resistance issue along with a high shunt conductance. The resulting threshold voltage was approximately 1V. There was no obvious difference in the threshold voltage or saturation current between the planar and FinFET devices.**

I. Introduction

The need to make faster, cheaper devices has forced the microelectronic industry to scale MOSFETs (metal oxide semiconductor field effect transistor) to smaller sizes. As they are scaled below 50nm, it will become more difficult to deal with short channel effects. It will become necessary to find a new structure that can help to overcome these problems.

One recent improvement that has become very common in many applications is the use of SOI devices. These result in devices that are isolated from the bulk of the substrate. This results in lower source/drain capacitances. It also allows for lower power consumption and/or higher speeds.

One novel device that uses the benefits of SOI is a FinFET. The FinFET consists of a thin silicon fin connecting the source drain contact areas. The gate surrounds the fin. This structure allows the device to act as a double gate device. The FinFET gains the benefits of both SOI and double gate devices.

Manuscript received on May 20, 2003.

Fig. 1 shows the basic FinFET design.

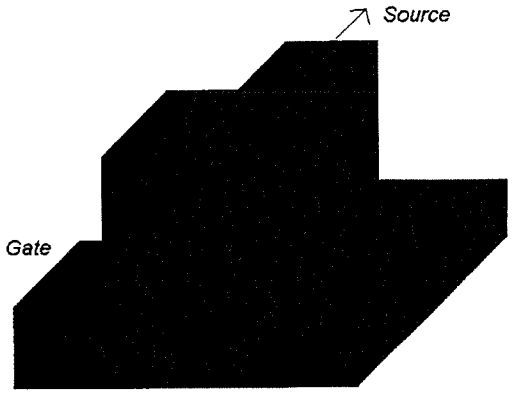

Fig 1. Basic FinFET Design

The FinFET is a double gate device. The surround gate is able to control the current from both sides of the channel. As the aspect ratio of the fin is increased, the top surface has little control in comparison to the sides. This double gate allows for more gate control. This gate control results in better subthreshold characteristics including subthreshold swing and lower leakage current. It is also possible to achieve high drive currents with small-area devices.

There are some issues with the design and fabrication of a FinFET device. The silicon thickness on the SOI substrate must be dealt with. This needs to be fairly thin but high aspect ratios for the fin must also be met. This is difficult when the silicon thickness reaches the couple thousand-angstrom range. The gate stack is also more difficult. It is desired to form the gate stack on the vertical sidewalls. It is very difficult to get a uniform gate oxide and conductor on the sidewalls. Another problem is the lack of an accurate TCAD model for the FinFET making the device very difficult to model.

Although there are many difficulties associated with FinFETs, there are also many benefits. FinFETs have the advantages low source/drain capacitance, lower power and high speed like an SOI device, but also add the benefits of double gate devices. According to the ITRS, the FinFET could be a common device in future semiconductor applications.

II. Design and Fabrication

A. Design of a FinFET

FinFETs were designed and fabricated previously at RIT[3]. Functioning devices were testing. The results showed that there was a large amount of series resistance. The new design contains structures that will help in the understanding of this series resistance and functioning of the FinFET. The design includes FinFETs with varying fin and gate widths (1 to 4 μm). It also includes fin resistors (no gate) and Transfer Length Method (TLM) structures were included. The design also included FinFET devices with short fins in an attempt to minimize the series resistance.

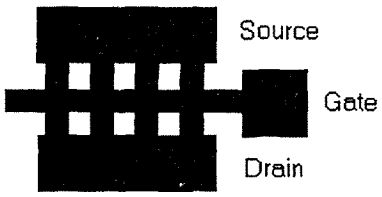

Fig. 2: Basic Layout of a FinFET device

B. Fabrication of a FinFET

FinFETs were fabricated using the previously fabricated mask. The starting substrate was p-type SOI with a 1900 A silicon layer over 4000A buried oxide. Regular p-type crystalline silicon wafers were also used. The process used was similar to the previously used process with a few key differences. Previously, the silicon fin etch and the poly gate etch were done using the STS deep RIE tool. The process presented here uses a Drytek Quad RIE tool with SF6 and CHF3 plasma for the Si fin etch and a Lam plasma etcher with SF6 and O2 for the gate etch. This process also uses rapid thermal annealing (RTA) for the implant anneal step as opposed to a long furnace anneal. RTA is used to help with the thermal budget, which will become smaller when the FinFET is scaled smaller in the future at RIT. For this process, all patterns were defined using a GCA g-line stepper with a minimum critical dimension of 1μm. Table 1 gives an overview of the process used.

Step	Process
1	Litho Level 1: S/D/Fin Definition
2	Si Etch (Drytek Quad RIE)
3	Gate Oxide Growth (150A, Dry O2, 1000C)
4	Gate Poly Dep (3000A LPCVD)
5	Litho Level 2: Gate Definition
6	Poly Gate Etch (LAM Plasma Etcher)
7	Sac Oxide Growth (100A Dry O2, 1000C)
8	SA Gate Implant (P31, 1E15, 55keV
9	RTA (1000C, 30sec)
10	LTO Dielectric (3000A LPCVD)
11	Litho Level 3: Contact Cut Definition
12	CC Etch isotropic Buffered HF
13	Metal Dep: Sputter Al/Si (1%)
14	Litho Level 4: Metal Definition
15	Metal Etch: Isotropic Wet Etch
16	Sinter: 425C 30 minutes

Table 1: Process Overview for FinFET Fabrication

Fig. 3 and 4 show pictures from an optical microscope of the completed FinFETs.

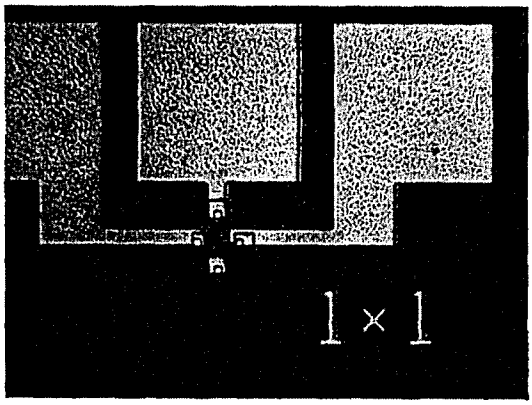

Fig. 3: Optical Picture for 1μm X 1 μm FinFET

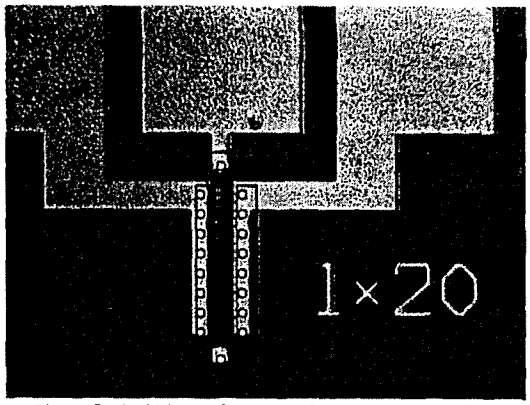

Fig. 4 Optical Picture for 1μm X 20um FinFET (20 fins)

III. Results and Analysis

Electrical testing was done on the fabricated FinFET devices. The testing was done on an HP4145 analyzer.

The devices on the SOI substrate showed functioning field effect. A family of curves and threshold voltage were achieved for various FinFET sizes. Fig. 5 shows the family of curves plot for a 2x20 μm FinFET.

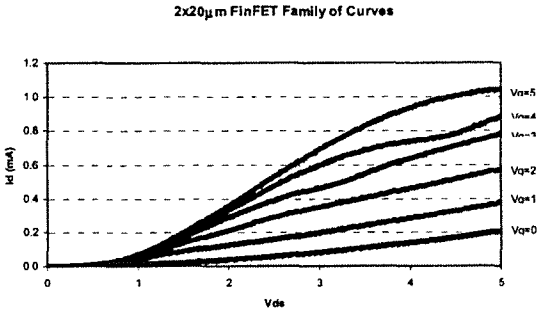

Fig 5: I_{DS}-V_{DS} characteristics for 2 x20 μm FinFET

From this plot, we see that there appears to be non-ohmic contact behavior. This is similar to results from previous work at RIT. We also see that there is a large amount of leakage current. This leakage current is due to a shunt conductance. Fig. 6 shows the schematic that shows where this is coming from where Rc is the contact resistance, Rs is the series resistance and G is the shunt conductance.

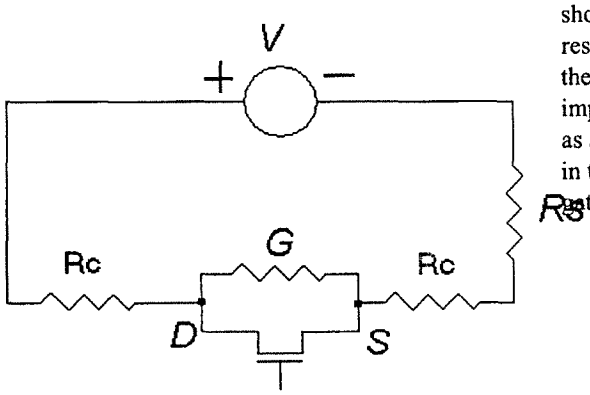

Fig. 6: Schematic of Tested Structure

The non-ideal linear-region characteristics likely come from either the long fins or from the contact resistance. The new mask design will be able to show which of these structures actually has the higher resistance. A shorter fin could result in lower series resistance. A high contact resistance could result from making contacts on the thin silicon layer. Although the deposited aluminum was saturated with silicon already, there is a chance that the long sinter helped to consume much of the shallow source drain. This could result in the high series resistance. The contact resistance could be improved by finding the optimal sintering process for thin SOI or by growing or depositing raised source drain contact areas. This could be done by growing epitaxial silicon or by depositing polysilicon. Either of these could help the problem with contacting thin source/drain regions.

The threshold voltage for these devices could not be found at low Vds because of the poor characteristic. For this reason, the threshold voltage was found at saturation. Vg was plotted against the square root of the drain current at saturation. This plot is shown for a 2x40 μm FinFET in Fig. 7. It can be seen that the V_T is approximately 1.15V. The threshold voltage ranged from about 0.9V to 1.3V for various devices.

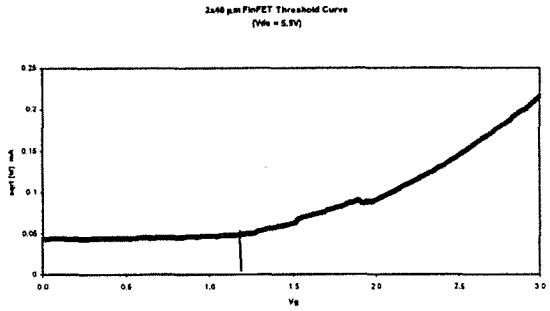

Fig 7: Threshold voltage curve for 2x40μm FinFET

The bulk-Si FinFET devices were also tested. They showed evidence of a field effect, but acted mainly as resistors. This is likely due to the lack of isolation from the bulk. Any area that was not covered by the gate was implanted n type. This caused the device to mainly act as a resistor, although the gate showed some field effect in that it allowed a shorter path of low resistance at high gate voltages.

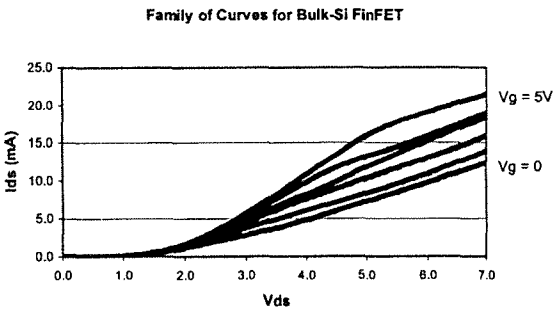

Fig. 8: I_{DS}-V_{DS} characteristics for bulk-Si FinFET

The mask design had planar devices as well as FinFETs. The planar devices were compared to the FinFETs in order to find the advantages of using FinFETs. Fig 9 shows the family of curves for a 2x40 μm FinFET. Fig. 10 shows the family of curves for a 2x40 μm planar FET.

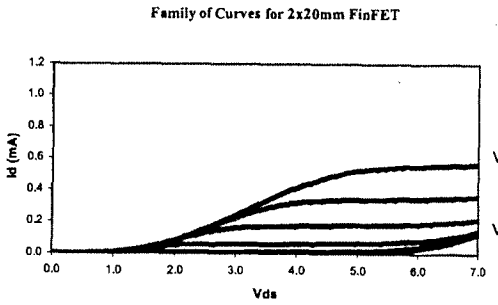

Fig. 9: I_{DS}-V_{DS} characteristics for for a 2x40 μm FinFET

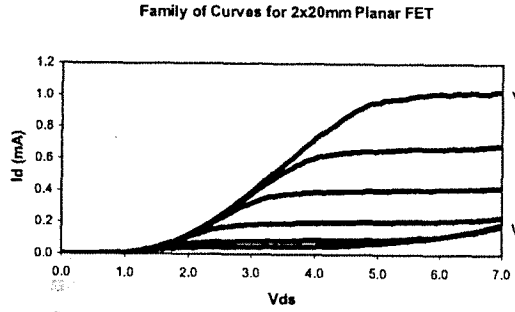

Fig. 10: I_{DS}-V_{DS} characteristics for for a 2x40 μm planar FET

From these plots, it can be seen that there is little or no difference between a planar device and a FinFET. The threshold voltage for each was ~1V. The drive current was was twice as high for the planar FET over the FinFET. This is likely explained because the 2 micron fins were actually resulted in thinner than 2 micron. This would cause the current possible to drop for these devices. The reason that there is no other difference between the two is because of the poor aspect ratio for the fins. For this device, the aspect ratio is 0.1. Better double-gate characteristics would be seen if this aspect ratio could be increased.

IV. Conlusions

In conclusion, functioning FinFETs were fabricated at RIT. A RTA process was added to the process along with processing using standard etch tools as opposed to the proprietary STS deep Si etch process previously used. These devices showed non-ohmic contact behavior and shunt conductance. The resistance is likely due to either the fin length or due to contact resistance. A mask was designed in an attempt to determine values for resistance due to both of these issues. The work done on FinFETs will help RIT realize a process at RIT that could include various ways of thinning the fin to achieve a higher aspect ratio. .

Acknowledgment

The author acknowledges Dr. Santosh Kurinec, Dr. Karl Hirschman, and Dr. Sean Rommel as advisors for this project, Jesse Siman and Chris Harvey for their previous FinFET work at RIT, and the SMFL staff for their support in keeping the SMFL running smoothly.

References

[1] Choi, Yang-Kyo et al "A Spacer Patterning Technology for Nanoscale CMOS", IEEE Transactions on Electronic Devices, Vol 49, No3, March 2002.

[2] Harvey, Christopher , "Raised Polysilicon Source/Drain FinFET Fabrication", RIT 20th Annual Microelectronics Engineering Conference, May 2002.

[3] Siman, Jesse, "Design, Fabrication, and Testing of Crystalline Silicon Source/Drain FinFETs" RIT 20th Annual Microelectronics Engineering Conference, May 2002

[4] Fossum, Jerry, "Speed Superiority of Scaled Double-Gate CMOS", IEEE Transactions on Electron Devices, Vol 49, No. 5, May 2002.

[5] Baccarani, Giorgio and Reggiani, Susanna, "A compact Double-Gate MOSFET Model Comprising Quantum-Mechanical and Nonstatic Effects", IEEE Transactions on Electron Devices, Vol 46, No. 8, August 1999.

[6] Zhang, Shengdong et al, "Implementation and Characterization of Self-Aligned Double-Gate TFT With Thin Channel and Thick Source/Drain", IEEE Transactions on Electron Devices, Vol 49, No. 5, May 2002.

[7] Kim, Keunwoo and Fossum, Jerry, "Double-Gate CMOS: Symmetrical-Versus Asymmetrical-Gate Devices", IEEE Transactions on Electron Devices, Vol 48, No. 2, February 2001.

[8] Hisamoto, Digh et al, "FinFET-A Self-Aligned Double-Gate MOSFET Scalable to 20nm" IEEE Transactions on Electron Devices, Vol 47, No. 12, December 2000.

[9] Huang, Xuejue et al, "Sub-50nm P-Channel FinFET", IEEE Transactions on Electron Devices, Vol 48, No. 5, May 2001.

[10] Chen, Qiang et al, "A Comprehensive Analytical Subthreshold Swing Model for Double-Gate MOSFETs" IEEE Transactions on Electron Devices, Vol 49, No. 6, June 2002.

[11]Pei, Gen et al, "FinFET Desin Considerations Based on 3-D Simulation and Analytical Modeling", IEEE Transactions on Electron Devices, Vol 49, No. 8, August 2002.

[12] Zhang, Rongtian and Roy, Kaushik, "Low-Power High-Performance Double-Gate Fully Depleted SOI Circuit Design", IEEE Transactions on Electron Devices, Vol 49, No. 5, May 2002.

[13] Lopez-Villanueva, Juan et al, "Effects of the Inversion-Layer Centroid on the Performance of Double-Gate MOSFETs", IEEE Transactions on Electron Devices, Vol 47, No. 1, January 2002.

[14] Auth, Christopher and Plummer, James, "A Simple Model for Threshold Voltage of Surrounding-Gate MOSFETs", IEEE Transactions on Electron Devices, Vol 45, No. 11, November 1998.

[15] "Quantum Confinement Effects in a 3D FinFET Transistor", ISE Integrated Systems Engineering ©2003

Steven D. Kirby, originally from Moatsville, WV received a B.S. in Microelectronic Engineering from the Rochester Institute of Technology in 2003. He attained co-op work at Dominion Semiconductor in Manassas, VA and Micron Technologies in Boise, ID. He will be entering the Material Science and Engineering Ph.D. program at Cornell University in the Fall of 2003.