Moving RIT to Submicron Technology:
Fabrication of 0.5μm P-Channel MOS Transistors

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Abstract— **In this investigation, efforts have been made to move the Microelectronic Engineering Program at Rochester Institute of Technology to the next technology node by developing and fabricating a 0.5μm PMOS process. Currently, RIT is fabricating 1.0μm CMOS devices. A successful 0.5μm PMOS process can be incorporated into a full flow 0.5μm CMOS process. Both process and electrical simulations were done in order to predict performance. Key process features include blanket n-well, LOCOS isolation, 15nm gate oxide, i-line lithography, self-aligned source and drain, P+ doped polysilicon gates, and shallow source and drains. A test chip was created and the fabrication process was completed. The process was unable to produce working devices. The failure mode is residual oxide in the contacts to the polysilicon gates.**

Index Terms— **Submicron Technology, PMOS, CMOS, Moore's Law,**

I. Introduction

In order to be competitive, the cost of manufacturing electronic devices needs to continually decrease. A reduction in cost is achieved by shrinking the sizes of the devices, which allows more transistors to fit on a chip and more chips to fit on a wafer. Moore's Law predicts that the number of transistors that fit onto an integrated circuit will double every 18 to 24 months. Since its inception 21 years ago, the Microelectronic Engineering program at Rochester Institute of Technology has evolved to keep pace with innovations in the semiconductor industry. The participation of students in technology development educates the critical workforce needed for the industry. Currently, RIT has the capability of manufacturing 1.0μm CMOS technology on 6" wafers. The smallest transistor made at RIT to date is 0.75μm.

In this investigation, efforts have been done to move RIT to the next technology node. The development of a 0.5μm PMOS transistor will serve as an initial feasibility study on the ability to fabricate 0.5μm technology using the facilities at RIT. A successful 0.5μm PMOS process can be incorporated into a full flow 0.5μm CMOS process.

Although advanced features are recommended, this process is simplified due to time constraints. LOCOS will be used instead of shallow trench isolation, P+ doped polysilicon gates will be used to eliminate the use of a threshold adjust implant, and shallow source-drain structures will be used without adjacent deep source-drain structures. The advanced process features are not critical for this particular study.

The design of a new test chip is required for use in the fabrication of the 0.5μm PMOS transistors. Prior to fabrication, process and electrical simulations are essential in predicting performance.

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II. Test Chip Design

A. Layout

The layout was done using Mentor Graphics IC Station. Four process layers were used to create the devices. Active is the first layer and defines the areas where the transistors will be built. The widths of the active areas define the widths of the transistors. The active area is also used to define alignment marks. The second layer, poly, defines the location for the polysilicon gates. The lengths of the poly lines define the lengths of the transistors. The smallest length in the layout is 0.5μm and the largest length is 5μm. Contact cut, the third layer, defines the areas for the contacts. This layer defines source and drain contacts to metal in the active areas and gate contacts to metal in field areas. The final layer is the metal, which is used to create both interconnects and bond pads.

The layout contains a variety of transistors with different lengths and widths. The smallest transistor has a length of 0.5μm and a width of 1.0μm. Verniers and Van der Pauw test structures were also included.

B. Mask

The test chip layout was then used to create four masks for use in the fabrication process. The mask set was made with a Perkin Elmer MEBES III for use with a Canon FPA 2000i1 i-line exposure tool.

III. Device Calculations

Calculations using device physics equations were done in order to determine threshold voltages. The selected doping levels are 4E19/cm^3 for the heavily doped P+ source and drain, and 2E17/cm^3 for the blanket N-well. The devices are designed for use with 3V technology. The device equations and the results for calculations using both P+ doped and N+ doped polysilicon gates are shown below in figures 1 and 2. The gate oxide thickness is 150A and Nss is set at 1E10/cm^3.

Bulk Potential: $\phi n = +\frac{kT}{q} Ln\left(\frac{Nd}{ni}\right)$

Work Function Difference: $\phi ms = \phi m - (\chi + \frac{Eg}{2} + \phi n)$

Flatband Voltage: $Vfb = \phi ms - \frac{qNss}{C'ox} - \frac{1}{C'ox}\int_0^{Xox} \frac{X}{Xox}\rho(x)\partial x$

Threshold Voltage: $Vt = Vfb - 2\phi n - \frac{1}{C'ox}\sqrt{4\varepsilon_s qNd(2\phi n)}$

Fig. 1. Device Physics Equations used to determine threshold voltages.

	P+ Doped Gate	N+ Doped Gate
ϕn	0.427V	0.427V
ϕms	1.016V	-0.161V
Vfb	1.009V	-0.169V
Vt	-0.879V	-2.06V

Fig. 2. Results for Threshold Voltage Calculations.

In order to prevent punch through from occurring, the depletion regions of the p-n junctions of the source and drain can't touch. An effective channel length is defined as the depletion width of the source and the depletion width of the drain subtracted from the mask length. When a maximum reverse bias voltage of 3V is applied to the source and drain, the effective channel length must be greater than half the gate length. The calculation shown below verifies that punch through will not occur for the smallest device with a mask length of 0.5μm.

$$L_{effective} = L_{mask} - 2\sqrt{\frac{2\varepsilon_s}{q}(\Psi o + Vr)(\frac{1}{Na} + \frac{1}{Nd})}$$

$$L_{effective} = 0.5 - 2*10^4\sqrt{\frac{2*8.854E-14*11.8}{1.602*10^{-19}}(1+3)(\frac{1}{2*10^{17}} + \frac{1}{4*10^{19}})} = 0.27\mu m$$

IV. Simulations

A. Process

Silvaco Supreme International Athena software package was used to simulate the process flow. Implant and thermal processes were designed in order to create the appropriate doping levels at the surface. The doping profiles of the source-drain and the well are shown in figure 3. The N-well profile was achieved by using a P31 implant at 150KeV with a dose of 1E13/cm^2 followed by a 4 hour drive in at 1025C in an N2 ambient. The junction depth of the well is 1.2μm, which is deep enough to accommodate a shallow source and drain. The source and drain profile was created using a Bf2 implant at 50KeV with a dose of 1E15/cm^2. The anneal process was done by ramping from 800 to 900C for 20minutes, soaking for 10minutes at 900C, and ramping down from 900 to 800 in 20minutes. The low temperature anneal resulted in a junction depth of 0.22μm.

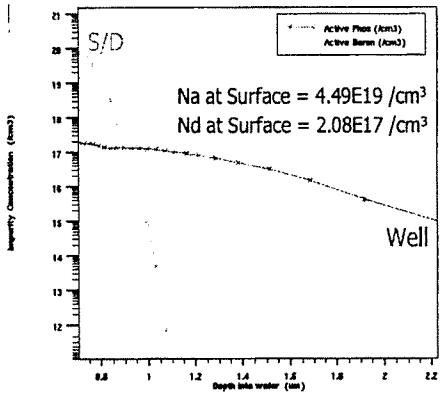

Fig. 3. Simulated impurity profiles

B. Electrical

Silvaco Supreme International Atlas software package was used to simulate the electrical performance of the process. The structure used for the simulations is shown in figure 4 with the electrodes labeled.

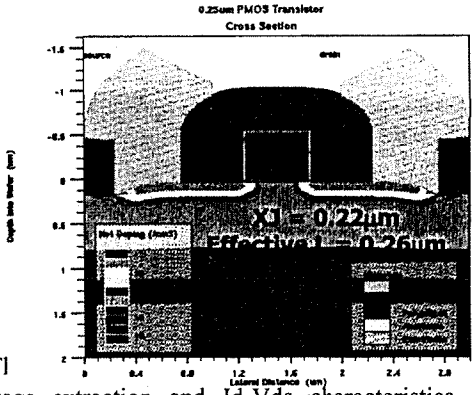

Fig. 4. Device used in electrical simulations

The threshold voltage was extracted for devices with different gate lengths in order to study the threshold voltage roll off phenomena. Simulations were done for devices with both N+ and P+ doped polysilicon gates. For the smallest device, the threshold voltage was –0.795V using a P+ doped gate and –1.872V using an N+ doped gate. Graphical results of the simulations are shown in figures 5-6.

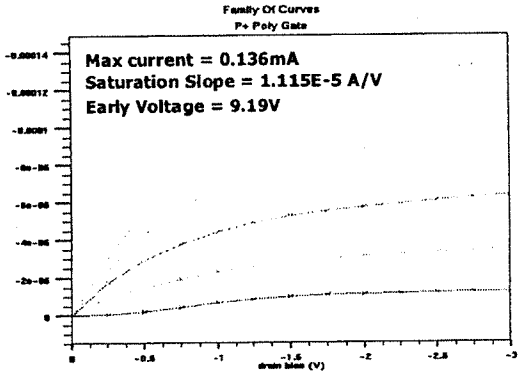

Fig. 5. Simulated Ids-Vds curves for a device with gate length = 0.5μm.

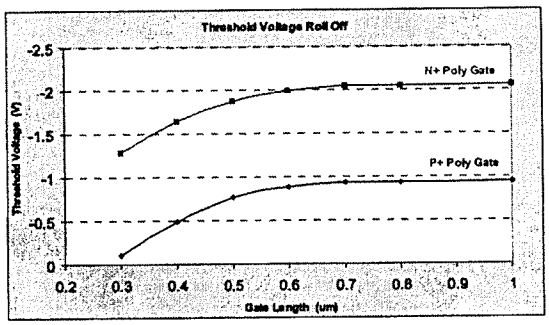

Fig. 6. Ids-Igs curves for devices with different gate lengths. The bottom curve represents the threshold voltage for devices using P+ doped polysilicon gates and the top curve shows the threshold voltage for devices with N+ doped polysilicon gates.

V. RESULTS

The fabrication process was completed. The electrical test results revealed that working transistors were not achieved. Voltage applied across the source and drain terminal resulted in no current flow. This indicates that depletion mode devices were fabricated. Until voltage is applied across the gate, the devices will not conduct. When voltage was applied across the gate, however, the devices still did not conduct.

Van der Pauw structures were also tested. The metal and source/drain structures conducted and the sheet resistances were determined. The poly gate Van der Pauw structures did not conduct. This indicates that a good connection is unable to be made to the polysilicon gates. When 30V was applied to the poly Van der Pauw structures, the oxide broke down and the devices began to conduct. The high breakdown voltage suggests that about 200 to 300A of residual oxide is located inside the gate contacts.

The exact cause of the gate contact problem is not known and is still under investigation. There are a few possibilities for the presence of residual oxide.

The contact cut etch process is the most likely cause of the residual oxide. Thermal oxide is grown for about 5 minutes during the source-drain anneal. During this 5 minutes, about 1000A is grown. This thermally grown oxide is not removed. Later in the process, low temperature oxide (LTO) is deposited over the thermally grown oxide. During the contact cut etch, the LTO and the thermally grown oxide both need be etched. The etch rate is determined using a wafer with LTO. A 15% over etch is then added to a calculated etch time. Normally, a 15% over etch is adequate. However, the thermally grown oxide etches slower than the LTO. The 15% over etch was enough to clear the source and drain contacts, but it was not able to clear the gate contacts. This indicates that more oxide was present over the polysilicon regions. Using a quick process simulation, it was revealed that heavily doped polysilicon oxidizes faster than silicon. The problem can be resolved by adding in a larger over etch, 25% to 40%, or by etching the oxide grown after anneal in a wet buffered oxide etch.

Topography differences between gate and active regions may have caused the LTO to deposit thicker over the polysilicon gates. Etching longer during the contact cut etch would solve this problem.

Another possible cause of gate contact failure is the spin on glass used to dope the polysilicon. Spin on glass containing impurities is coated over the polysilicon, baked, annealed in a furnace, and etched off in a buffered oxide etch. If the wet etch did not remove all the spin on glass, then there would be a thin layer of glass left over the gate areas. This cause is possible, but not likely, because the failure occurred with both N+ and P+ doped polysilicon gates. The chance that both processes left residual glass over the polysilicon is low.

TABLE I SHEET RESISTANCE RESULTS DETERMINED USING VAN DER PAUW STRUCTURES

$$Rs = \frac{\pi}{Ln(2)} * \frac{\partial V}{\partial I}$$

$$Rs(metal) = 51.5ohm/sq$$

$$Rs(S/D) = 82.2ohm/sq$$

VI. FUTURE WORK

Additional work needs to be done to improve the 0.5μm PMOS process. A 0.5μm NMOS process also needs to be developed. In the future, successful 0.5μm PMOS and NMOS processes can be integrated into a 0.5μm CMOS process with STI, silicide, and dual-doped polysilicon gates.

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