SPICE Parameter Extraction from Simulations and Experimental Data

Robert L. Saxer Jr.

Abstract—**SPICE parameters are a valuable tool used in the designing of integrated circuits. SPICE parameters communicate device behavior to circuit simulators. The purchase and support of Silvaco's UTMOST software provided the function of extracting SPICE parameters from devices at RIT. With this new capability, RIT can obtain new levels of circuit simulation accuracy before fabrication. A method of SPICE parameter extraction was created and documented for simulated and experimental data.**

Index Terms— **BSIM3, Parameter extraction, SPICE, UTMOST.**

I. Introduction

IN the production and development of modern integrated circuits, SPICE parameters are an important link between circuit designers and process technology. Accurate SPICE parameters loaded into simulation software provide an essential tool to test the functionality and performance of circuit designs. Increased model accuracy reduces the possibility of critical errors and costly manufacturing iterations. SPICE models are extracted from both physical devices, and simulated devices. In the latter case, process designers using process simulation can create simulated devices, which are used to extract parameters. If the process simulation contains the required accuracy, the extracted SPICE models can be passed to circuit designers. Using this method, the circuit designers can update device models and modify their designs before the physical process is initiated in the lab.

The objective of this investigation was to develop a process of parameter extraction at RIT. To achieve the desired accuracy, use of the higher-level SPICE models was desired. The UTMOST parameter extraction program by Silvaco International was utilized as it can output and convert between many different levels and versions of SPICE parameters. It was necessary to develop an understanding of the extraction routines, and strategy to complete this work.

Using the UTMOST software, methods of parameter extraction have been documented; specifically a process of extracting parameters was developed for both electrical simulation results and electrical measurements taken on RIT fabricated devices.

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II. Background

What is SPICE?

SPICE or Simulation Program with Integrated Circuit Emphasis, simulators predict the electrical characteristics of circuit elements. The simulator is used to determine how a complex circuit will respond to applied bias. SPICE requires a circuit schematic and circuit element models as inputs, and provides a simulated circuit response as the output. The elements in a circuit may include resistors, capacitors, inductors, diodes, field effect transistors, bipolar junction transistors, transmission lines, voltage sources, and current sources. Each of these circuit elements is described by a list of SPICE parameters. It is necessary to have accurate parameters for accurate SPICE simulations. This project focused on parameter extraction from MOS transistors.

Methods of simulating circuit elements include physically based simulators such as ATLAS by SILVACO, that use differential equations derived from Maxwell's laws. These simulators take in specific biasing conditions, a device structure, like that of a MOSFET, and solve for the carriers in the structure. Electrical performance is determined by simulating carrier movement through the structure. Physical simulators are highly accurate when the appropriate physics is programmed in. The simulators are very useful for investigating single devices, but are not generally used for circuit analysis. This is due to the complex computing required to solve the multi-dimensional differential equations.

SPICE solves for current and voltages at each node in a circuit similar to a student solving nodal and mesh analysis in an undergraduate Electrical Engineering Circuits class. Time is treated as the independent variable in SPICE circuit simulations. The response of

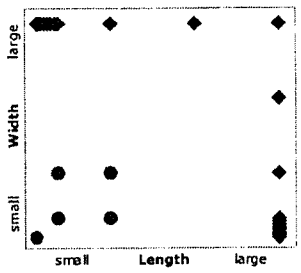

Fig. 1. Extraction geometries. The diamond ◆ points indicate geometries suitable for extraction. The circle ● geometries are useful as model verification points.

capacitors, the charge up and discharge effects are also fitted to model equations, for use in SPICE. Transistors require an additional amount of complexity in their associated models.

SPICE History

SPICE was originally developed by the University of California, Berkeley in 1972. The original SPICE levels 1,2, and 3 were derived straight from undergraduate device physics text books. These SPICE models were strongly tied to physical meaning. However, the mathematical implementation of these models was poor, and the SPICE simulators had convergence problems with these first models.

The Berkeley Short-channel Insulated gate field effect transistor Model (BSIM) was created to improve mathematical implementation and thus simulation convergence. While the BSIM and BSIM2 models did fit accurately and simulate well, they lacked physical meaning. A model containing good physical meaning is easier to extract parameters than a model without physical meaning. Parameters with physical meaning can be extracted by isolating a geometry or electrical bias. Purely empirical parameters are determined with curve fitting algorithms.

BSIM3 offers an improvement in physical meaning. BSIM3 uses a single equation to define operation over all bias conditions. This improves the continuity of I-V and C-V curves. The BSIM3 model is made up of 185 parameters that describe the functionality of a MOSFET manufactured with a certain process technology. Due to its accuracy, the BSIM3 SPICE model was chosen for extraction in this project.

UTMOST

UTMOST stands for Universal Transistor Modeling SofTware. UTMOST is a data acquisition and parameter extraction tool that can easily and quickly create accurate SPICE parameter models. This software can extract parameters from both simulated and physical devices. UTMOST interacts with other SILVACO software, and can control a variety of test equipment including automated probe stations and parameter analyzers.

xtraction and Requirements

MOSFET SPICE models can be broken down along ometric and bias conditions. Parameters can be tracted by isolating these effects using methods milar to a full factorial designed experiment. The neral requirements for extracting a MOSFET model e as follows. The devices are to be biased in all gions. Bias dependent parameters are extracted by alyzing and curve fitting each geometry device in the llowing regions; the subthreshold region, the linear gion, and the saturation region. For extraction of bulk effects, it is essential to have four terminal MOSFET devices; gate, source, drain, and substrate (or well) terminals. The necessary geometries required for extraction are a large length and large width device, large length devices of varying width, and large width devices of varying length. The desired geometries are shown graphically in Fig. 1. Large length and large width devices are used for extraction of the root SPICE model. The other sets allow length and width effects to be decoupled. Layout of the desired geometries with 4 terminals each allows accurate BSIM3 model extraction.

Extraction in a New Technology Development Mode

SPICE parameters are necessary for the development of new integrated circuits (IC). When developing an entirely new process flow, new IC parameters need to be made available for circuit designers.

By using a physical based simulator during development, a starting SPICE model can be obtained for circuit simulation. This approach fits nicely into the process of technology development. During the

development of a new technology, physical based modeling is used to develop a process that gives the desired results. ATHENA by SILVACO can *virtually* take a wafer from starting substrate to metallization. Once a complete device is constructed on the computer, the device can be electrically simulated using ATLAS. The use of CAD tools greatly reduces cost and time, compared to exclusively developing a new technology in the cleanroom.

Development starts with the simulation of processes, and an entire device. The process flow is then modified until the device demonstrates the desired electrical characteristics. Once this is achieved, devices are simulated with geometries suitable for extraction. These devices are 'electrically tested' and the results are used for parameter extraction. By making SPICE parameters available at this early stage, the work of developing the technology into a manufacturable process can occur in parallel with circuit development and test.

Model Verification from Fabricated Devices

Once a manufacturable process is obtained, parameter extraction can be repeated with real devices. For real devices, the structure is created in the cleanroom, and the electrical data is taken using a parameter analyzer. A parameter analyzer will provide DC data for extraction. Capacitance and high frequency parameters are also necessary for a complete SPICE model. These parameters can be extracted by using C-V meters and high frequency analyzers in a manner similar to DC testing.

III. Motivation

Parameter extraction is an enabling capability. It enables the Microelectronic Engineering department to provide circuit designers with accurate SPICE models.

SPICE parameters extracted from the RIT Subμ CMOS [1] or the RIT Strongarm [2] CMOS processes are valuable in the design and development of complex circuits. By using SPICE parameters extracted from RIT processes, the circuit simulation should provide a reasonable match to the manufactured result.

IV. Procedure

Extraction from Simulated Devices

The Strongarm CMOS process simulation developed in EMCR604/704 [3] was used as a starting point. The "Semiconductor Process & Device Modeling" class provides a study into the use of physical simulation to model complex processes and electrical operation.

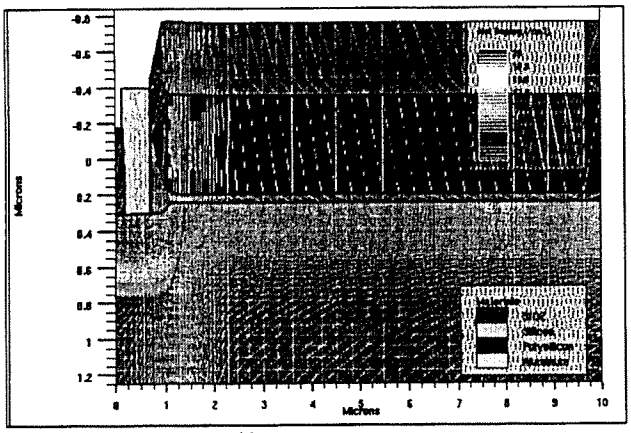

Fig. 2. ATHENA process grid.

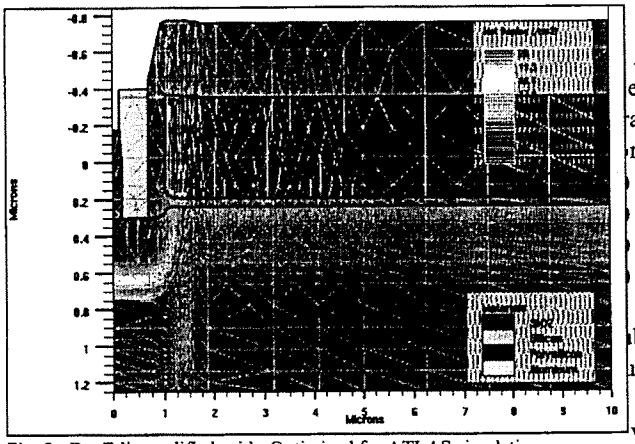

Fig. 3. DevEdit modified grid. Optimized for ATLAS simulation

The grid created by the initial ATHENA Strongarm simulation was not optimum for ATLAS simulation. DevEdit was used to reduce the number of nodes, and the number of obtuse triangles. Fig. 2 and Fig. 3 show the device before and after the regrid operation. Although it is outside the scope of this project, it is important to note that more accurate ATHENA simulation results would have been obtained if extra node points had been placed in the gate oxide and polysilicon.

An ATHENA routine was then created that modifies the starting structure into a full MOSFET of the appropriate length. The ATHENA routine takes the starting structure file, mirrors it on the right, cuts the resulting structure to half the desired length, and mirrors again on the right side. This method checks the critical dimension of the channel length and uses variables to return a device of the exact channel length specified. This ATHENA routine was repeated 14 times in a simulation file to produce structures of 14 different lengths from the starting structure file.

TABLE I
GEOMETRIES USED FOR EXTRACTION

	Width	Length
1)	1 µm	20 µm
2)	1 µm	15 µm
3)	1 µm	12 µm
4)	1 µm	10 µm
5)	1 µm	8.0 µm
6)	1 µm	6.0 µm
7)	1 µm	5.0 µm
8)	1 µm	4.0 µm
9)	1 µm	3.0 µm
10)	1 µm	2.5 µm
11)	1 µm	2.0 µm
12)	1 µm	1.7 µm
13)	1 µm	1.6 µm
14)	1 µm	1.5 µm

An ATLAS simulation was then created to perform e necessary electrical simulations. Four drain current aphs are required for extraction of BSIM3 parameters, r each device geometry.

- IDS vs VGS stepping VBS, with a low VDS
- IDS vs VDS stepping VGS, with a low VBS
- IDS vs VGS stepping VBS, with a high VDS
- IDS vs VDS stepping VGS, with a high VBS

Graph 1 was used by UTMOST to extract linear and bthreshold region parameters. Saturation region tput conductance parameters were extracted in Graph In Graph 3, subthreshold conductance parameters are vestigated. Graph 4 permits extraction of KETA, a SIM3 bulk effect parameter.

Many bias points were necessary for suitable accuracy in UTMOST extraction. This was due to the number of points per curve, and the quantity of different geometries. To handle such a large quantity of physical electrical simulations (bias points > 14300) a fast computer was required. A Linux workstation was outfitted with dual AMD ATHLON MP-2600+ processors and 2 gigabytes of random access memory. The station was essential for running the thousands of lines of simulation code for several reasons.

1) This system did not stop mid simulation, compared to the previous computers.
2) This system provided quick simulation turnaround time. For example, if a line of simulation code contains a syntax error, it is quickly arrived upon. The pure speed of the system increased the pace of troubleshooting.

The UTMOST interactive software was then used to create a template logfile. The template logfile serves as a vehicle for transporting external data into the parameter extractor and contains the appropriate headers describing bias information.

Batch mode UTMOST (using DECKBUILD) was used to convert the ATLAS electrical data into an UTMOST logfile format. Once in the correct format,

the data was manually moved into the template logfile under the appropriate headers.

The completed template logfile was ready for extraction. Extraction of the BSIM3 model is simple at this point. Parameters: TOX (oxide thickness), XJ (source/drain junction depth), NCH (channel doping), and NSUB (substrate or well doping) taken from the ATHENA TONYPLOT were loaded manually into the SPICE parameter file. TOX had to be loaded into UTMOST, since no CV measurements were made from which to extract oxide thickness. TOX is critical in many of the extraction algorithm. Manually loading XJ, NCH, and NSUB provide an accurate starting point for the BSIM3 extraction routine.

Next the logfile was loaded and the extraction routine run. Immediately after extracting the parameters, a comparison between the data and the model was shown for each bias region, and each geometry. Then the parameters were automatically placed in the parameter file.

If the results show good match up, then the process is complete. If the model does not fit, then UTMOST contains a number of optimization options. Figures 4-9 show the model fit, for a single geometry over all useful bias conditions.

Width effects were neglected in the extraction of simulated Strongarm CMOS BSIM3 models. ATHENA is incapable at creating three-dimensional structures. ATLAS does have the capability of creating and measuring three-dimensional structures. However, structures created in ATLAS are not the physically simulated structures like those made in ATHENA. For this project, it was desirable to understand how to extract parameters from realistic simulations. Therefore, the Author decided that the width term should be neglected.

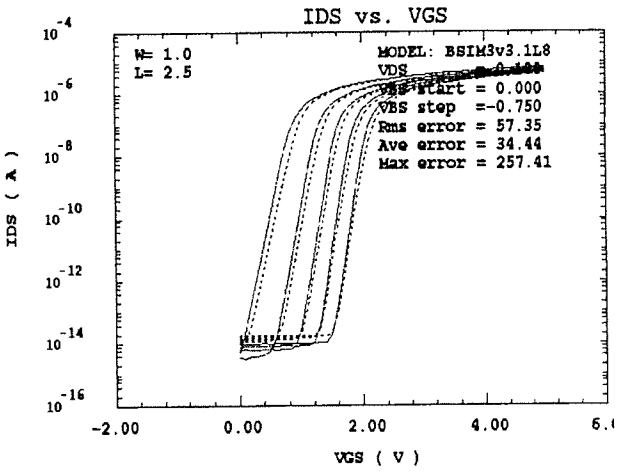

Fig. 4. Subthreshold bias conditions. VDS in the Linear region. Log scale

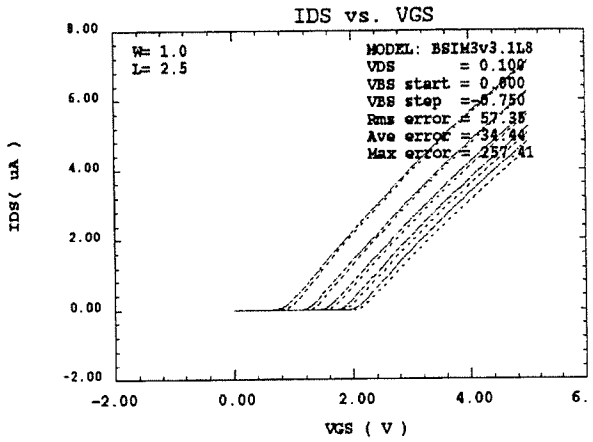

Fig. 5. IDS vs VGS. VDS in the Linear region. Linear Scale

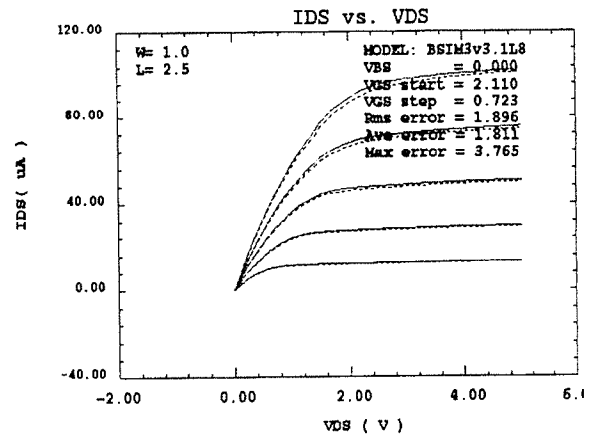

Fig. 6. Linear and Saturation bias regions. Low VBS.

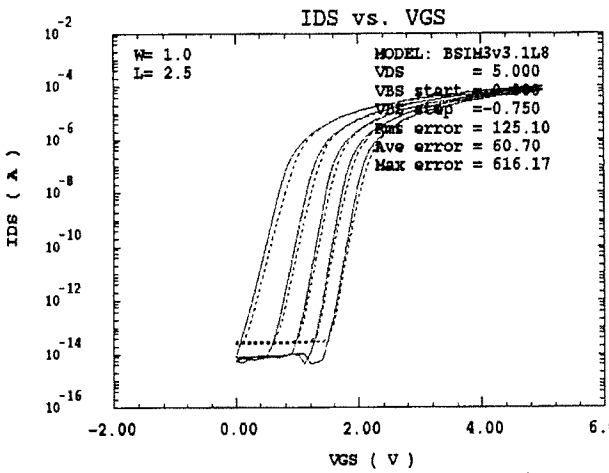

Fig. 7. Subthreshold bias conditions. VDS in saturation. Log scale

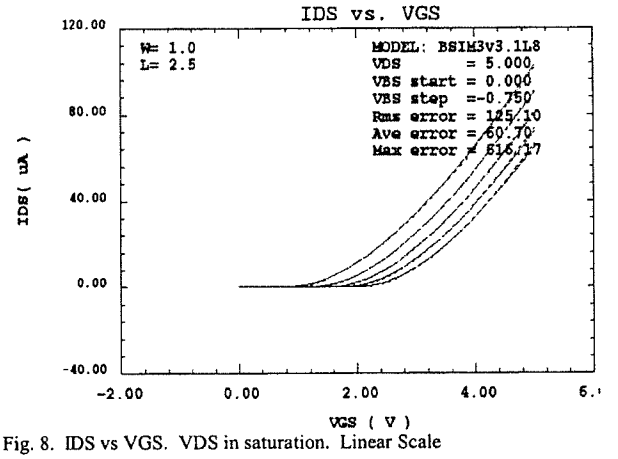

Fig. 8. IDS vs VGS. VDS in saturation. Linear Scale

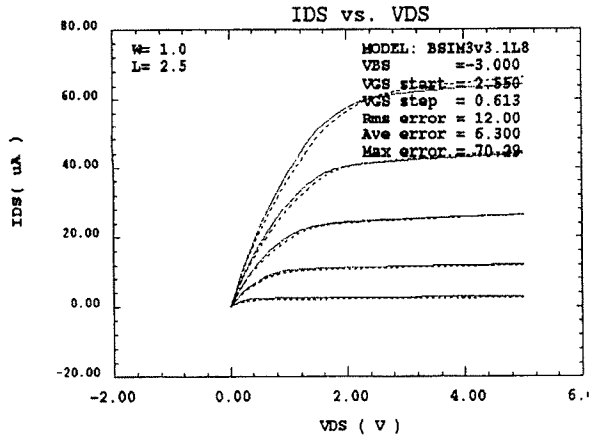

Fig. 9. Linear and Saturation bias regions. High VBS.

Extraction from Fabricated Devices

Extraction from fabricated devices was straightforward once all the necessary connections were in place. As listed previously, devices of the appropriate geometry need to be present as test ructures. In addition, each test device is required to be four terminal device.

A National Instruments GPIB-232CT-A serial to PIB converter box was obtained, along with a null odem serial cable. With these connections, it was ɔssible for the HP4145 to communicate with the TMOST software.

The HP4145 probes were connected to the device ıder test (DUT), and UTMOST was set to measure and ctract. UTMOST then told the HP4145 to bias the ɔvice, as the setup required, and query for the next ɔvice hookup. While measuring each device, the sults were shown on the workstation. If the final ımmary of results showed good match up, then the ocess was complete. If not, then the parameters could ɔ optimized. Note that no further measurements ɔeded to be taken for optimization. UTMOST used the ıta or subsets of the data already taken to perform ɔtimization.

Although the intent was to extract SPICE parameters om fabricated devices, accurate models were not eated. Communication between the extraction ıgineer and layout engineer did not occur early enough request four terminal devices, and appropriate ɔometries.

V. Conclusion

A method of parameter extraction from both ɔperimental and simulated devices has been realized ıd documentation has been created. The simulated rongarm CMOS process was used for BSIM3 spice ırameter extraction and the resulting model matched e original data. The full BSIM3 model is shown in ppendix 1. A BSIM3 model was also extracted for a aled version of the Strongarm CMOS process. The sults also looked very good and the model is located in ppendix 2.

The UTMOST software is capable of controlling and ɔtracting parameters from other commonly used easurement equipment. The methods learned and mple instruction manual created will be easily ɔpandable into the extraction of high frequency, and ıpacitance – voltage related parameters.

Appendix

Simulated Strongarm CMOS

DEVICE PARAMETER LISTING
SPICE: SmartSpice
MODEL: BSIM3v3.1L8

NAME	OPTIMIZED	UNIT
1[LEVEL]	8	

2[VERSION]	3.1		56[PDIBLCB]	0	V^-1.0
3[TNOM]	27	degreesC	57[DROUT]	0.1342	-
4[TOX]	4.40E-08	m	58[PSCBE1]	3.20E+09	V/m
5[XJ]	4.80E-07	m	59[PSCBE2]	3.13E-08	V/m
6[NCH]	2.94E+16	cm^-3	60[PVAG]	0	-
7[NSUB]	7.40E+15	cm^-3	61[DELTA]	0.01	V
8[VTH0]	0.8865	V	62[NGATE]		cm^-3
9[K1]	1.246	V^0.5	63[ALPHA0]		m/V
10[K2]	-0.0309	-	64[BETA0]		V
11[K3]	0	-	65[ALPHA1]		1/V
12[K3B]	0	V^-1.0	66[IIRAT]		
13[W0]	2.50E-06	m	67[GEO]		
14[NLX]	2.00E-08	m	68[RSH]		ohm/square
15[DVT0W]	0	m^-1.0	69[RD]		ohm/square
16[DVT1W]	0	m^-1.0	70[RS]		ohm/square
17[DVT2W]	-0.032	V^-1.0	71[RDC]		ohm/square
18[DVT0]	2	-	72[RSC]		ohm/square
19[DVT1]	0.4731	-	73[NDS]		
20[DVT2]	0.0422	V^-1.0	74[VNDS]		V
21[VBM]		V	75[LD]		m
22[U0]	832.97	cm^2.0/Vs	76[WD]		m
23[UA]	3.70E-09	m/V	77[ACM]		m
24[UB]	-6.50E-18	(m/V)^2	78[LDIF]		m
25[UC]	-1.83E-10	V^-1.0	79[HDIF]		m
26[VSAT]	1.47E+05	m/sec	80[N]		m
27[A0]	0.5295	-	81[JS]		A/m^2
28[AGS]	0	V^-1.0	82[JSW]		A/m
29[B0]	0	m	83[IS]		A
30[B1]	0	m	84[MOBMOD]	1	-
31[KETA]	-0.0722	V^-1.0	85[TEMPMOD]		-
32[A1]	0	V^-1.0	86[PRT]	0	ohm*um/C
33[A2]	1	-	87[UTE]	-1.5	-
34[RDSW]	569.99	ohm*um^WR	88[KT1]	0	V
35[PRWG]	0	V^-1.0	89[KT1L]	0	V*m
36[PRWB]	0	V^-.5	90[KT2]	0	-
37[WR]	1	-	91[UA1]	4.30E-09	m/V
38[WINT]	2.14E-08	m	92[UB1]	-7.60E-18	(m/V)^2
39[LINT]	1.17E-08	m	93[UC1]	-5.60E-11	V^-1.0
40[XL]	0	m	94[AT]	3.30E+04	m/sec
41[XW]	0	m	95[VFB]		V
42[DWG]	0	m/V	96[PHI]		V
43[DWB]	0	m/V^0.5	97[GAMMA1]		V^0.5
44[VOFF]	-0.0952	V	98[GAMMA2]		V^0.5
45[NFACTOR]	1.128	-	99[VBX]		V
46[CIT]	0	F/m^2	100[XT]		m
47[CDSC]	2.42E-05	F/m^2	101[VBI]		V
48[CDSCD]	0	F/Vm^2	102[NQSMOD]	0	-
49[CDSCB]	0	F/Vm^2	103[ELM]		-
50[ETA0]	0	-	104[WL]	0	m^WLN
51[ETAB]	0	V^-1.0	105[WLN]	1	-
52[DSUB]	0.0341	-	106[WW]	0	m^WWN
53[PCLM]	1.395	-	107[WWN]	1	-
54[PDIBLC1]	0.0489	-	108[WWL]	0	m^WWN+WLN
55[PDIBLC2]	1.00E-05	-	109[LL]	0	m^LLN

110[LLN]	1	-
111[LW]	0	m^LWN
112[LWN]	1	-
113[LWL]	0	m^LWN+LLN
114[NLEV]		
115[AF]		
116[KF]		
117[NOIMOD]		
118[NOIA]		-
119[NOIB]		-
120[NOIC]		-
121[EM]		V/m
122[EF]		V/m
123[CAPMOD]	2	-
124[INTCAP]		-
125[VFBCV]		-
126[CJpar]	0	F
127[CJSWpar]	0	F
128[XPART]	0	
129[CGDO]		F/m
130[CGSO]		F/m
131[CGBO]		F/m
132[FC]		F/m
133[CJ]		
134[PB]		
135[MJ]		
136[CJSW]		F/m
137[PBSW]		F/m
138[MJSW]		
139[CJSWG]		
140[PBSWG]		
141[MJSWG]		
142[CBD]		F
143[CBS]		F
144[JCAP]		
145[TEMPLEV]		
146[TEMPLEVC]		
147[EG]		e/V
148[GAP1]		eV/K
149[GAP2]		K
150[XT1]		
151[TCJ]		1/K
152[TPB]		
153[TMJ1]		1/K
154[TMJ2]		1/K^2
155[TCJSW]		1/K
156[TPBSW]		V/K
157[TMJSW1]		1/K
158[TMJSW2]		1/K^2
159[TTT1]		1/K
160[TTT2]		1/K^2
161[TRD1]		1/K
162[TRD2]		1/K^2
163[TRS]		1/K
164[TRS2]		1/K^2
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166[CGDL]		
167[CKAPPA]		
168[CF]		
169[CLC]		
170[CLE]		
171[DLC]	0	
172[DWC]	0	
173[WMIN]		
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176[LMAX]		
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179[NLIM]		
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183[BINUNIT]		
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185[DELVTO]		V

2. Simulated Strongarm CMOS [Scalled]

DEVICE PARAMETER LISTING
SPICE: SmartSpice
MODEL: BSIM3v3.1L8

NAME	OPTIMIZED	UNIT
1[LEVEL]	8	
2[VERSION]	3.1	
3[TNOM]	27	degreesC
4[TOX]	2.00E-08	m
5[XJ]	3.50E-07	m
6[NCH]	1.38E+17	cm^-3
7[NSUB]	3.30E+16	cm^-3
8[VTH0]	0.9096	V
9[K1]	1.184	V^0.5
10[K2]	-0.00783	-
11[K3]	0	-
12[K3B]	0	V^-1.0
13[W0]	2.50E-06	m
14[NLX]	2.19E-08	m
15[DVT0W]	0	m^-1.0
16[DVT1W]	0	m^-1.0
17[DVT2W]	-0.032	V^-1.0
18[DVT0]	2	-
19[DVT1]	0.2247	-
20[DVT2]	0.0877	V^-1.0
21[VBM]		V
22[U0]	625.72	cm^2.0/Vs
23[UA]	1.64E-09	m/V
24[UB]	-8.70E-19	(m/V)^2

25[UC]	-7.80E-11	V^-1.0	79[HDIF]		m
26[VSAT]	1.07E+05	m/sec	80[N]		m
27[A0]	0.4529	-	81[JS]		A/m^2
28[AGS]	0	V^-1.0	82[JSW]		A/m
29[B0]	0	m	83[IS]		A
30[B1]	0	m	84[MOBMOD]	1	-
31[KETA]	-0.0422	V^-1.0	85[TEMPMOD]		-
32[A1]	0	V^-1.0	86[PRT]	0	ohm*um/C
33[A2]	1	-	87[UTE]	-1.5	-
34[RDSW]	686.14	ohm*um^WR	88[KT1]	0	V
35[PRWG]	0	V^-1.0	89[KT1L]	0	V*m
36[PRWB]	0	V^-.5	90[KT2]	0	-
37[WR]	1	-	91[UA1]	4.30E-09	m/V
38[WINT]	5.40E-08	m	92[UB1]	-7.60E-18	(m/V)^2
39[LINT]	6.70E-08	m	93[UC1]	-5.60E-11	V^-1.0
40[XL]	0	m	94[AT]	3.30E+04	m/sec
41[XW]	0	m	95[VFB]		V
42[DWG]	0	m/V	96[PHI]		V
43[DWB]	0	m/V^0.5	97[GAMMA1]		V^0.5
44[VOFF]	-0.1031	V	98[GAMMA2]		V^0.5
45[NFACTOR]	1.035	-	99[VBX]		V
46[CIT]	0	F/m^2	100[XT]		m
47[CDSC]	-2.69E-04	F/m^2	101[VBI]		V
48[CDSCD]	0	F/Vm^2	102[NQSMOD]	0	-
49[CDSCB]	0	F/Vm^2	103[ELM]		-
50[ETA0]	0	-	104[WL]	0	m^WLN
51[ETAB]	0	V^-1.0	105[WLN]	1	-
52[DSUB]	0.0706	-	106[WW]	0	m^WWN
53[PCLM]	0.9076	-	107[WWN]	1	-
54[PDIBLC1]	0.00496	-	108[WWL]	0	m^WWN+WLN
55[PDIBLC2]	8.30E-04	-	109[LL]	0	m^LLN
56[PDIBLCB]	0	V^-1.0	110[LLN]	1	-
57[DROUT]	0.0706	-	111[LW]	0	m^LWN
58[PSCBE1]	5.50E+09	V/m	112[LWN]	1	-
59[PSCBE2]	2.97E-08	V/m	113[LWL]	0	m^LWN+LLN
60[PVAG]	0	-	114[NLEV]		
61[DELTA]	0.01	V	115[AF]		
62[NGATE]		cm^-3	116[KF]		
63[ALPHA0]		m/V	117[NOIMOD]		
64[BETA0]		V	118[NOIA]		-
65[ALPHA1]		1/V	119[NOIB]		-
66[IIRAT]			120[NOIC]		-
67[GEO]			121[EM]		V/m
68[RSH]		ohm/square	122[EF]		V/m
69[RD]		ohm/square	123[CAPMOD]	2	-
70[RS]		ohm/square	124[INTCAP]		-
71[RDC]		ohm/square	125[VFBCV]		-
72[RSC]		ohm/square	126[CJpar]	0	F
73[NDS]			127[CJSWpar]	0	F
74[VNDS]		V	128[XPART]	0	
75[LD]		m	129[CGDO]		F/m
76[WD]		m	130[CGSO]		F/m
77[ACM]		m	131[CGBO]		F/m
78[LDIF]		m	132[FC]		F/m

133[CJ]		
134[PB]		
135[MJ]		
136[CJSW]		F/m
137[PBSW]		F/m
138[MJSW]		
139[CJSWG]		
140[PBSWG]		
141[MJSWG]		
142[CBD]		F
143[CBS]		F
144[JCAP]		
145[TEMPLEV]		
146[TEMPLEVC]		
147[EG]		e/V
148[GAP1]		eV/K
149[GAP2]		K
150[XT1]		
151[TCJ]		1/K
152[TPB]		
153[TMJ1]		1/K
154[TMJ2]		1/K^2
155[TCJSW]		1/K
156[TPBSW]		V/K
157[TMJSW1]		1/K
158[TMJSW2]		1/K^2
159[TTT1]		1/K
160[TTT2]		1/K^2
161[TRD1]		1/K
162[TRD2]		1/K^2
163[TRS]		1/K
164[TRS2]		1/K^2
165[CGSL]		
166[CGDL]		
167[CKAPPA]		
168[CF]		
169[CLC]		
170[CLE]		
171[DLC]	0	
172[DWC]	0	
173[WMIN]		
174[WMAX]		
175[LMIN]		
176[LMAX]		
177[SMOOTH]		
178[ABULKLIM]		
179[NLIM]		
180[LAMBLIM]		
181[UEFFLIM]		
182[PARAMCHK]		
183[BINUNIT]		
184[BERK]		
185[DELVTO]		V

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