Process Design, Development, Fabrication and Verification of a CMOS Technology for RIT

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Abstract – **The motivation in creation of the Strongarm process flow was to create a robust "enabling" process that was easy to manufacture. Optimum process conditions have been determined through extensive SUPREM simulation. Electrical examination using ATLAS software allowed for parameter extraction of the computer-generated devices. Modeling the extracted parameters with standard device physics equations allowed for a SPICE level-2 analysis that could be verified through electrical testing of actual fabricated devices. The technology was designed for a two micron, twin-well process incorporating a 40nm gate oxide and an N+ poly gate. Source and drain implants are at 2E15 cm^{-2}, and a unique NMOS V_T adjustment is used that occurs during channel stop implant. The manufacturability of the technology was observed through the successful fabrication and verification of two initial lots in the Rochester Institute of Technology (RIT) Semiconductor and Microsystems Fabrication Laboratory (SMFL).**

Index Terms—**Strongarm Process, CMOS, Process Development, Silvaco, Athena, Atlas, Terada-Muta, RITD.**

I. INTRODUCTION

Modern CMOS processes are fine tuned to exact process flows and specifications. Process simulation software can help predict the outcome of a fabricated integrated circuit technology, yet falls short if not validated with actual fabrication and parameter verification. The goal is to create a technology that works within a toolset's process capability and produces good results. Working devices can be fabricated if a sound robust process is used and care is taken to meet the process specifications.

The objective of this investigation was to develop a new CMOS technology (referred to as the Strongarm process) with a focus on ease of manufacturability and ability to verify the operating parameters of the constructed devices. The process was designed for robustness due to the varying conditions present in the academic environment of the RIT SMFL. Due to the expensive nature of processing integrated circuits, extensive simulation was done to not only improve process latitude, but also provide a background into the inner workings and process sensitivities inherent in the technology.

Manuscript received May 21, 2003. This work was supported in part by the Rochester Institute of Technology, Department of Microelectronic Engineering.

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II. MOTIVATION

RIT is in a position to offer a unique opportunity to students of not only Microelectronic Engineering, but also across disciplines, including Electrical and Computer Engineering. A strong and stable integrated circuit manufacturing process will support collaboration between departments, in which the Microelectronic Engineering department can fabricate designed circuits and provide SPICE models for circuit designers.

At the forefront of this initiative is the manufacturing process and its abilities. A worthwhile process has a great need for robustness. The academic environment present at RIT focuses on education and learning, and cannot operate with the strict tolerances that industry manufacturing environments adhere to. As such the processes run in the SMFL need to be tolerant of tool variances and processing fluctuations.

At the same time, ease of manufacturability needs to be attended to. With the premise that many students would be manufacturing using the Strongarm process it had to be easy to fabricate working devices using it. Unorthodox processing techniques and complicated steps would surely lead to failures.

Once well established, the Strongarm process is intended to act as an "enabling" technology. The desire is to have advanced devices integrated alongside CMOS circuits. Quantum devices such as tunneling diodes, micro-electrical mechanical systems (MEMS) and bipolar technology can be constructed together with a CMOS technology that will hold up to various processing conditions.

III. DEVELOPMENT

RIT currently has multiple process flows, including a twin-well submicron CMOS process [1]. The current process is fabricated in EMCR650 Factory class and suffers from a non-ideal manufacturing environment. Multiple students over multiple lab sessions process lots a process step at a time. Understandably students mis-process wafers, not only being unfamiliar with the manufacturing equipment, but also by not being able to

know the exact conditions and results from previous steps. Not only does care need to be taken to meet the process specifications, but a robust process must be used to create working devices. While the current factory class is an excellent learning opportunity, it is not an ideal environment to fabricate devices for the initiative that is proposed.

The Strongarm process is a variation on past and present CMOS processes at RIT, including methods from RIT n-well, p-well and twin-well processes and other process flows [2]. It began as a class development project for EMCR604/704 Semiconductor Process and Device Modeling [3], and as such it has seen extensive process simulation and device modeling.

A. Process Flow

The Strongarm process is defined as follows:

- Scribe, 4pt Probe, RCA Clean
- Pad-Ox1 - 20min ramp to 1000°C in $DryO_2$, 22min $DryO_2$ w/TLC, 5min $DryO_2$ soak, 20min N_2 Purge, 30min ramp down in N_2
- Nitride1 is flexible with thickness
- Lithography Level1 is N-well
- N-well implant uses Pad-Ox1 as screen

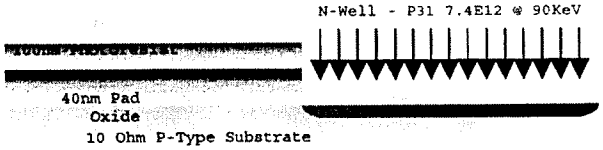

Figure 1: Representative Cross-section through N-Well Implant

- Resist Strip, RCA Clean
- Locos1 - 10min Ramp to 950°C in $DryO_2$, 120min soak $WetO_2$, 20min N_2 Purge, 30min Ramp Down in N_2
- Oxynitride strip - 30sec in BOE
- Nitride strip in Hot Phosphoric Acid
- P-well implant through PadOx1

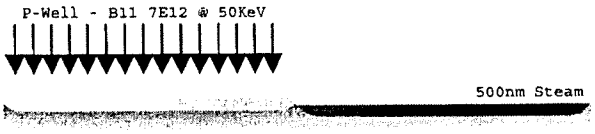

Figure 2: Representative Cross-section through P-Well Implant

- Well Drive - 20min ramp to 1100°C N_2, 60min stabilization in N_2, 360min (6hr) $DryO_2$ Purge, 2280min (38hr) Soak in N_2, 30min Ramp in N_2
- Temperature stays below 1100°C to allow 6in processing

Figure 3: Representative Cross-section through Well Drive - In

- Oxide Etch – 10min in BOE
- Pad-Ox2 - Same recipe as Pad-Ox1
- Nitride2 is critical layer - Thin to allow Channel Stop implant to pass into Nfet active region
- Lithography Level2 is Active Mask
- Resist Strip, Lithography Level3 is Channel Stop (Reverse N-well mask)
- Channel stop implant acts as Nfet VT adjust

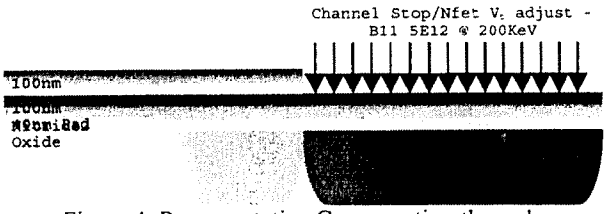

Figure 4: Representative Cross-section through Channel Stop Implant

- Resist Strip, RCA Clean
- Locos2 - 15min ramp to 950°C in $DryO_2$, 300min soak in $WetO_2$, 5min $DryO_2$ purge, 20min N_2 purge, 20min ramp down in N_2
- Nitride Strip in Hot Phosphoric, 1min Oxide etch in BOE
- Kooi Oxide - 10 min ramp to 900°C in $DryO_2$, 45min soak in $WetO_2$, 20min N_2 Purge, 20min ramp down in N_2
- Lithography Level4 is Pfet VT adjust

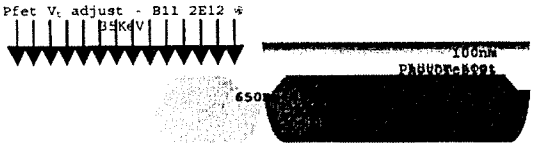

Figure 5: Representative Cross-section through PFET V_T adjust

- Resist Strip, Kooi Oxide etch – 1.5min BOE,RCA Clean
- Gate Oxide Growth - Same as PadOx1 & 2
- Poly gates are doped with N250 spin on glass - 20 min ramp to 1000°C in N_2, 15min soak N_2, 30min ramp down in N_2
- Etch SOG
- Lithography Level5 is Poly gate definition

- RIE Poly Etch

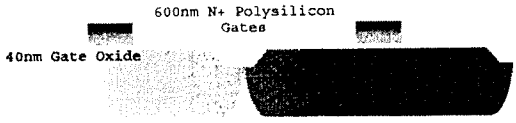

Figure 6: Representative Cross-section through Polysilicon Etch

- Resist strip
- Lithography Level6 is N+ Source/Drain
- N+ S/D Implant, Resist Strip
- Lithography Level7 is P+ Source/Drain
- P+ S/D Implant, Resist Strip, RCA Clean
- Polysilicon is processed through a re-oxidation and densification - 10min ramp to 850°C, 15min soak in $WetO_2$, 5min $DryO_2$ purge, 10min ramp down

Figure 7: Representative Cross-section through Polysilicon Re-Oxidation

- Deposit LTO
- S/D Anneal - 10min ramp to 1000°C in $DryO_2$, 20min soak in N_2, 10min $WetO_2$ soak, 10min ramp down in N_2
- Lithography Level8 is Contact Cut
- RIE Oxide Etch, w/ follow-up BOE dip
- Resist Strip, RCA Clean
- Aluminum Sputter
- Lithography Level9 is Metal1
- Aluminum Etch, Resist Strip
- Sinter - 20 min. 425°C in H_2/N_2

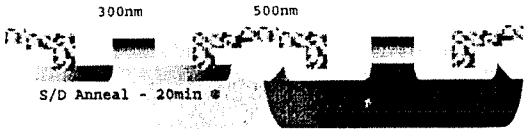

Figure 8: Representative Cross-section through finished process

B. Process Simulation

Silvaco simulation tools were employed to accurately predict the outcome of devices fabricated with the Strongarm process. Full process tolerances were explored, with effects ranging from changes in film thickness, implant dose/energy, and thermal budget being investigated.

Table 1: NFET & PFET Parameters for Simulated Devices

	NFET	PFET
Channel Type	surface	buried
1-D VT	+1.0V	-1.0V
Gate Oxide	40nm	40nm
Junction Depth	0.50μm	0.75μm
Surface Conc.	NA=3E16cm^{-3}	ND=4E16cm^{-3} w/o adjust

Silvaco's Athena was used to finalize the process steps to meet the target specifications. Table I shows the physical specifications for the CMOS devices, to which SPICE Level-2 parameters were extracted through numerical methods. Fig 9a and fig 9b show screen captures of the simulated NFET and PFET. The devices were simulated to a 2μm metallurgical length. Fig 10 shows a family of curves for both an NFET and PFET with mask-defined channel length of 2μm.

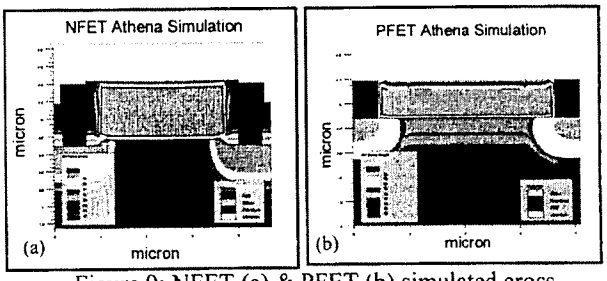

Figure 9: NFET (a) & PFET (b) simulated cross-sections

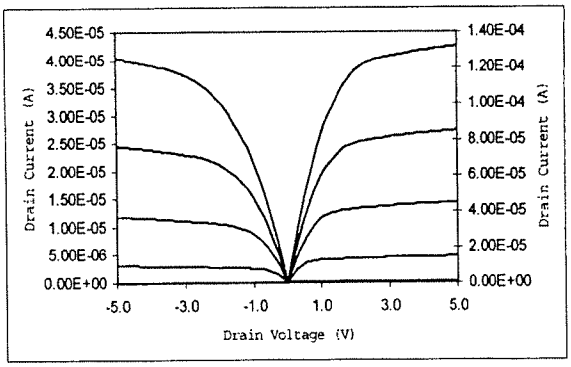

Figure 10: NFET & PFET Family of Curves – L_{met}=2μm

C. Parameter Extraction

SPICE Level-2 parameters were extracted using standard device physics equations. The equations and the method for parameter extraction are seen in great detail in Reference [3]. The reader is encouraged to seek this reference for a more detailed explanation. What follows in Table 2 is a summary of the extracted parameters on a simulated PFET.

Table 2: SPICE Level-2 Parameters for a Simulated PFET

Parameter	Value
V_{TO}	-1.025V
Gamma	$0.501V^{1/2}$
μ_0	$318cm^2/v\text{-}sec$
Theta	$0.016V^{-1}$
ΔL	0.06μm
R_{SD}	2.5KΩ-μm
V_{MAX}	1E6cm/sec
Lambda	$0.075V^{-1}$
S-Swing	100mV/dec

Following the completion of SPICE parameter extraction a model was created and compared to simulated Athena results. Fig 11 shows an overlay for a PFET of Athena family of curves with extracted SPICE Level-2 models. The fit is good, yet shows the limitation of SPICE Level-2 accuracy.

IV. FABRICATION

There is a definite need to verify any theoretical and/or simulated device or process with real world results. Following the work put into simulating and extracting parameters from the theoretical devices the Strongarm process was used to fabricate two initial lots of CMOS wafers.

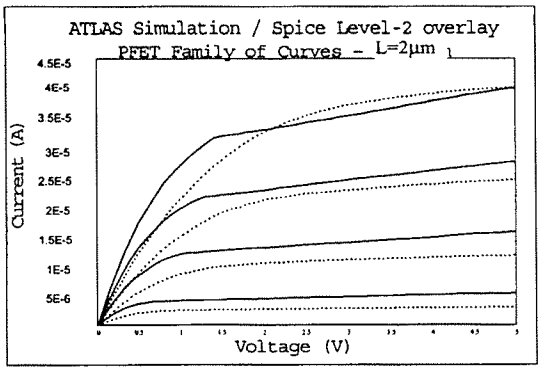

Figure 11: Overlay of Simulated & SPICE Level-2 Model Family of Curves for a PFET – L_{met}=2μm

A. Electrical Test on Strongarm CMOS Lot #1

SPICE Level-2 parameters were extracted from the fabricated devices. Measurements were taken on an HP4145 Semiconductor Parameter Analyzer, networked via GPIB to a PC using Metrics software.

The NFET threshold voltage hit the target of 1V (see fig 12), with good uniformity within-wafer, and wafer-to-wafer. The PFET threshold voltage came in at -2.1V (refer to fig 13), or about 1.1V below the expected -1V. Interestingly enough, this includes four process splits that adjusted the PFET V_T adjust implant between $2E12cm^{-2}$ and no implant, with all wafers showing similar threshold voltages. The problem is still currently under investigation

Table 3 shows the results of the SPICE Level-2 extraction performed on the fabricated devices of mask drawn length of 8μm. It should be noted the ΔL term equal to 2.45μm. This effectively makes the 8μm devices 5.55μm long, and gives good reason as to why mask drawn lengths of 2μm did not yield. In examining the cause of this it is noted that the polysilicon RIE was over aggressive, causing a large undercut.

The μ_0 factor for the NFET seems unusually low for the electron mobility. What needs to be noted is that this term is calculated with a W_{eff} of 8μm which may actually be smaller. Over etch of Nitride2 could result in a decreased width, as well as the birds-beak affect from LOCOS2.

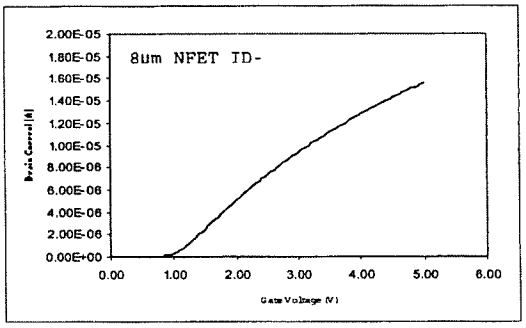

Figure 12: NFET ID-VG Curve

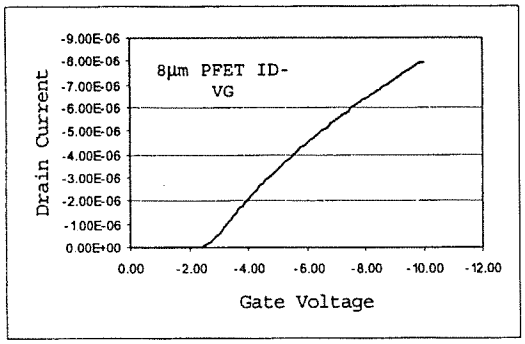

Figure 13: PFET ID-VG Curve

Table 3: SPICE Parameters from Measured NFET & PFET

Parameter	NFET Value	PFET Value
VTO	1.0V	-2.1V
Gamma	$1.13V^{0.5}$	$0.455V^{0.5}$
μ_0	$430cm^2/v\text{-}sec$	$245cm^2/v\text{-}sec$
Theta	$0.066V^{-1}$	$0.068V^{-1}$
ΔL	2.45μm	2.45μm
R_{SD}	600Ω-μm	100Ω-μm
S-Swing	125mV/dec	140mV/dec

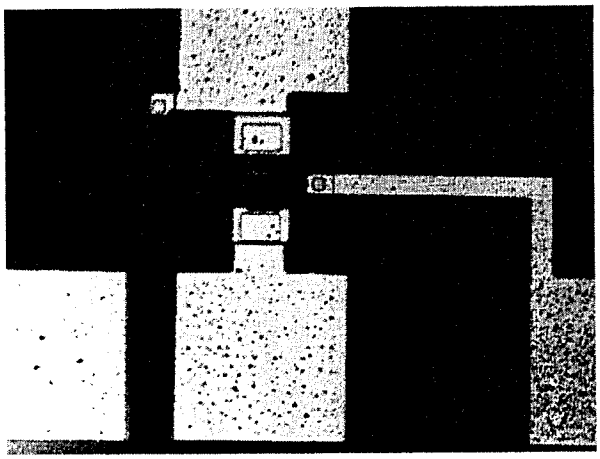

Figure 14: Photograph of 8μm x16μm (L x W) NFET

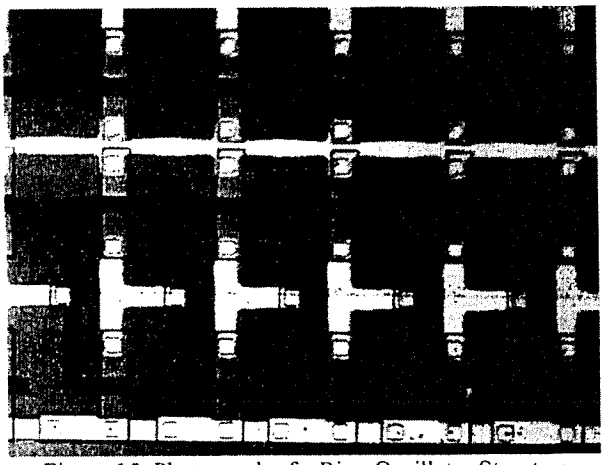

Figure 15: Photograph of a Ring Oscillator Structure

B. Strongarm CMOS Lot #2

As the first CMOS lot using the Strongarm process came to completion a second lot was started. This second lot was to be used to test the integration of CMOS transistors with Resonant Interband Tunneling Diodes (RITD) [4]. Not only was this a logical progression for testing the repeatability of the Strongarm process, but it was also an excellent opportunity to assess the ability to integrate a second technology with Strongarm fabricated CMOS. Fig 16 shows a representative cross-section of the proposed devices. As seen in fig 17 there was a large variety of CMOS and RITD structures on the die.

Upon completion of the lot, electrical test was conducted in the same way as the first lot. Threshold voltages for the NFET and PFET proved to be the same as the initial lot, showing the Strongarm process is repeatable, including the PFET V_T issue.

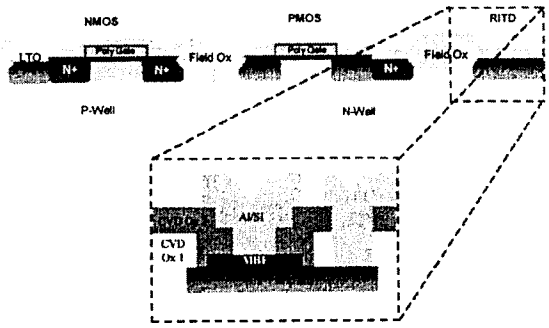

Figure 16: Representative Cross-section of RITD integrated with Strongarm CMOS

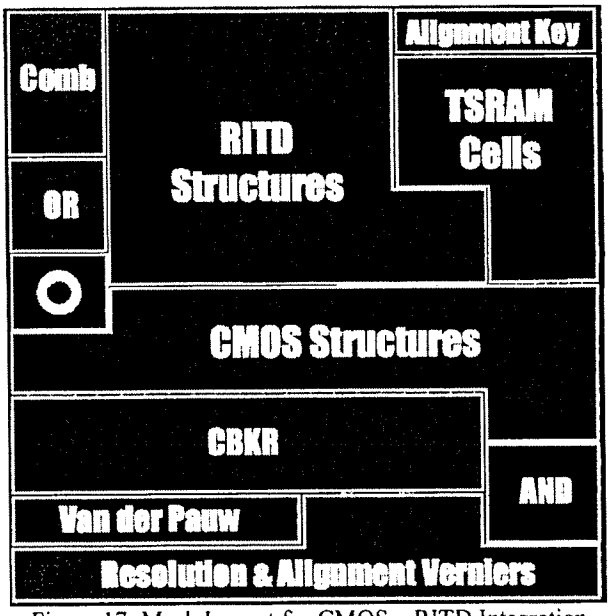

Figure 17: Mask Layout for CMOS – RITD Integration Project

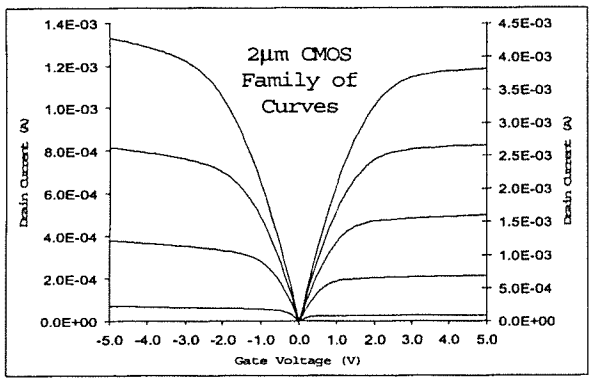

Figure 18: NFET and PFET Family of Curves – L=2µm

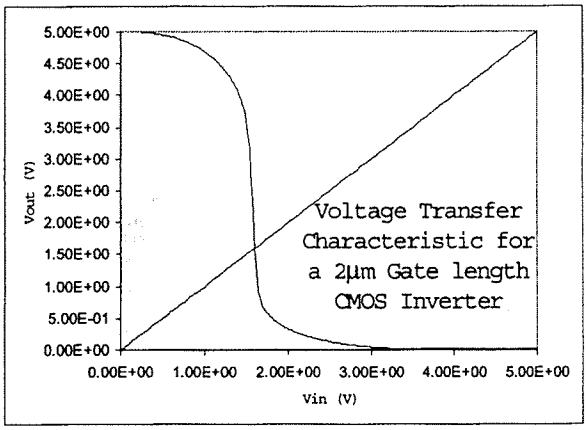

Figure 19: VTC for a CMOS Inverter – L=2µm

Further electrical test into the CMOS structures on the second lot proved a good family of curves for 2µm NFET and PFET devices. This was encouraging, and attributed to the fact that a different polysilicon etch was done, using a different reactive ion etcher. Fig 18 shows the NFET and PFET family of curves, while Fig 19 shows a voltage transfer characteristic for a CMOS inverter, with drawn gate lengths of 2µm.

V. CONCLUSIONS

Strongarm has proven to be a very robust and well characterized manufacturing process. Extensive simulation and characterization created an excellent understanding of the process and allowed a good prediction of how devices would operate once fabricated. As the cost of manufacturing IC's increases, the ability to accurately predict the results prior to committing to silicon becomes critical. Accurate SPICE modeling from simulation can help to speed up the design process for circuit designers, enabling faster turnarounds.

As shown during this investigation, a robust and repeatable process has been designed. This opens the door for further development in the realm of integration with additional devices, as seen with the RITD's [5]. Additionally, the repeatable nature allows the ability for RIT to design circuits that utilize the Strongarm process, and view good working results.

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ACKNOWLEDGMENTS

The author acknowledges Dr. K. Hirschman as advisor for the project, Dr. S. Kurinec, R. Saxer, S. Sudirgo, K. Tabakman and S. Widlund for help and guidance throughout the project. Also the SMFL staff including S. Blondell, R. Battaglia, J. Nash, B. Tolleson, D. Yackoff, J. Cabacungan, S. O'Brien, T. Grimsley and A. Raisanen.

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