Micro Shutters on Quartz Substrate

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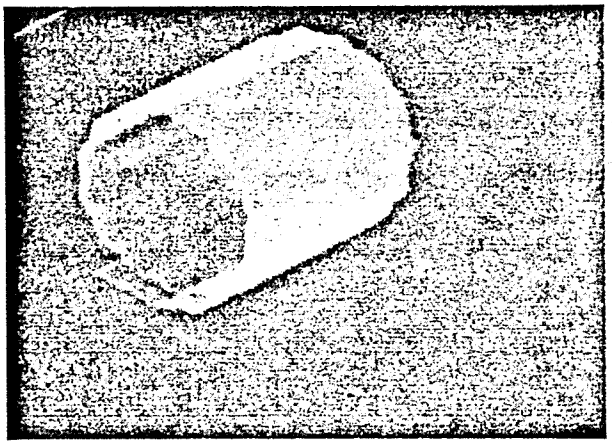
Abstract-Micro shutters are micro mechanical devices that fulfill optical and/or electrical functions. The use of such devices has gained momentum in the recent years as their minute size and high speed are viewed to be advantageous for use as optical or electrical switches. The particular type of device targeted in this project is generally referred to as a micro-actuator. It is a device that is curled in its natural state and uncurls when an external voltage is applied to it. When a transparent plate (E.g.: quartz substrate) containing thousands of such shutters can be inserted in a telescope for example, we can selectively extend regions of shutters (by making them uncurl through the application of voltage) to block out and reduce the intensity of bright sources (brighter stars) that may overshadow weaker light sources in the image. The shutters will in essence reduce the proximity effect that leads to the loss of resolution when two objects are closer than the Raleigh criterion. Micro shutters on transparent substrates were built and patented in 1998 through further research from the same participants [2].

1. INTRODUCTION

A. *THE MICRO-ACTUATOR*

The particular type micro-shutter of interest in this project is generally referred to as a micro-actuator, while one side of the device is attached to the conductive layer, the other sides are free to move, enabling the device to curl in it's preferential direction due to internal stress. The film stack would uncurl when a bias is applied on the conductive layer of the stack. The device shown is a micro-actuator in its' natural state (without applied voltage) built on Silicon substrate by students working under Dr.Grande's supervision at RIT. The possibility of use of such devices in telescopes has sparked interest within the department of imaging science at RIT. When a transparent plate (E.g.: glass substrate) containing thousands of such shutters can be inserted in a telescope for example, we can selectively extend regions of shutters (by making them uncurl through the application of a voltage) to block out and reduce the intensity of bright sources (brighter stars) that may overshadow weaker light sources in the image. This will enable us to obtain clear images containing brighter and weaker sources that are next to each other. The shutters will in essence reduce the proximity effect that leads to the loss of resolution when two objects are closer than the Raleigh criterion. The primary distinction between this project and the previous research performed by the co-op students is that the devices manufactured in this experiment would be on a transparent substrate (either Pyrex or Quartz).

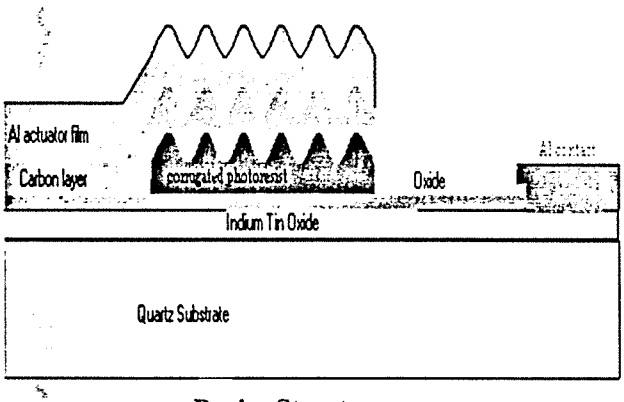


SEM photo courtesy of Dr.Grande's co-op students.

The lithography process for the transparent substrates would be the key to this experiment, various issues such with wafer coating, aligning and exposing using the GCA-stepper and achieving the desired corrugated profile would prove to be a challenge. Another benefit from this project would be the experimental determination of the optimal settings to obtain the smooth sinusoidal corrugated profile of the resist.

B. CORRUGATION PROFILES

The corrugated profile is vital to how well the device functions. The sinusoidal profile on the top of the layer makes the film stack that is deposited on top (namely the carbon layer and the Al actuator film) to conform to the same topography. This results in the horizontal perforations on the stack that force it to curl upwards



Device Structure

rather than in any other direction. An exposure matrix would be run to obtain the optimum exposure (level 4-mask) for the resist. The figure given above represents the built device before the removal of the photoresist; once the photoresist is removed the film stack would curl upwards.

2. EXPERIMENTAL DESIGN

A. DOE

The corrugation profiles are created by exposing Level 3 of the Micro shutter mask and immediately following it with a short exposure of Level 4. Level 3 defines the areas in which the resist should be in (patterning on top of Al contact layer) and Level 4 concerns itself with the formation of the corrugated profiles. An exposure array was run for level 3 and level 4 separately. The optimum exposure time was expected to be about 30% higher than that of the values required to make corrugations on photoresist coated Silicon. The required exposure times for photoresist on Silicon were 0.4 seconds for Level 3 immediately followed by 0.023 seconds of exposure on Level 4 on the mask. The exposure array proved that the required exposure times were much higher than the expected increase of 30%. By inspecting the features obtained through the exposure arrays it was determined that the optimum exposure time for level 3 was about 0.6 seconds. From the preliminary runs it was observed that the exposure time of Level 4 had a direct impact on the depth of the corrugation profiles. A DOE was designed to obtain the optimum corrugation profile. The Level 3 exposure time was held constant at 0.6 seconds. The level 4 exposure time was varied in minimal amounts as tremendous shifts in the corrugation profile could be observed for minimal changes in Level 4 exposure time.

Post exposure bake was chosen as factor because it reduces the dependency of the corrugation profiles on the exposure time. This would intern give us more process latitude in regards to the depth of the corrugation profile. Develop time had an impact on how sharp the resist profiles were, when either over developed or under developed the only partial corrugations were seen in the resist layer.

Pattern	Level 4 Exposure time	PEB Temperature	Develop Time
0	0.2094	130	45
—	0.2092	125	35
-+-	0.2092	135	35
+-+	0.2096	125	55
+++	0.2096	135	55
-+	0.2092	125	55
+-	0.2096	125	35
++-	0.2096	135	35
0	0.2094	130	45
-++	0.2092	135	55

DOE

A two level fractional factorial design was chosen because of limitations to resources. There were ten Pyrex wafers available and that limited the number of runs to ten. This was so because access to AFM is limited and is time consuming (roughly 3 hours/wafer). The wafers had to be taken out of SMFL to be measured therefore we cannot bring them back in for processing repeatedly.

3. PROCEDURE

1. Deposit ITO using CVC601 sputterer (5mT/100W/150degrees/15sccmO2/120sccmAr).
2. Deposit O2 using the 6" LTO machine. Oxide thickness target = 5000A.
3. Pattern contact cuts (1rst level of mask). GCA stepper used with stepper job: TIONA.RSC
   Mack: Justin Brown's micro-shutter mask (Level 1). Photo steps were performed using the wafer-track.
4. Sputter Aluminum (5,000A).
5. Pattern and etch the Al contact cuts. (2nd level of the same mask.).
6. 3rd and 4th Levels of the mask exposed. A high dose for exposure of level 3 immediately followed by a low dose exposure of level 4 would give the corrugated profile on the resist that is desired.
7. Deposition of Carbon film using the Drytech Quad. (Only gas flown was methane.)

8. Deposition of Aluminum for Actuator film (400A).
9. Patterning of level 5 (micro shutter pattern).
10. Etch Aluminum in 50C Al etch solution.
11. Etch carbon layer, done in Drytech with O2 clean recipe.
12. Liftoff in Acetone/IPA bath to remove the resist.

4. PROCESSING ISSUES

A. HANDLING CONCERNS

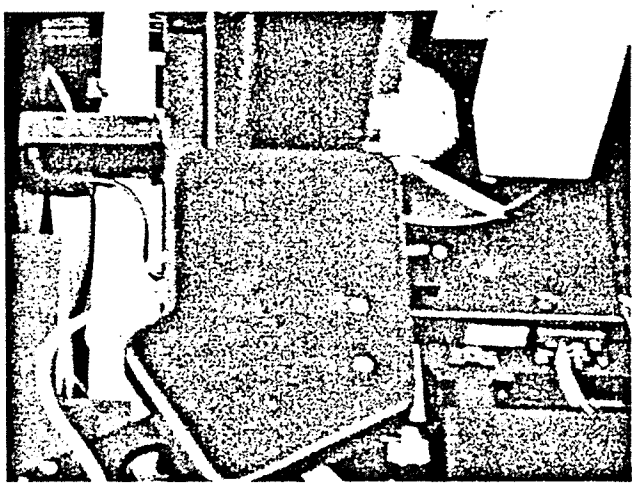
The cassette-loading bay in the SVG-wafer coating track had optical sensors. These sensors would go through the quartz substrate thus they could not "see" the wafers. Past attempts to coat photoresist on quartz had resulted in broken substrates therefore it was decided not to use the SVG-track. The wafers were coated manually using the hand-spinner with the standard recipe (1) at 4500RPM.
Similar obstacles were expected when attempting to load and find the flat in the GCA-g-line stepper because it had optical sensors as well. It was decided to use either a photoresist marker and darken a ring at the edges of the substrate to block the sensors from going through thus, enabling the sensors to recognize the presence of the wafer and the position of the flat. Another method thought of was to coat the back of the wafer with dyed resist (HIPR6517) that was already available at RIT.

B. ALUMINUM OXIDE FORMATION

Aluminum (contact layer) when in contact with Indium tin Oxide (bottom electrode) begins to extract the oxygen and form Aluminum Oxide. This would be an issue of concern as AlO_2 is an insulter. A thin W film was deposited as a buffer layer to enhance the conductivity.

C. ALIGNMENT ISSUES

The vacuum chuck at the loading bay of the GCA-stepper had difficulties picking the Quartz substrate. It would rise and attempt to continue going through the wafer unlike with the silicon substrate, which the chuck would lift and slide over to the track towards the flat aligner. It appeared that the chuck could differentiate the weight difference between the substrates. The wafers are then transferred from the cassette to the flat finder that finds the flat using optical sensors and a robotic arm lifts and places the wafer under the lens column in the stepper. The flat finder cold not "see" the quartz substrate and would alarm out. As this was an anticipated issue a black ring was made on the outer edge of the wafer in order to block the sensors from through thus enabling the flat finder to realize the presence of the quartz substrate. However, this method did not work for reasons yet to be known. Varying widths of the ring were tried and the dyed photoresist from the marker appeared to be completely opaque. In order to get around this obstacle a Silicon Dummy was allowed to load all the way to the chuck. Vacuum was shutoff and the dummy was replaced with the quartz substrate. The wafer flat was aligned with the chuck flat as seen in figure 3. Chuck vacuum LED served as an indicator to see how



good the positioning was because if the wafer flat were not positioned exactly above the chuck flat the LED would not be lit.

D. OBTAINING THE CORRUGATIONS

The corrugation profiles of photoresist on Quartz had not been done ever at RIT and there were no available literature to indicate the appropriate time requirements for exposure. The prediction was that the increase would be about 30% but after numerous iterations of exposures the times of exposures were found to be 50% greater for Level 3 and above 800% increase (0.023 for Si based corrugations to 0.2094 for Quartz based corrugations) greater for Level 4.

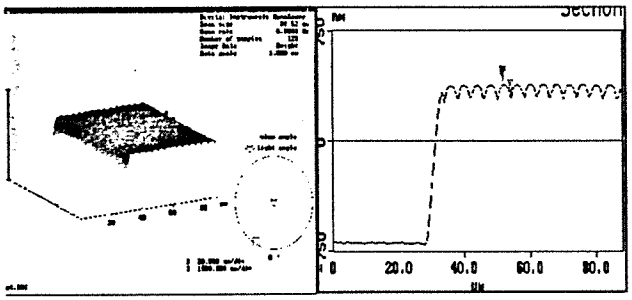
6. RESULTS

A. ITO LAYER

The successful deposition of a conductive and transparent ITO layer was achieved using the CVC601 sputtering tool. The two gasses that were flown were O_2 and Ar. If the O2 flow increased it was observed that the film became more metallic and opaque. A balance had to be struck to obtain a film that was transparent yet conductive. Four pt probe test was performed, for an applied current of 53mA the corresponding voltage was 0.068V. Which results in a sheet resistance of 0.58ohms.

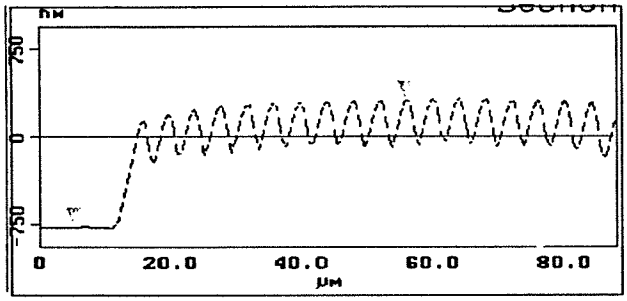
B.CORRUGATIONS

The corrugation profiles obtained from the DOE were inspected under an electron microscope; the ones that appeared to have the best profiles were then taken over to



Figure

the Mechanical Engineering department and measured using the Atomic Force Microscope. In figure 4 the profile was obtained for Exposure time of 0.2092 seconds, PEB =125degrees and Develop time of 45seconds. It had a step height of 1.09uM and the amplitude of corrugations was 50nm. This profile had a smooth sin wave pattern on the top of the resist, but these corrugations might not be the most suitable as they possibly are not deep enough.



Another wafer was identified to have profiles (shown above) that were more appropriate for the use in Micro-shutter construction. It had the amplitude of corrugations as 180nm, this would be deep enough. The profile also looks sharper which would be advantageous because it allows for the deposition of thicker films above it if needed. Sharper and deeper corrugations can force the stack above to adopt the same profile better than a smooth corrugated profile. An increase of 130nm, which was a direct result of the increase in exposure time by 0.0002seconds.

C. W DEPOSITION

W was deposited using CVC601 sputtering tool with 500W/3mT/8.4e-6for 480s sec to obtain 500A film. The deposition was successful but the film started to peel and flake within minutes of removal from the chamber.

7.DISCUSSION

Pyrex wafers were used for the DOE to obtain corrugation profiles. While Quartz wafers were used for the construction of the devices. There were only 4 quartz wafers available due to cost and a limited budget. Pyrex wafers could not be used for the construction of devices as they would contaminate chemical baths and possibly other processes that are performed in the lab due to the fact that they contain small amounts of Na and other material that are harmful to device processes.

Further processing is needed to obtain suitable process conditions for W so that the adhesion issue may be solved or find other conductive materials that would not form an oxide at the ITO interface. Another material that could be used is TiW but the target is not available for CVC601 sputtering tool. However, evaporation methods may an option to deposit the film.

The time of exposure dependency for the corrugation profiles is still too high. As the AFM becomes more available further processing can be performed towards achieving more process latitude with regards to exposure time requirement for Level 4. Alignment was a major issue throughout the project. Level 1 did not require any alignment. Level 3 and 4 were run consecutively while only the mask was swapped leaving the Pyrex wafer in the stepper. Therefore alignment between Level 3 & 4 was not an issue. However when the device wafers (Quartz) with contact Al deposited were ready for Level 2 exposure (contact pattern) alignment was off. By this time the wafer was opaque and with the outer ring of the wafer dyed using a photoresist pen the flat finder in the stepper could "see" it. After various attempts with different methods it was concluded that the method of manually swapping the quartz wafers for Level 1 had enough deviation that would align with robotically placed Level 2.

After further experimentation with the stepper it was decided that the ideal way to process Quartz substrates would be to deposit 400A of Al at the back of the wafer and block out the outer ring (lip form the wafer holder prevents the deposition of Al in the edges) with photoresist pen. The only way to get around the loading bay is to let a Si dummy be picked up from the cassette and placed on the track towards the flat finder and replacing the dummy with the quartz wafer before it reaches the flat finder. Tests were performed and the flat finder did find the flats, next the robotic arm will place the wafer under the exposure column and alignment can be done.

8. CONCLUSION

Through the course of the project some of the most important Suitable corrugations were obtained. The difficulties in alignment hindered the successful completion of the project. Another limitation was the lack of device wafers. Once the optimum way to process was determined there were no Quartz substrates available. We expected a lot of issues handling Quartz wafers and dealing with tool limitations and have addressed all that have appeared so far. All levels of the device (5 lithography steps along with multiple deposition steps) have been performed at various stages of the project. Most of the issues regarding the fabrication process have been addressed. Through this project it was determined the Process is feasible. The project presented numerous challenges and served as a great learning experience in a region in which not much processing had been done at RIT.

REFERENCES

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