Design and Fabrication of a Micromechanical Pressure Sensor

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Abstract—A Microelectromechanical (MEMS) pressure sensor was designed, fabricated, and tested. Photomasks were designed for the project and built in house at RIT. The masks included designs for three separate device designs: devices to be fabricated with a KOH bulk etch, devices to be fabricated with an Surface Technology Systems (STS) Deep Reactive Ion Etch (DRIE), and a third set of scaled device designs for use with the STS DRIE process. Devices were tested in house, and the ideal design was determined. The most sensitive device, which had a resistor L/W of 10, demonstrated a voltage differential of 39 mV.

Keywords

Microelectromechanical Systems (MEMS), Potassium Hydroxide (KOH), Deep Reactive Ion Etch (DRIE)

1. INTRODUCTION

Microelectromechanical systems (MEMS) are devices that have mechanical and electrical components. By utilizing the material properties of silicon, many small devices ranging from accelerometers to tiny motors can be fabricated on a single chip. The focus of this project will be to design, fabricate, and test micromechanical pressure sensors. The sensors will operate by allowing a thin single-crystal silicon membrane to deflect under positive and negative pressure situations. By sensing the amount of deflection at various pressures, the chips can be tested. The amount of deflection will be proportional to the pressure being detected. Small polysilicon resistors will be fabricated on the membrane and connected in a wheatstone bridge arrangement. Four resistors will be connected serially on top of the membrane to form a loop. Applying a voltage across two nodes, and sensing another voltage across the remaining two nodes can obtain a signal. As the membrane of thinned silicon deflects, the resistors atop it will change shape slightly. Their resistance will change as a result of their change in shape, and the output voltage across two nodes will change, indicating a pressure. By calibrating the sensor to normal conditions and then measuring this voltage, pressure can be determined empirically. Tests can be performed using a voltage supply and a voltmeter. A vacuum chuck will provide the necessary stimulus to make a change in output voltage, and allow calibration of the device, provided a known vacuum is applied. The accuracy of the sensor can be compared to previous iterations of the device as well as designs fabricated within the scope of this project.

2. THEORY

These pressure sensors operate as a result of two factors. A thin silicon membrane must first deflect under pressure, and the amount of deflection must then be detected somehow and then calibrated. This will allow a pressure to be detected. There are several ways of detecting the amount of deflection in a diaphragm. Capacitive, piezoresistive, and optical sensors may all be used.

The capacitive sensor works by fabricating two parallel conductive plates over the surface of the diaphragm. One plate is fixed to the moving diaphragm, while the other is not. As a pressure is applied, the distance between the two plates will change. Capacitance will change as a function of the spacing between the two plates, indicated by equation 1. C is capacitance, ε_0 is the permittivity of free space, A is the area of the capacitor, and d is the distance separating the plates.

$$C = \frac{\varepsilon_0 A}{d}$$

Equation 1: Capacitance Equation

Electronics are frequently used to convert the capacitance of the sensor into an output voltage. This makes the sensors easier to integrate into other devices. Advantages of this type of sensor are excellent precision and accuracy, although this type of sensor is typically more difficult to fabricate due to added complexities of the capacitance to voltage electronics.

The optical sensor works by illuminating the diaphragm with a laser of known wavelength and detecting the reflected intensity from the diaphragm. As the diaphragm deflects, the reflected intensity will swing from high to low every half wavelength as the reflected signal

interferes constructively and destructively with the incident radiation. By monitoring this signal, interferometric techniques may be used to detect pressure.

The piezoresistive sensor was fabricated in this project. Resistors are placed at the edges of the diaphragm, as shown in figure1.

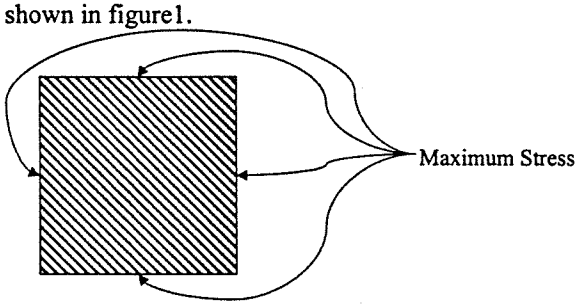

Figure 1: Maximum Stress Points

These areas are the maximum stress points of a square diaphragm. When the diaphragm distorts under pressure, the resistors will distort proportionally under stress. By arranging the resistors in a wheatstone bridge pattern, and applying a voltage across two nodes and measuring a voltage across the other two, an output voltage can be obtained that will vary with applied pressure.

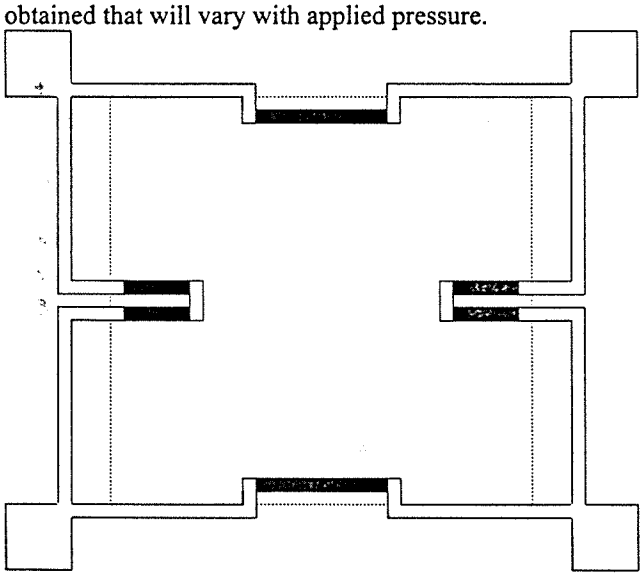

Figure 2: Wheatstone Bridge

As the diaphragm deflects, each resistor will distort in the direction of the center of the diaphragm. This will mean that the resistors at the left and right of figure two will stretch, increasing their resistance, while the resistors located at the top and bottom will widen, decreasing their resistance. One advantage to this design is that no other circuitry is required to obtain a voltage signal, as in the case of the capacitive sensor. These devices are subject to inaccuracies due to temperature, unlike the capacitive sensors described earlier.

Using equation 2, the approximate stress at the maximum strain points was calculated.

$$\sigma = 0.3\left(\frac{L}{H}\right)^2 p$$

Equation 2: Stress at Diaphragm Edges *[K. Wise]*

Where L is the length of the diaphragm, p is the applied pressure, and H is the thickness of the diaphragm. Using values for L of 3500 μm and H of 15μm, the stress is equal to 1.6×10^6 N/m^2. By using equation 3, the stress at the edges of the diaphragm can be converted to strain, where sigma is stress, gamma is Young's Modulus of silicon in this case, and epsilon is strain.

$$\sigma = \gamma\varepsilon$$

Equation 3: Stress Strain Relationship

Using the values obtained above, the approximate strain experienced in the resistor locations is 8.9×10^{-6}

The values for each of the resistors can be found using equation 4, where rho_s is the sheet resistance of the polysilicon, L is the resistor length, and W is the resistor width.

$$R = \rho_s \frac{L}{W}$$

$$\rho_s = \frac{V}{I}\frac{\pi}{\ln 2}$$

Equation 4: Resistor Equations

Using sample values for the sheet resistance of the doped polysilicon, the resistance of a device with L/W of 6 was estimated to be about 372Ω.

When no pressure is applied, the resistors will remain at their design values of 372Ω. However, when pressure is applied, the resistance will change as strain acts on the resistors. By substituting the change in physical resistor dimensions into the resistor equations, equation 6 can be used.

$$R_{Longer} = \rho_s \frac{(L + \Delta L)}{W}$$

$$R_{Wider} = \rho_s \frac{L}{(W + \Delta W)}$$

Equation 5: Resistance under Stress

Using the values above, The resistors at the sides of the diaphragm will increase their resistance to 372.003Ω. The resistors located at the top and bottom of the diaphragm will decrease resistance to 371.997Ω.

Because of this slight change in resistance, a voltage difference in the mV range can be measured with applied pressure.

3. DESIGN

Three photomasks were designed and fabricated. The first mask was a backside mask, used to define the openings for the diaphragms on the back of the wafer. The second mask was a front side mask used to define the polysilicon resistors located atop the thin silicon diaphragm. The third level was metal, used to cover areas of the polysilicon layer not intended to become resistors, as well as creating contact pads for test equipment. Each reticle contained a three x three array of a test die.

Several device types were created on this test die. Figure 3 shows a schematic of the mask used. Three devices were designed for the mask. Devices on the left column of the reticle field were designed for the KOH process. KOH etches [100] single-crystal silicon along the [111] crystal direction *Petersen[4]*. This results in a sidewall profile of 54 degrees for devices fabricated with this etch. The opening on the backside of the wafer for these devices is nearly 1300 μm larger than the intended diaphragm on the front of the wafer to compensate for this etch.

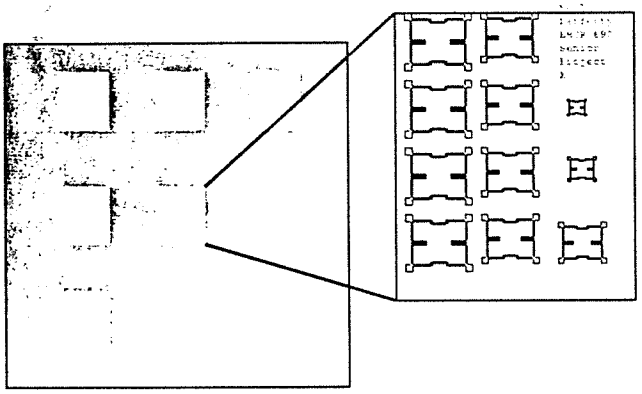

Figure 3: Reticle Layout

Devices in the left column have the same diaphragm size as each other. The backside openings for these devices are 4376 μm by 4376 μm, in order to achieve a diaphragm size on the front of the wafer close to 3000 μm. The center column contains devices which were optimized for the STS DRIE process. This process will have near 90 degree sidewalls, and therefore backside openings for these devices are 3000 μm x 3000 μm. The right column contains scaled devices, whose diaphragm size varies from 2500 μm x 2500μm to 1000 μm x 1000 μm. Devices in the top row have resistor sizes of 210 μm x 50 μm for a L/W of 4.2. The next row has resistor sizes of 310 μm x 50 μm for a L/W of 6.2. The second row from the bottom has resistors 500 μm x 50 μm for a L/W of 10, and the bottom row has resistors 300 μm x 10 μm for a L/W of 30.

4. FABRICATION PROCESS

A. KOH Bulk Etch Process

Devices using a potassium hydroxide bulk silicon etch were fabricated by first double side polishing a [100] wafer. Wafers were double side polished to get better images during the subsequent backside lithography step, as well as to increase nitride uniformity on the wafer backside. Wafers were polished using Levasil 100/45, diluted 2:1 with water. The table RPM was set to 60 RPM, the downforce was set to 6 PSI, the slurry flow was adjusted to about two drips per second, and the wafers were polished for 20 minutes each. After the polish, both sides of the wafer had equal mirror like shine. An RCA clean was performed next, in order to remove metal ions from the wafer that may contaminate the low-pressure chemical vapor deposition (LPCVD) tool. The wafers first go to an APM bath for 10 minutes, then a 5-minute rinse. The wafers are then dipped in hydrofluoric acid for 1 minute followed by a 5-minute rinse. The wafers then go to an HPM bath for 10 minutes, followed by a 5-minute cascade rinse. Finally, wafers are dried using a spin rinse dryer (SRD) unit.

Nitride is then deposited. The factory Nitride 810 recipe is used with a deposition time of 10.8 minutes in order to obtain 700 Å of Si_3N_4. This will be the nitride hard mask used to protect the wafer in the KOH for nearly 10 hours. Optical film thickness metrology was performed on the film using a Nanometrics Nanospec AFT tool. The color of the wafers was a deep purple.

Backside lithography was performed on the wafer using a Karl Suss MA-150 mask aligner. Shipley 812 positive photoresist was coated on the SVG wafertrac using program 1. Each wafer received an HMDS vapor prime to promote adhesion of the photoresist, followed by a 60-second chill, and then resist was coated at 4500 RPM. A softbake was done at 90 degrees C for 1 minute in order to remove more solvents from the resist then spin coating alone, further enhancing imaging capabilities. The backside diaphragm mask was used with a dose of 50 mJ/cm^2 to image the diaphragm outlines in resist. Development was done by hand using CD-26 positive developer for 1 minute with slight agitation. A 1-minute hardbake at 120 C was used to harden resist slightly before etching. Microscope inspection confirmed that backside litho was performed successfully.

Using the LAM AutoEtch 490, the Si_2N_4 was etched using a custom made recipe. The etch pressure was set to 310 mTorr, Electrode gap was set to 1.15, and SF_6 flow was set to 60 SCCM. Each wafer was etched for a total of 20 seconds at 175 watts. All Nitride was removed in areas uncovered during photoresist develop. Wafers were then sent to the branson asher, where the 4 inch hard ash was used to remove photoresist prior to KOH bath.

Figure 4 shows a schematic of the wafer processed up to this stage.

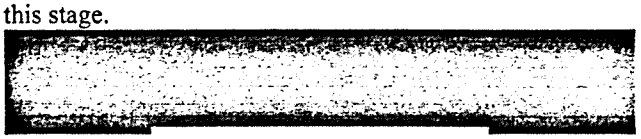

Figure 4: Wafer after Resist Removal

Next, KOH is used to define the regions where the thin diaphragm will exist. Wafers are assumed to be on the order of 500 μm thick. Therefore, to create a 20 μm thin diaphragm, approximately 480 μm of Si must be etched. The KOH rig was set to 72.0 C, stirrer speed of 2, and 22.5% KOH by weight was used to perform the etch. The KOH bath used had an etch rate of about 0.7 μm/min. The wafer was etched for about 10.5 hours total.

An RCA clean was then performed using the same process described above. With the diaphragms defined and tested for movement, the next stage was the deposition and doping of polysilicon. Using the SMFL standard polysilicon recipe and the six-inch LPCVD tool, 6000Å of polysilicon was deposited. Emulsitone N-250 phosphorus doped glass was used as a dopant, and spun on at 3000 RPM. The wafer was baked for 15 minutes at 200C, then loaded into the N-type diffusion furnace for a doping step. Recipe 120 was used to dope the polysilicon. The recipe features a 1000 C soak for 15 minutes in order to activate the phosphorus from the spin on glass (SOG). The diffusion is followed by a dip in buffered HF for 5 minutes in order to remove the glass layer from the wafer surface. Wafers were rinsed for 5 minutes, then sent to SRD. A four-point probe to check resistivity of the polysilicon was performed. Using the second part of equation 4, the polysilicon was found to have a resistivity of 6.19 Ω/sq.

Resistor level lithography was done using hand resist coating. With the diaphragms already defined, the vacuum chucks typically used to hold the wafers during spin become less effective, and it was feared that the wafer might have released during processing. The wafer was first dehydrate baked at 200 C for two minutes. After cooling, the wafer was coated with HMDS (1 drop) and spun at 3000 RPM for 1 minute. The wafer was then coated with Shipley 812 using the same recipe. A softbake was performed at 90 C for 1 minute. Using a wafer scribe, two diaphragms were punched through on opposite hemispheres of the wafer. The holes would serve as alignment features so that the polysilicon resistors would be placed at the correct high strain areas on top of the diaphragm. Alignment and exposure was performed on the MA-150 using a dose of 50 mJ/cm^2. A post exposure bake (PEB) was done at 110 C for 1 minute. CD-26 positive developer was used with slight agitation for 1 minute to develop the resist. A hardbake was performed for 1 minute at 120 C in order to harden the resist. Optical inspection revealed that the resist had been patterned properly and that alignment with the diaphragm level was within specifications.

Using the Drytek quad reactive ion etch (RIE) tool, the polysilicon was etched using the FACPOLY recipe. The time of etch was changed to 3 minutes and 45 seconds, in order to remove the polysilicon in all exposed areas without damaging the nitride layer underneath. The resist was subsequently ashed using the branson asher and 4 inch hard ash recipe. Figure five shows a process cross section up to this step.

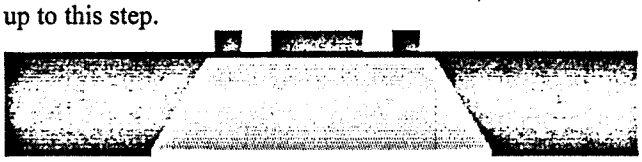

Figure 5: Wafer after Polysilicon Etch

Now the wafers are ready for aluminum deposition. Using the CVC sputtering tool, 5000 Å of aluminum was deposited on the wafer.

Lithography was performed on the aluminum using the resist process described above. The metal level photomask was used with the MA-150. Optical inspection revealed acceptable alignment, and the device was ready for etch. The wafers were etched in aluminum etchant type A, heated to 50 C. Wafers took 3 minutes to clear aluminum in the field areas. Wafers were rinsed for five cycles in the dump rinse, then SRD. Resist was removed with the 4 inch normal ash recipe on the branson asher. The aluminum was sintered using Bruce furnace tube 2. The devices were now ready for test. Figure 6 shows a completed device in cross section.

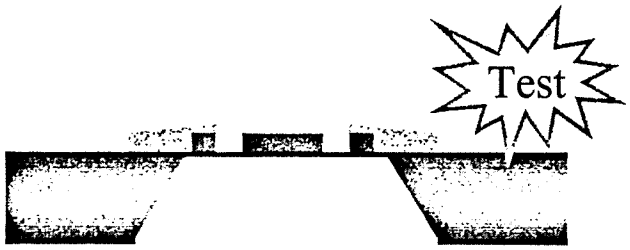

Figure 6: Finished Device Cross Section

B. STS DRIE Bulk Etch Process

For the devices in the center and right column of the mask layout, the STS fabrication process was used. Many of the steps are similar between the two processes but there are a few important differences.

Wafers were double side polished to get better images during the subsequent backside lithography step, as well as to increase nitride uniformity on the wafer backside. Wafers were polished using Levasil 100/45, diluted 2:1 with water. The table RPM was set to 60 RPM, the downforce was set to 6 PSI, the slurry flow was adjusted to about two drips per second, and the wafers were polished

for 20 minutes each. After the polish, both sides of the wafer had equal mirror like shine. An RCA clean was performed next, in order to remove metal ions from the wafer that may contaminate the diffusion furnaces.

Because the STS process is not very selective to nitride, and much more selective to SiO_2 (100:1), the nitride mask was substituted for oxide. An etch this deep using the STS tool had not been performed at RIT before, so in order for the best chance of success, a 2 μm thick oxide mask was grown using tube 2. Recipe 522 was used to deposit the film, which features a 630-minute soak at 1100 C. It was presumed that the oxide mask alone would not hold out long enough to preserve the pattern of the diaphragms all the way through a 480 μm etch, so a new thick resist process was also developed.

ASPR 528 photoresist was selected because of its ability to coat much thicker than standard Shipley 812. A spin speed of 2000 RPM was chosen to give a final resist coating of 4.4 μm. First, the wafer was dehydration baked at 200 C for 2 minutes. The surface is then primed by spin coating 1 drop of HMDS primer for 60 seconds at 2000RPM. An HMDS activation bake of 110 C for 1 minute was then performed. ASPR 528 was then coated at 2000RPM for 1 minute, and baked at 110 C for 5 minutes. The resist requires a much higher dose than conventional resist at this thickness. Dose requirement was on the order of 700 mJ/cm^2, so the wafer was exposed on the MA-150 using the diaphragm level mask for 304 seconds in order to deliver the required energy into the resist. A PEB was done at 110 C for 60 seconds, and the resist was developed in CD-26 positive developer for 1 minute with slight agitation. Because the resist would need to withstand a deep reactive ion etch, it was then sent to a modified hard bake cycle. The wafer was baked at 120 C for 30 minutes, then UV flood exposed for 30 minutes. The wafer was baked again at 200 C for 30 minutes, then UV flood exposed for another 30 minutes. The purpose of these long term, high temperature bakes is to make the resist difficult to remove, in the hope that it will withstand a full two hour etch. BHF was used to etch though two μm of oxide before Si etch in the STS.

The wafer was etched using the STS DRIE for nearly 2 hours to obtain a diaphragm thickness of 10-20 μm. Resist was then removed using 90 C Nanostrip for 30 minutes.

An RCA clean was then performed using the same process described above. With the diaphragms defined and tested for movement, the next stage was the deposition and doping of polysilicon. Using the SMFL standard polysilicon recipe and the six-inch LPCVD tool, 6000Å of polysilicon was deposited. Emulsitone N-250 phosphorus doped glass was used as a dopant, and spun on at 3000 RPM. The wafer was baked for 15 minutes at 200C, then loaded into the N-type diffusion furnace for a doping step. Recipe 120 was used to dope the polysilicon. The recipe features a 1000 C soak for 15 minutes in order to activate the phosphorus from the spin on glass (SOG). The diffusion is followed by a dip in buffered HF for 5 minutes in order to remove the glass layer from the wafer surface. Wafers were rinsed for 5 minutes, then sent to SRD.

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Now the wafers are ready for aluminum deposition. Using the CVC sputtering tool, 5000 Å of aluminum was deposited on the wafer.

Lithography was performed on the aluminum using the resist process described above. The metal level photomask was used with the MA-150.

5. RESULTS

A. KOH Bulk Etch Process

These wafers were processed fully. An important thing to note with these wafers is that during the KOH bulk etch, pinholes in the nitride that occur during handling will begin to etch. This resulted in the wafer becoming very fragile during process. After the Polysilicon deposition, when unloading the wafer, a crack had begun to develop across the wafer inline with the top level of diaphragm. This crack most likely developed due to incorrect care when handling the wafer. Throughout all subsequent processes, the crack widened, but never broke.

During the polysilicon deposition stage as well, an error in the amount of polysilicon deposited was made, and 3000 Å of poly was deposited instead of 6000 Å. The wafers were scrapped and the process started over at that stage.

After the diaphragm etch in KOH, certain resistors and pinholes would etch all the way through. This was initially not a problem, as most devices were still functioning properly. However, during resistor alignment to the backside level, alignment became impossible because the vacuum intended to be drawn between wafer and chuck was now drawn between chuck and mask, with the wafer sandwiched in between. After the first wafer had to be re-done, a solution was found. By cutting a thin film of plastic the size of the chuck, and then taping the wafer to it, the vacuum could be drawn more fully and confined to the wafer. This prevented the wafer mask sticking issue, and alignment could be performed much more easily. This method was used on both the resistor level and metal level alignments.

Devices were tested by applying 5 Volts across two nodes diagonally, and then determining the voltage difference across the other two. Figure 7 shows a diagram of the test setup.

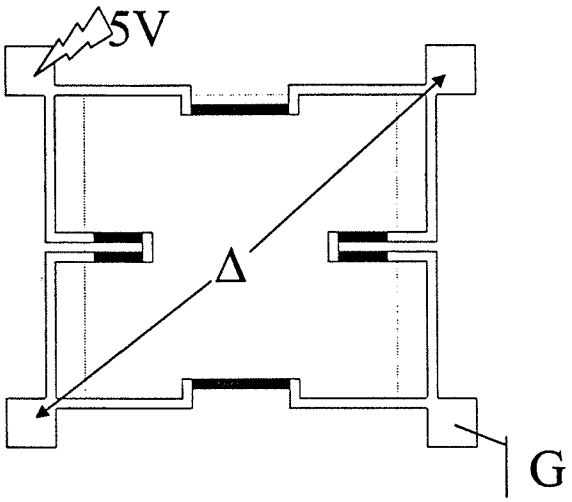

Figure 7: Test Setup

Four probes were place on each device, and while under probe, vacuum of 14.7 PSI was applied using a vacuum chuck. The change in voltage was observed and recorded for each device design, and can be seen in table 1.

Device L/W	No Pressure	14.7 PSI	Δ
4.2	377 mV	378 mV	1 mV
6.2	316 mV	326 mV	10 mV
10	809 mV	848 mV	39 mV
30	2 mV	2 mV	0 mV

Table 1

The device that worked the best was clearly the L/W of 10. Only the last device with L/W of 30 displayed an initially zero voltage as intended. In this device, it is most likely due to overetch of the extremely small resistors designed, and therefore represents a non-working device. The resistors may have been etched laterally during the polysilicon etch. If this were to occur with some non-uniformity in the lateral etch, different resistor sizes would result, which would explain the voltage with zero pressure applied.

The devices still functioned properly, with almost all displaying a voltage shift in the millivolt range with applied pressure.

B. STS DRIE Bulk Etch Process

The STS devices were fabricated after the KOH process had been started. Consequently, they were not finished within the time of the course. Wafers were processed up to the polysilicon deposition, but were unable to be doped and completed.

The STS process has several advantages over the KOH process. The STS wafers took approximately two hours to etch, while a similar etch in KOH took almost 10 hours. In addition, the sidewalls of the diaphragms defined by the STS etch were near vertical, while the KOH process produced the characteristic 54-degree sidewall angle. This meant that the devices for the STS process could potentially have a smaller backside opening, and be smaller in general.

The development of a mask to protect the wafer during etching was a success as well. Prior to this experiment, extended etches had not been performed in the STS. The resist lasted until the very end of the etch and still had to be removed with Nanostrip. The oxide was never exposed to etch conditions. Because of the selectivity the etch had to oxide and photoresist, pinholes did not develop as in the case of the KOH wafer. The wafers were much more durable than their counterpart KOH wafers. In conclusion, the speed, scalability, and increased durability of the STS process make it a more manufacturable process than the KOH process.

6. CONCLUSIONS

Two types of fabrication processes for microelectromechanical pressure sensors were investigated. One process used a KOH bulk etch, while the other utilized a DRIE bulk etch. The KOH process was completed, and finished devices were tested to determine the best functioning design. The devices that functioned best had resistor dimensions of 500 μm by 50 μm, which corresponds to an L/W ratio of 10. The STS DRIE process was started but not completed. Successes of this process include the development of a resist mask able to withstand long etches using in house photoresist and existing equipment. Diaphragms were created with near vertical sidewalls. Both processes show promise, however, the STS DRIE fabricated sensors are more manufacturable due to the speed of the process, increased scalability, and increased durability, resulting in a higher wafer yield.

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