Integration of Low-k Dielectric with Copper

Deoram Persaud
Microelectronic Engineering
Rochester Institute of Technology
Rochester, NY 14623

Abstract-- As VLSI technologies advance, they closely follow Moore's Law where devices are scaled down to smaller dimensions. Their performances, however are limited by the interconnect system. Introducing a low k dielectric material as an inter-metal dielectric brings a major contribution to the device's performance improvement. With the advent of Chemical Mechanical Polishing (CMP), copper has become an ideal metal for interconnect layers. It not only lowers resistance, but also when incorporated with a low k dielectric, it lowers capacitance, thus producing a higher conductivity. Using the environmentally compliant low k dielectric material Flowable Oxide (Fox®-17), which was generously donated by Dow Corning Corporation, these properties were demonstrated. The goal of this study is to, optimize the deposition and curing parameters of Flowable Oxide (Fox®-17) for use in a dual damascene copper process. A stacked film of sputtered tantalum, as the diffusion barrier layer, sputtered copper seed layer and platted copper were deposited and polished to achieve a contact/via connection. A usable dual damascene copper interconnects metallization with low k dielectric constant inter-level dielectric (ILD) for a future integrated circuit device generation was developed.

1. INTRODUCTION

The constant thrust in technology towards increased circuit speeds is leading to devices being scaled to smaller dimensions. Stringent demands are being placed on the performance and reliability of interconnects systems integrated circuits (IC). This has allowed the integration of a lower-k material to continue to be an area for extensive research for the semiconductor industry. A consistent industry-wide focus has been placed on minimizing the permitivity values (k) of new dielectrics. Most of its applications are developed for use in advanced sub-micron IC's interconnect system to increase performance. Interconnect performance improvement requires the reduction of the resistance-capacitance (RC) delay and power consumption. Interconnect RC Delay dominates device performance in determining density, reliability and manufacturing cost.

The purpose of this research was to develop a usable dual damascene copper interconnects metallization, with low k dielectric constant inter-level dielectric (ILD) for a future integrated circuit device generation here in the Microelectronic Engineering facility at Rochester Institute of Technology. The usage of low-k material Flowable Oxide (Fox®-17) was studied extensively, where its permitivity value was tested both optically and with the fabrication of capacitors. Process parameters were optimized for film quality and uniformity. Its coating ability as a function of time and speed as it relates to thickness were determined. Methods of curing, patterning and etching (high etch selectivity) this material were also investigated. Following this extensive understanding of Fox®-17, it was then incorporated with copper in the dual damascene process.

2. THEORY

The following are general statistics that demonstrates the improvements made in RC delay when the switch from aluminum as the main metal to copper was made and when a low-k interlayer dielectric incorporated:

Lower Resistance (1997)

AL ⟶ Cu
Reduces RC Delay by 35%

Lower Capacitance (Today)

SiO_2 (k=4) ⟶ Air (k=1)
Reduces RC Delay by 75%

A. Dielectrics

Dielectrics are materials that are poor conductors of current because all of its electrons are tightly bound to atoms, thus cannot move about freely. The charges within its molecular structure do, however, respond to the presence of an electric field. In the electric field, the positive and negative charges are pulled in opposite directions creating an electrical dipole. The permitivity value (k) of dielectrics ranges form 1 for air up to 100 or more for certain ceramics. They are utilized in capacitors to store charges, thus increasing the efficiency of the capacitor.

Low k interlayer dielectrics play an important role in IC performance by reducing capacitance and cross talk between metal lines. As device generations are scaled into deep submicron feature sizes, low k dielectrics become even more important because they enable higher speed of

operations. Most low-k dielectrics are SiO_2 based that are deposited either by plasma enhanced chemical vapor deposition (PECVD), chemical vapor deposition (CVD) or spin-on.

B. Flowable Oxide (Fox®-17)

Flowable Oxide *(Fox®-17)* is produced and was donated by Dow Corning Corporation. In the flowable oxide family there is exists *Fox®-14* thru *Fox®-25*, the major difference being the respective k values. *Fox®-17* is a Hydrogen Silsesquioxane $(HSiO_{1.5})_n$ material with a low-k constant of 2.75-2.9. It possesses superior planarization, controlled film thickness, excellent gap-fill and low defect density. It is used primarily as an inter-level dielectric material in multilevel metal integrated circuits.

It's a spin-on flowable polymer that when cured becomes a microporous amorphous film. The recommended method of curing is using three hot plates under a nitrogen blanket set at 150°C, 200°C and 350°C respectively for 1minute then baked in a quartz tube furnace for 60 minutes at 400°C also in a N_2 ambient. The purpose of the N_2 ambient is to eliminate CO_2 and water vapor absorption from the environment.

C. Dual Damascene Process

With Chemical Mechanical Planarization (CMP) permitting the use of difficult-to-etch metals such as copper, the very cost effective process of dual damascene took center stage. It is named in honor of its origins as an art used by ancient artisans of Damascus. Dual Damascene facilitates patterning of copper conductors to meet the geometry demands for shorter circuit delays and smaller transistor dimensions. The main advantage of a dual damascene process is that it creates a via/contact connection (2 levels) in one CMP step, while only requiring one etch step and one metal fill. It produces shorter metal lines, allowing for higher density of devices on chip. It also reduces electromigration effects thus improving the reliability of the device.

3. EXPERIMENTAL

The optimized method of coating and curing employed in the application of *Fox®-17* was coating with a spin speed of 4000 rpm for 10 minutes. This time is compromised of a planarization and drying step. The manufacturer recommended method of curing proved to be a challenge at the RIT facility; instead *Fox®-17* was cured in a Heraeus oven for 3 hours. This includes two hours of ramp-up to 400 °C and a soak time for one hour. This was done under a N_2 ambient as recommended by the manufacturer. This method achieved a thickness of 5500Å - 6000 Å.

A. Optical Permitivity Verification

To verify the k value of *Fox®-17* a bare silicon wafer was coated and cured. It was then measured using the ellipsometer with wavelength of 632 nm and 830 nm respectively. Each resulted in a average thickness of 5531Å with refractive index (n) of 1.39. Utilizing these values in the following equation:

$$k = 1 + 4.43\,(n_{632\,nm} - 1) + 0.95\,(n_{632\,nm} - 1)^2$$

$$k = 2.89$$

Equation 1: Calculation of k value

B. Capacitive Permitivity Verification

In verifying the k value for *Fox®-17* capacitors were created on two heavily doped p-type wafers (R = 0.008 – 0.012). Wafer *p1* was coated and cured with 5240 Å of *Fox® – 17* on the bare silicon wafer. On wafer *p2,* 994 Å of dry oxide was grown and then it was coated and cured with 6252 Å of *Fox® – 17.* On both wafers 4116 Å of aluminum was then evaporated using a shadow mask. The front was protected, and the backside was Buffered Oxide Etched (BOE). 5000 Å of aluminum was sputtered, wafers were ashed using acetone and then sintered at 450 C to create ohmic contacts. *(See Figure 1).*

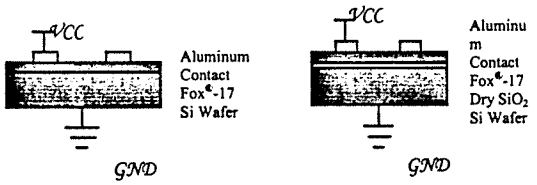
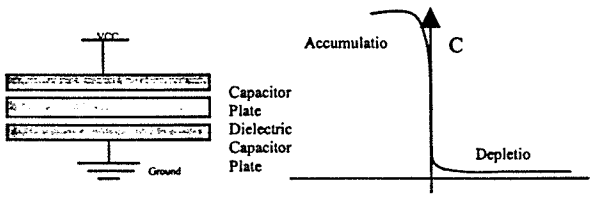


Figure 1: Wafer p1 and Wafer p2 respectively

In using heavily doped p-type wafers, when an electric field is applied and charges begin to accumulate at the capacitor plates, the capacitor will stay in accumulation and not go into the depletion mode. Therefore we have a C-V plot of a horizontal line. *(See Figure 2)*



Typical C-V Plot

Figure 2: Capacitor Characteristics

To determine the theoretical capacitor value assuming the k value of *Fox®-17* is 2.9, the following equation was used:

$$C_{ox'} = \frac{\epsilon_o \epsilon_r}{X_{ox}}$$

Equation 2: Calculation of theoretical capacitor value

ϵ_o = permitivity of free space

ϵ_r = permitivity of *Fox®-17*

X_{ox} = thickness of ILD

With a thickness of 5240 Å of ILD, Cox' = 4.99 nF.

To find the actual k value of *Fox®-17* of wafer p1 the following equation was used:

$$C = \frac{\epsilon_o \epsilon_r \ Area}{X_{ox}}$$

Equation 3: Calculation of actual capacitor value

Area = area of the aluminum contacts

For wafer p2, there are two capacitors in parallel, therefore to find the actual k value the following equation was used:

$$C = \left[\frac{X_{ox}}{\epsilon_o \epsilon_{ox} \ Area}\right] + \left[\frac{X_{Fox®\text{-}17}}{\epsilon_o \epsilon_{Fox®\text{-}17} \ Area}\right]^{-1}$$

Equation 4: Calculation of parallel capacitors

Wafer #	Area (cm^2)	Measured C (nF)	Permitivity (ϵ_r)
p1	0.25	1.5	3.55
p2	0.25	1.2	3.93

Table 1: Permitivity Verification of Fox®-17

B. Dual Damascene Processing

On n-type wafers 12,234 Å of wet field oxide was grown. To serve as a 1st level metal layer, 1778 Å of n^+ polysilicon was deposited and patterned using reactive ion etch (RIE). The poly was doped n-type using spin-on-glass (N-250) (product of Emulsitone Co). The first level of ILD *Fox®-17* was coated and cured using the optimized parameters. To serve as an etch stop a very thin layer of silicon nitride (325 Å) was deposited. This was the patterned, using RIE, to open the via connections. The 2nd level of *Fox®-17* was then coated and cured. To pattern a thick coating of photoresist (ASPR 528) was utilized as an etch mask for the long RIE etch necessary to open contact/via *(See Figure 3).*

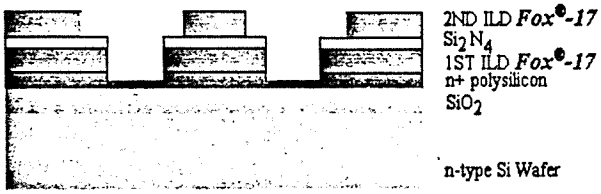
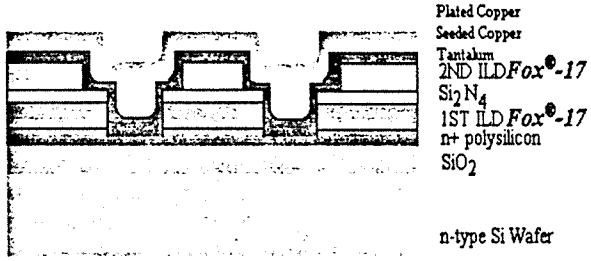


Figure 3: After the 2nd ILD step



A stacked layer of sputtered tantalum for a diffusion barrier layer and copper for a seed layer was deposited. Wafers were then copper platted at the facilities at University of Rochester with the help of Dr. Jacob Jorne. This process fills the contact/via opening. CMP was then utilized to pattern the contact/via connection. The slurry used was of the EKC MicroPlanar™ CMP 9000™ series. A mixture of CMP 9007™ oxidized solution, CMP 9001™ alumina abrasive solution and DI water in a 50% / 25% / 25% respectively was the composition of the slurry. *(See Figure 4 and 5)Figure 4: After the Tantalum, Seeded Cu and Plated Cu process*

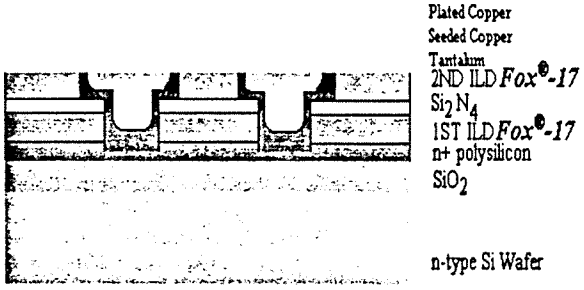


Figure 5: After CMP

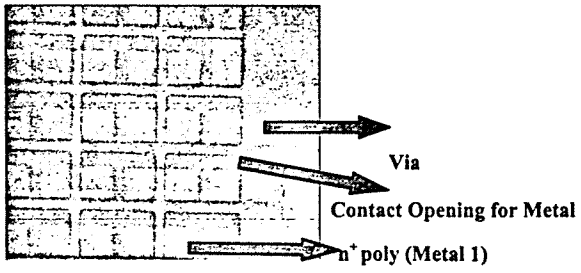
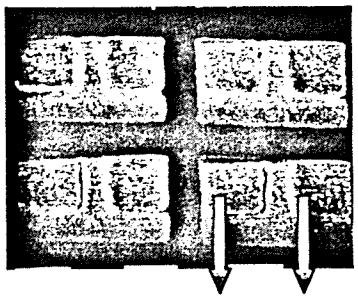


Figure 6: Aerial View of Via chains prior to Metal Deposition



Via after copper

Figure 7: SEM Aerial View of Via Chains

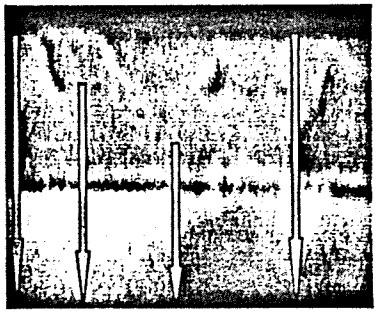


Figure 8: SEM cross-sectional View of Via Chains

4. CONCLUSION

A usable dual damascene copper interconnects metallization with low k dielectric constant inter-level dielectric (ILD) for a future integrated circuit device generation was developed. In the process, a system of coating and curing and the ability to pattern and etch low k dielectric material *Fox®-17* at Rochester Institute of Technology Microelectronic Fabrication facility was developed.

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Deoram Persaud, originally from Guyana, South America, by way of Bronx, NY, received B.S in Microelectronic Engineering from Rochester Institute of Technology in 2002. He attained co-op experience at Motorola Inc.and while doing CMP research under Dr. Richard Lane at RIT. He is actively seeking full time employment in the semiconductor industry as a process or device engineer