

0.5 μ NMOS Devices: Process and Fabrication

Sean Houlihan
Microelectronic Engineering
Rochester Institute of Technology
Rochester, NY 14623

Abstract—

The purpose of this paper is to describe the design and the process used to fabricate NMOS devices. The goal of the experiment was to design and build the smallest NMOS transistor that has been fabricated in the SMLF manufacturing facility. A NMOS transistor is short for n-channel metal oxide silicon field effect transistor (NMOSFET or NMOS). NMOS uses electrons as the majority carrier, a major advantage in terms of device speed. The educational reasons for doing this experiment is to prove the viability of the Canon, being able to complete multi-layer aligning and to increase RIT's ability to process smaller devices.

1. INTRODUCTION

The trend in CMOS technology is to make transistors smaller. Thus making the transistors faster and use smaller voltage supplies. Current industry standers for gate widths are about 0.13-microns or less. This trend is quantified by Moore's law, which says that device density should double every 2 years.

According to Moore's law RIT needs to keep developing new process with small devices. Currently RIT has a working process for 3-micron and 1-micron transistors, but a process that's sub 1 micron needs to be developed. As a first step to improve RIT capabilities, this experiment will give a foundation to design the next generation of RIT process, by processing .5-micron NMOS devices.

Figure 1 shows the expected cross section of an NMOS transistor. The design is a stander transistor with side wall spacers and low doped drains and sources.

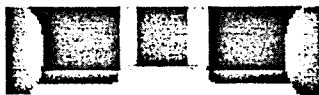


Figure 1

Fig 1 – a drawing of the expected cross-section of the NMOS device

A challenge is designing the process for scaling transistors. At a smaller scale it becomes difficult to image

the small gates and grow the ultra thin oxides. These problems are going to push RIT's equipment to their edge of function ability. The other problem with scaling devices is the increase chance of seeing short channel effects. Some of the short channel effects are punch through, and hot carrier effects. As a result extra process steps have to be put into the process to minimize the short channel effects. Examples of these process steps are low-doped drain, source, and sidewall spaces.

The reason for NMOS devices instead of CMOS devices is simplification. In a ten-week period it is not reasonable to design a complete CMOS process, so a NMOS process will be developed. Not only will a process be developed, but also devices will be fabricated and tested. The tested results will take the form of gate width measurements and various electrical testing.

2. FABRICATION PROCESS AND MASK LAYOUT

To achieve this goal a few new process improvements or changes will have to be made to the RIT standard Sub-CMOS process. New doping concentrations have to be calculated to minimize the size of the space charge layer. Also the gate oxide process has to be enhanced to grow a thinner gate dielectric. A thinner gate dielectric is needed to invert the channel. These are just a few of the changes that will be made. Four mask levels will be needed to achieve this goal.

The Mask contains two rows of transistors, the 1st row has scaled gate widths and the 2nd row contains fully scaled devices. The mask layout was designed specifically for this process, the masks where fabricated in RIT Mask shop. An image of the mask layout can be found on the next page labeled figure 2.

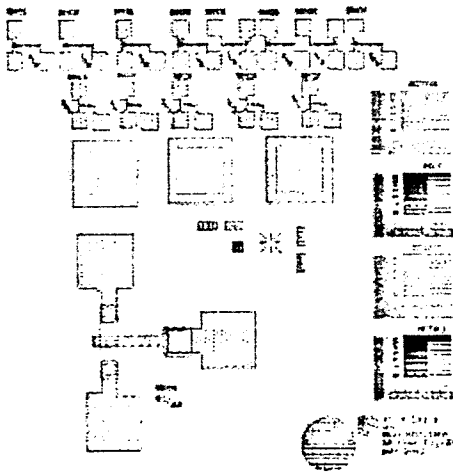


Figure 2

Fig 2. - the image of the mask layout used during the fabrication process

The fabrication process I used to fabricate the NMOS devices can be found below. I started with p-type wafers and my well concentration was $1E17 \text{ cm}^{-3}$.

1. Implant the entire wafer to create the P type well
2. Well drive
3. Oxide etch
4. Clean (RCA)
5. Pad oxide
6. CVD Nitride
7. Photo → Active
8. Etch Nitride
9. Strip Photoresist
10. Implant the Well Stop
11. Clean (RCA)
12. Field Oxide growth
13. Etch nitride
14. Etch pad oxide
15. RCA clean
16. Oxide → Gate 100Å
17. CVD Poly
18. Dope the poly Si → using solid source diffusion
19. Photo → poly
20. Etch poly to gate oxide → using the Drytek factor recipe
21. Strip resist
22. Ion implant low doped drain
23. Clean RCA
24. CVD → LTO
25. Anneal
26. Etch
27. Ion implant Drain and Source
28. Anneal
29. CVD → LTO
30. Photo → Contact Cuts
31. Etch LTO
32. Strip resist
33. Clean (RCA)
34. Deposit metal
35. Photo → metal
36. Etch metal
37. Strip photoresist
38. Sinter
39. Test

3. IN-PROCESS RESULTS

A four-point probe test was done after the well drive to verify that the doping concentration of the well was indeed $1e17 \text{ cm}^{-3}$. Figure 3 and 4 show images of active regions on a die. Figure 3 shows an image of the active region after the first lithography step. Figure 4 shows the same region but this time it's after the field oxide growth.

Figure 3

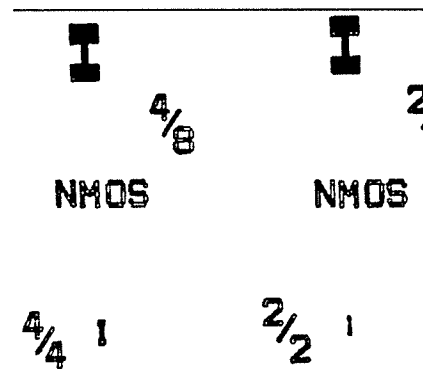


Fig 3 - shows an image of the active region after the first lithography step

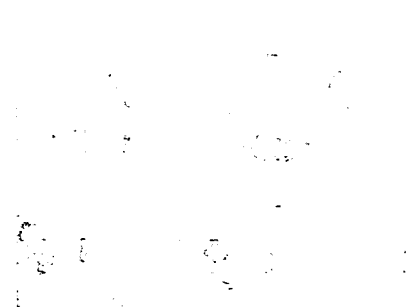


Figure 4

Fig 4 - shows the same region but this time it's after the field oxide growth

Do to problems outside my control the wafers were processed through the gate oxide step. The rest of the process was simulated for verification of tool settings.

4. RESULTS AND DISCUSSION

My results from this experiment can be summed up in a list of accomplishment. These accomplishments are stepping-stones to the completion of the NMOS devices.

- 0.5 μ m NMOS Fabrication process was designed and simulated
- Masks Layouts were designed and fabricated
- Wafers were processed through the gate oxide step
- Device electrical tests were designed

With this work accomplished I plan to finish the devices, the work done and the simulation work all leads to conclusion that I will fabricate the smallest NMOS device at RIT.

5. CONCLUSION

- Process device simulations gave expected dopings and thickness
- Device test is expected to show working 0.5 μ m NMOS

REFERENCES

- [1] W.PAIK, et al., VLSITSA, PP39-42, 1991
- [2] B. Min, et al., IDEM Tech. Dig., pp8730876
- [3] L. Fuller, "The Short Channel MOSFET", Class notes, 2001
- [4] I. Puchades, "Sub CMOS-Process", MS Thesis, 2000
- [5] L. Fuller, "Advanced CMOS Process Technology", Class notes, 2001

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Sean Houlihan, Woodbury, CT, received B.S in Microelectronic Engineering from Rochester Institute of Technology in 2002. He attained co-op work experience at Veeco Instruments and CVC. He is attending Graduate School in Electrical Engineering at RIT Starting in the fall of 2002