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III-Nitride Nanowire Deep-Ultraviolet Light Emitting Diodes

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RIT

III-Nitride Nanowire Deep-Ultraviolet Light Emitting Diodes

by

Bryan Melanson

A dissertation submitted in partial fulfillment of the requirements
for the degree of Doctor of Philosophy in Microsystems Engineering

Microsystems Engineering Program
Kate Gleason College of Engineering

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ABSTRACT

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Deep-Ultraviolet (DUV) Light Emitting Diodes (LEDs) emitting invisible light at wavelengths below 280 nm, have seen increased research interest over the last decade. Of their many potential applications, pathogen neutralization is perhaps the most presently relevant in the post-COVID era. While the high energy light of DUV LEDs has been found particularly effective at destroying viruses and bacteria without the need for application of chemical agents, the poor efficiencies of DUV LEDs currently prevent their widespread adoption in these applications. While a number of factors contribute to the poor efficiency of DUV LEDs, light extraction is perhaps the most significant and difficult to address. The polarization of light emitted by DUV LEDs make it difficult to extract from the conventional "mesa" structures which form the overwhelming majority of LEDs. An alternative to mesas is to use arrays of closely spaced nano- or micro-structures connected in parallel, which have been shown both experimentally and by simulations to have significantly enhanced light extraction efficiency.

In this work, the feasibility of using plasma etched arrays of nano- and micro-structures as alternatives to conventional mesa structures for emission of DUV light is investigated. New techniques for fabricating nanowire and micropillar array LEDs are developed, and a novel "inverse taper" crystallographic wet etch phenomenon which occurs in high Al-content AlGaN is discovered, described, and leveraged in device fabrication. The first reported demonstration of dry-etched, electrically driven, DUV emitting nanowire array LEDs is described in detail, in addition to the first demonstration of DUV emitting micro-LEDs based a novel AlGaN-delta-GaN active region previously designed by our research group.

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CHAPTER 1: Introduction to Deep-Ultraviolet LEDs

1.1 Light Emitting Diodes

Light Emitting Diodes (LEDs) have emerged over the past few decades as integral components of modern technologies, and can be found in almost every application imaginable. Their compactness, efficiency, and long lifespan makes them perfect replacements for incandescent and fluorescent light sources, and advancements in LED manufacturing technology have gradually made them cheap enough to replace these more conventional light sources in bulk lighting applications in the industrial, commercial, and residential sectors. Recent reports by the United States Department of Energy (DOE) estimate that LEDs will account for more than 84% of all lighting installations in the United States by 2035, saving nearly $1 trillion USD per year in energy costs [1]. As such, continued development of LED technologies, in particular the improvement of LED efficiencies over a wide range of emission wavelengths is of critical importance to the energy security of the United States and the world as a whole, and will also be a crucial tool for reducing energy consumption and combating the effects of climate change.

1.1.1 *History*

Electrically driven solid-state light emission was first observed in the early twentieth century, and was termed "electroluminescence," which, in contrast to incandescence (also known as heat glow) is defined as the emission of light by a material at room temperature when subjected to an external electrical bias [2]. Electroluminescence was first observed by Henry Joseph Round in 1907 while investigated SiC crystals for use in early crystal-detector radios [3]. Development of the first SiC LED was reported in 1928

by Oleg Lossev [4], but it was not until the late 1960s that advancements in SiC fabrication allowed for p-n junction blue LEDs emitting around 470 nm to be produced [2]. Over the next few decades SiC LEDs were gradually phased out of commercial use due to severe efficiency limitations produced by SiC's indirect bandgap. During the 1950s and 1960s, GaAs, AlGaAs, and GaAsP, were investigated and developed for use in longer wavelength light emitters with much higher efficiencies, with the first red emitting LED based on AlGaAs developed in 1962 [2]. Blue light emission from GaN was first reported in 1971 by Pankove *et al.,* with GaN and InGaN based LEDs further refined by Nobel laureate Nakamura *et al.* in 1993, allowing for extremely high brightness, high efficiency emission of blue and green light from this materials system [2,5,6]. AlInGaP was first developed in the 1980s for use in visible light lasers, but was later adapted for use in high efficiency, red emitting LEDs [2]. Today, state of the art light emitting diodes are based on AlInGaN alloys for ultraviolet, blue, and green emission, and AlInGaP alloys for red and infrared emission, with modern advancements in LED technology being mostly incremental and driven by improvements in material quality, light extraction efficiency, and active region design.

1.1.2 Fundamentals

Light Emitting Diodes operate on a phenomenon known as "recombination," in which a free electron within a semiconductor crystal relaxes from an "excited" energy state to a lower energy state, emitting a photon of energy equal to the energy difference between the excited state and relaxed state. In semiconductor device physics this process is typically described in terms of electron and "hole" recombination, where a hole is the localized absence of an electron with the valence band of a semiconductor. In a semiconductor at

equilibrium, all available states in the valence band are filled by electrons, however, electrons can be excited to states above the valence band, in the so called “conduction band” through absorption of thermal, optical, or kinetic energy. Heating of a semiconductor to very high temperatures can cause electrons in the valence band to absorb enough thermal energy to be “excited” in the unoccupied states in the conduction band, where they are unbound from the nuclei of the atomic lattice, and can participate in conduction, hence the name “conduction band.” Likewise, when a semiconductor is exposed to an external light source, electrons in the valence band can absorb incident photons and, if the energy of the absorbed photon is greater than the bandgap (E_g) (the energy separation between the edges of the valence and conduction bands) of the semiconductor, can be excited into the conduction band. Excitation to the conduction band can also occur if an electron absorbs sufficient kinetic energy from an impactor, such as another electron or ion.

Figure 1.1.1 shows the alignment of the conduction bands (CB) and valence bands (VB) for a metal (left), a semiconductor (middle), and an insulator (right). A material’s classification as a metal, semiconductor, or insulator is entirely dependent upon its bandgap, or lack thereof. In metals, the conduction and valence bands overlap, giving the bandgap a value of $E_g = 0$ eV, and as a consequence the valence electrons in metals can participate in conduction, being only loosely bound to local atomic lattice sites. In a semiconductor, a small bandgap exists between the edges of the conduction and valence bands. In an insulator, the bandgap is much larger, effectively preventing any excitation of electrons into the conduction band except by very high temperatures or very high energy photons. The distinction between semiconductors and insulators is hazy, but

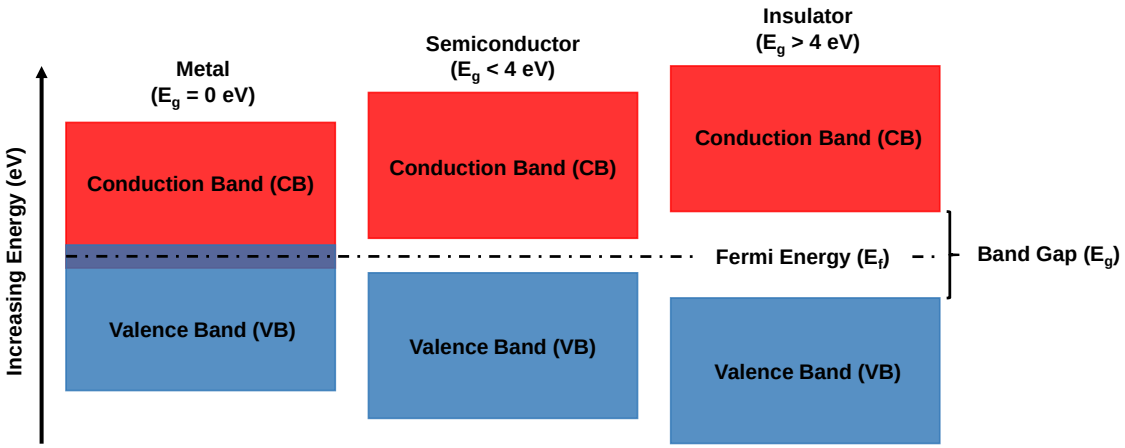

Figure 1.1.1: Conduction (CB) and valence (VB) band alignments for metals, semiconductors, and insulators.

semiconductors are generally defined as having bandgaps of $E_g < 4$ eV, with any material of $E_g > 4$ eV being classed as an insulator.

When an electron is excited to the conduction band, it leaves behind a "hole" in the valence band, a quasi-particle with no physical mass which exists as a consequence of unscreened nuclear charge. In most cases, excited electrons will rapidly relax back into the valence band in what is termed electron-hole recombination. In this process, the electron loses potential energy, recombining with and annihilating a hole and emitting light in the process. It is important to note that light emission only occurs during electron-hole recombination in semiconductors with a "direct-bandgap." In direct-bandgap semiconductors the conduction band minimum (E_c) and valence band maximum (E_v) are not separated in *k*-space, allowing electrons to recombine into the valence band without a change in momentum. In "indirect-bandgap" semiconductors, E_c and E_v are not aligned in *k*-space, and recombination involves a change in momentum is what is referred to a "phonon-assisted" electron-hole recombination. Whether a semiconductor is direct- or

indirect-bandgap ultimately determines its usefulness as a light emitter, with indirect bandgap semiconductors such as Si and Ge being incapable of emitting light, while direct-bandgap semiconductors such as GaN and GaAs see widespread use in lasers, LEDs, and photodetectors. More information on electron-hole recombination in LEDs can be found in *Light-Emitting Diodes* Chapter 2 [2].

The most useful property of semiconductors, and the one which allows them to be used to fabricate transistors, LEDs, lasers, and other electrically driven devices, is doping, or the ability to change the majority charge carrier through inclusion of impurities in the crystal lattice. In a semiconductor, a dopant impurity acts as either a donor or acceptor depending on its valence number. In silicon, with a valence of four, boron, with a valence of three, will act as an electron acceptor, substituting for a Si atom in the crystal lattice and becoming a negatively charged lattice site, while creating a mobile hole which can participate in conduction. Likewise, phosphorus, with a valence of five, will act as an electron donor, substituting for a Si atom in the crystal lattice and becoming a positively charged lattice site, while creating a mobile electron which can participate in conduction. By controlling the type and concentration of impurities in a semiconductor, it is possible to change the majority charge carrier responsible for conduction and flow of electric charge in the material while also drastically increasing the concentration of charge carriers available to participate in conduction. Un-doped semiconductors are referred to as "intrinsic," with only the naturally occurring free electrons and holes being available to participate in conduction. Intrinsic semiconductors generally have very high resistivity because the concentrations of mobile charges carriers are very low, and behave much like insulators from an electrical perspective. Doped semiconductors are referred to as

"extrinsic," because the majority of their mobile charge carriers, either electrons or holes, are contributed by dopant atoms. High dopant concentrations can lead to multiple order of magnitude improvements in free charge concentration within a semiconductor, massively reducing its resistivity and causing it to behave more like a metal from an electrical perspective. If a semiconductor is doped primarily with electron acceptors, it is termed a p-type material, while if it is doped primarily with electron donors, it is termed an n-type material. In p-type semiconductors, holes are the majority charge carrier, and although holes have no physical mass, they do have what is referred to as "hole effective mass" (μ_h) which is a description of how they interact with, and move within, the crystal lattice. In n-type semiconductors, electrons are the majority charge carrier, and behave according to the electron effective mass (μ_e) of the material. The effective masses of electrons and holes is different for all semiconductors, and plays a crucial role in determining their conductivity/resistivity. More information on semiconductor doping can be found in *Silicon VLSI Technology* Chapter 1 [7].

Any direct-gap semiconductor is generally capable of emitting light through electron-hole recombination when excited by either high energy photons (photoluminescence (PL)), incident electrons or ions (cathodoluminescence (CL)), or an electric current (electroluminescence (EL)). However, a device which requires high energy light or an electron/ion beam to itself emit light is of very limited practical usefulness. Light emitting diodes are, by definition, semiconductor devices which emit light through electroluminescence, in which electrons and holes are injected into the semiconductor from an external current source and recombine within it to emit light. While it is possible of any bulk, un-doped direct-gap semiconductor to emit light when subjected to high enough

applied voltage and current density, this process is very inefficient. As such, more complex engineering approaches based on "PN-diodes" are needed to fabricate high efficiency LEDs. In a light-emitting PN-diode, positive bias is applied to a region of p-type semiconductor, while negative bias/ground is applied to an n-type region. Because each of these regions has a majority charge carrier, it is difficult for electron-hole recombination to occur in them due to a lack of minority charge carriers. For example, in the n-type region there are many majority carrier electrons, but very few minority carrier holes, so it is rare for electron hole recombination to occur. This allows the n- and p-type regions to be used to "funnel," in a sense, the majority charge carriers in each region toward the junction between the regions, as can be seen in Figure 1.1.2. When the majority charge carriers reach the junction, they are finally able to recombine with one another. The physics of PN-junctions is much more complex than has been explained here, but is beyond the scope of this explanation. More information on the physics of PN-junctions and their use in transistors and other electrical devices can be found in *Microelectronics* Chapter 1 [8].

While fabrication of LEDs using simple PN-junctions is possible, most modern LEDs rely on structures known as "quantum wells" (QWs) to confine recombination to certain regions and determine their emission wavelength. In a simple QW LED, a thin layer of un-doped lower bandgap material is sandwiched between two "barrier" layers of higher bandgap, with one side being p-doped and the other n-doped, as can be seen in Figure 1.1.2. Holes are supplied into the QW from the p-doped side, while electrons are supplied from the n-doped side. Under normal operation, electrons and holes occupy the quantum well at the same time, recombining from their respective ground states in the quantum well to produce light, as is shown in Figure 1.1.2. The advantage of using a quantum

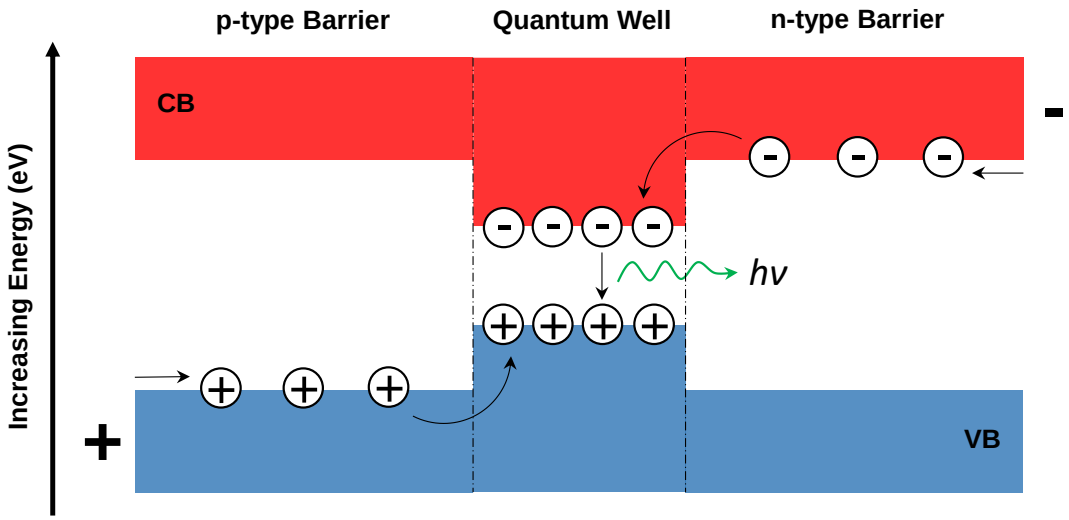

Figure 1.1.2: Electron-hole recombination in a generic PN quantum well. Band bending is not shown for simplicity.

rather than a PN-junction is that recombination is confined almost entirely to the region of the quantum well, which allows the emission wavelength to be tuned very precisely through variation of the alloy composition/bandgap of the QW region. Modern high-performance LEDs utilize multiple quantum wells (MQWs) to increase the volume in which recombination occurs and allow efficient operation at higher current densities.

Modern LEDs are typically fabricated starting with epitaxial growth of single-crystalline layers of doped semiconductor on a substrate wafer. The vast majority of LEDs manufactured in 2021 are based on the GaN/InGaN materials system. In the case of GaN/InGaN LEDs, which generally emit between 365 nm and 600 nm, metal-organic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE) is used to grow layers of GaN and InGaN on a sapphire, SiC, or Si substrate wafer anywhere from 50 to 200 mm in diameter at higher temperature. Doping of various layers is accomplished during the growth process, negating the need for external doping methods used in

fabrication of Si-based microelectronics. Growth generally consists of an AlN buffer layer grown on the substrate, followed by growth of several microns of n-doped GaN (n-GaN), a MQW active region consisting of alternating GaN barrier layers and InGaN QWs, several hundred nanometers of p-doped GaN (p-GaN), and a few dozen nanometers of p^+-doped GaN (p^+-GaN), as can be seen in Figure 1.1.3. Following growth of this "epistack," a photolithography and a plasma dry etch are used to pattern and etch features called mesas, with the etch terminating within the n-GaN layer. Metal contacts are then deposited, with the p-contact located on top of the mesa in contact with the p^+-GaN surface, and the n-contact located on the n-GaN surface exposed by the dry etch as shown in Figure 1.1.3. The wafer is then diced to produce many small LED "die," generally between 100 µm and 2 mm on a side, and the die are "packaged" to allow them to be used in a wide range of applications. Packaging usually consists of mounting the die to a small printed circuit board

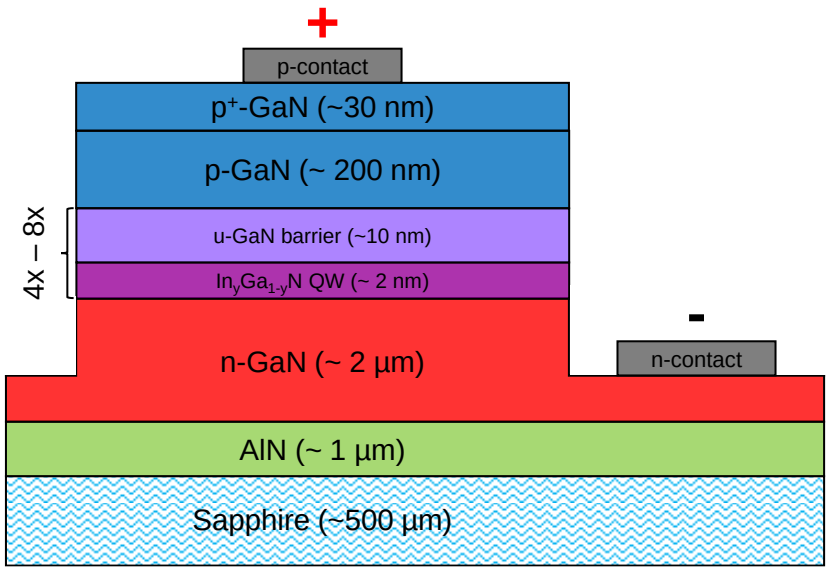

Figure 1.1.3: Representative structure of modern blue LED. Layer thicknesses are approximate and shown layer thicknesses are not to scale.

(PCB), making electrical connections between the PCB and the metal contacts on the die, and finally encapsulating the LED is a transparent material to protect it from the environment and increase light extraction.

1.1.3 Efficiencies

As with any modern electrical device, efficiency is a key consideration during the design and fabrication of LEDs. With LEDs becoming increasingly dominant in high power applications such as area lighting, even an increase of a few percent in device efficiency is worth extensive research and development costs. LEDs are most commonly characterized in terms of their external quantum efficiency, or EQE, which is a ratio of the number of electrons injected into a device to the number of photons which are emitted into free space. Wall-plug efficiency (WPE), also called the radiant efficiency, is another commonly used term, and is a ratio of the radiant flux of an LED to the electrical input power. WPE can be determined by multiplying the EQE of the LED by its "feeding efficiency," which is itself a ratio of the average photon energy to the energy imparted to a charge carrier pair by the LEDs power source. While both EQE and WPE are often used when quantifying the overall efficiency of an LED, other, more specific terms are needed to determine the location(s) of efficiency so that the design of the LED can be improved [2]. EQE is commonly defined as the product of three components, the carrier injection efficiency (η_{INJ}), radiative recombination efficiency (η_{RAD}), and light extraction efficiency (η_{EXT}). It is also common for η_{INJ} and η_{RAD} to be combined into a term called "internal quantum efficiency" or IQE, with EQE then being the product of IQE and η_{EXT}.

1.1.3.1 Carrier Injection Efficiency (η_{INJ})

η_{INJ} quantifies the ratio of charge carriers injected into the device at the n- and p-contacts to the number of charge carriers which successfully make it to the active region for recombination. η_{INJ} is lowered by a number of phenomena, including thermal losses due to contact and series resistance, recombination of carriers in the bulk region of the LEDs, surface recombination, and trapping of charge carriers at defect sites. In general, η_{INJ} can be improved through optimization of the electrical contacts, reduction of crystal defects and general improvement of the growth process, and passivation of exposed surfaces to reduce surface recombination [2].

1.1.3.2 Radiative Recombination Efficiency (η_{RAD})

Once electrons and holes reach the active region, the ratio of recombination events which result in emission of a photon of energy E_g is given by η_{RAD}. While radiative recombination is much more likely to occur in the active region compared to the bulk regions of the LED, non-radiative recombination can still occur, lowering the η_{INJ} of the LED. In the active region, electron-hole recombination can occur via three primary mechanisms, as shown in Figure 1.1.4. The first is trap-assisted non-radiative recombination, a type of Shockley-Read-Hall (SRH) recombination, in which an electron relaxes to a "trap" state (E_T) within the bandgap of the QW, and then relaxes again from that trap state to the valence band to recombine with a hole. This process occurs more frequently in materials with high defect density in which many trap states exist [2]. The time dependent dynamics of carrier recombination in the quantum well (as well as in the bulk regions) are governed by a property know as carrier lifetime (τ). The radiative carrier lifetime, τ_R, determines the average time taken for a carrier to experience radiative

recombination within the quantum well, while the non-radiative carrier lifetime, τ_{NR}, determines the average time taken for a carrier to experience non-radiative recombination, usually via a trap state. As such, η_{RAD} can be increased by increasing τ_{NR} or by decreasing τ_R, and can be estimated using equation 1.1.1. In SRH trap assisted non-radiative

$$\eta_{RAD} = \frac{\tau_R^{-1}}{\tau_R^{-1} + \tau_{NR}^{-1}} \tag{1.1.1}$$

recombination, the effectiveness of a trap state as a non-radiative recombination center is dictated by its position within the bandgap. Deep-level traps (DLTs) located near the middle of the bandgap are more effective recombination centers, and as such, high concentrations of DLTs generally reduce τ_{NR}, thus reducing η_{RAD}, making reduction of DLT density during the growth process critical for achieving high radiative recombination efficiency. Temperature also has a strong impact on η_{RAD}. As τ_{NR} is correlated inversely with temperature, increasing temperature in the active region will decrease η_{RAD}. By cooling as semiconductor to cryogenic (liquid nitrogen or helium temperatures) trap states can be "frozen out" as τ_{NR} is exponentially increased, allowing for realization of the highest achievable values for η_{RAD}. Carrier lifetimes in LEDs are usually measured using a technique known as cryogenic time-resolved photoluminescence (cryo-TRPL), in which carrier pairs in cryogenically cooled samples are excited by rapid pulses of light with energy greater than the active region bandgap. By analyzing the photoluminescence decay curve recorded by a spectrometer, τ_R and τ_{NR} can be extracted.

The second mechanism is Auger recombination, in which the energy released during relaxation of an electron to the valence band is dissipated through excitation of an electron high into the conduction band or excitation of a hole deep into the valence band as can be seen in Figure 1.1.4. The excited carriers eventually lose their excess energy

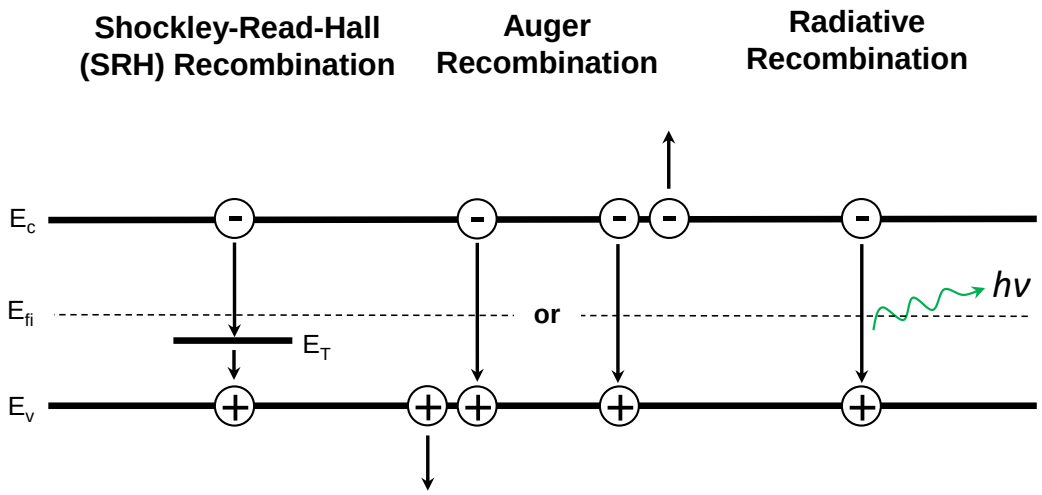

Figure 1.1.4: The three primary electron-hole recombination mechanisms likely to occur within the quantum wells of LEDs.

through emission of phonons while relaxing back to their ground states near the conduction or valence band edges. This process is non-radiative as well, and becomes more dominant at higher carrier densities due to a rate dependence on the cube of carrier density. While an ideal QW is un-doped, there is rarely parity between the concentrations of electrons and holes injected from either side of the QW region due to differences in the n- and p-dopant activation energies, carrier mobilities, and other factors. In GaN for example, Mg, with a large activation energy, is used as a p-dopant, and as such fewer holes are injected into GaN/InGaN QWs than electrons, leading to conditions where Auger recombination usually results in excitation of electrons above conduction band edge due to electrons being much more numerous in the QW [2].

The third, desired mechanism, is radiative recombination, in which an electron from the conduction band recombines directly with a hole in the valence band, emitting a photon with energy equal to the difference between the conduction band and valence band ground states. A high recombination rate is desired in all LEDs, and extensive research into

maximizing it has been conducted over the past several decades. In general, the radiative recombination rate is dependent upon the concentrations of electrons and holes within the QW, as well as upon a constant called the bimolecular recombination coefficient, which varies between materials.

1.1.3.3 Light Extraction Efficiency (η_{EXT})

The third component of EQE is light extraction efficiency, or η_{EXT}, which is a simple ratio of the number of photons which escape the LED structure into free space to the total number of photons emitted from the active region. Figure 1.1.5 shows 10 photons emitted from a simplified LED structure. Orange lines terminating in arrows represent photons which escape into free space, while lines terminating in X's represent photons which are reabsorbed by the structure. In this example, 6/10 of the photons are reabsorbed, while 4/10 escape, giving the LED in Figure 1.1.5 an extraction efficiency of η_{EXT} = 40%.

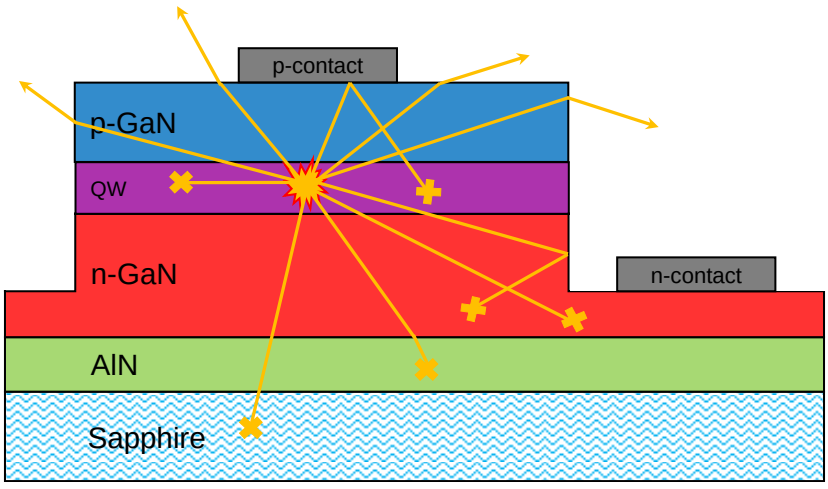

Figure 1.1.5: Light extraction from a simplified LED structure. Ten photons are emitted from a point-source in the center of the active region, with lines terminating in arrows representing escaping photons, and lines terminating in X's representing photons reabsorbed by the structure.

Light extraction efficiency is influenced by a number of parameters, including the polarization of emitted light, indices of refraction of the materials composing the LED, roughness of exterior surfaces and interior material interfaces, substrate composition and patterning (or lack thereof), and size and reflectivity of metal contacts. Light extraction efficiencies of state-of-the-art blue LEDs are currently approaching 90%, while shorter wavelength ultraviolet LEDs and longer wavelength red LEDs tend to have much poorer extraction efficiencies. Research aimed at improving the η_{EXT} of longer and shorter wavelengths has intensified in recent years, as demand for native red emitters and deep-ultraviolet (DUV) LEDs grows.

1.2 Ultraviolet Light

Ultraviolet (UV) light is typically defined as having wavelengths between 100 and 400 nm. As shorter wavelengths correspond to higher photon energy, many UV wavelengths are harmful to humans and other organism due to the ability of high energy photons to sever DNA base pairs and cause other damage to cells. UV light can be divided into four emission regimes, UV-A (315-400 nm), UV-B (280-315 nm), UV-C (200-280 nm), and vacuum-UV (V-UV) (100-200 nm), as shown in Figure 1.2.1. Some debate exists on whether wavelengths below 100 nm should be classified as extreme-UV (EUV) or soft x-rays, with most physics fields referring to < 100 nm as soft x-ray while semiconductor engineers generally use the term EUV. Exposure to UV-A and UV-B wavelengths is very common, with low UV-A and UV-B intensities present in sunlight at the earth's surface. UV-A represents around 3% of sunlight reaching the earth's surface, and around 90% of UV light which reaches the earth's surface, due mostly to its longer wavelengths experiencing less absorption in the atmosphere than shorter UV-B

wavelengths [9]. In humans, and most organisms, UV-A wavelengths penetrate further into the skin, and are responsible for acceleration of aging effects such as dermal discoloration wrinkling [9]. UV-B on the other hand, is absorbed almost immediately after impinging on skin, and is primarily responsible for more serious damage leading to skin cancers.

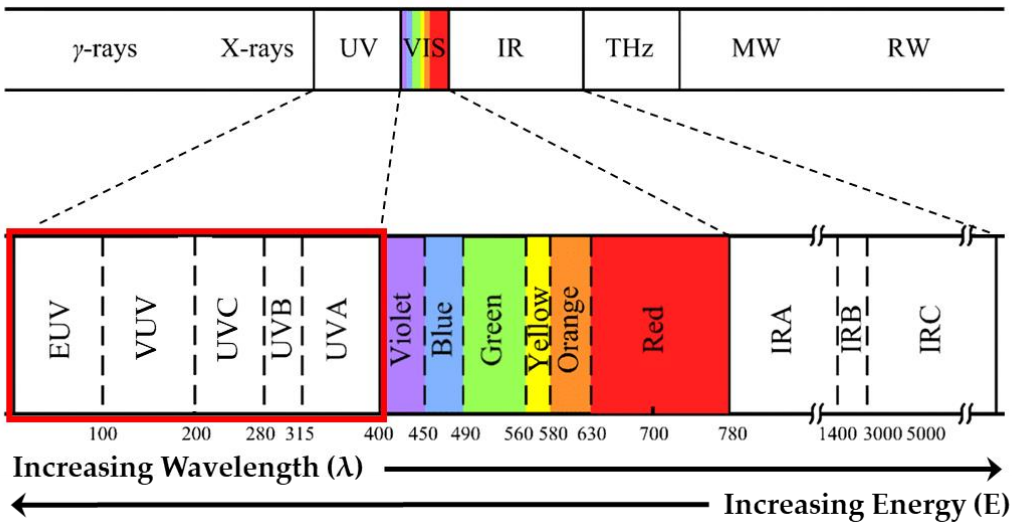

Figure 1.2.1: Electromagnetic spectrum between 10 and 1000 nm, showing the wavelength ranges of V-UV, UV-C, UV-B, and UV-A light.

While UV-B light is blocked almost entirely by window glass and sunscreen, longer wavelength UV-A light penetrates window glass and is unaffected by many traditional sunscreens [9]. UV-C, also referred to as deep-ultraviolet (DUV) light has been shown to have acute side effects in humans, causing near-instantaneous burns to the skin and eyes at higher intensities. The shorter wavelengths of UV-C light mean that it cannot penetrate deeply into skin, and is therefore less likely than UV-B to cause cancer. While most damage caused by UV-C light is temporary, exposure to high intensities can cause permanent blindness [9]. Human exposure to UV-C wavelengths is extremely rare, as all solar UV-C

radiation is absorbed by the earth's ozone layer. Exposure to UV-C light is attributed to artificial sources, such as tanning booths, mercury lamps, lasers, and other light sources.

The shortest wavelength, highest energy UV light (not accounting for EUV), is V-UV with wavelengths between 100-200 nm placing it on the upper edge of the x-ray spectrum. V-UV light is extremely hazardous to humans, causing painful burns and temporary blindness near instantaneously even at low exposure intensities [10]. V-UV photon energy is also high enough to permanently damage synthetic materials such as silicone rubbers and other plastics over the span of days or weeks [11]. The name 'vacuum-UV" derives from the fact that V-UV radiation is found almost exclusively in the vacuum of space, as it is aggressively absorbed by oxygen molecules in Earth's atmosphere. While V-UV radiation is rarely a threat to humans, its presence is space and ability to damage synthetic materials means it must be taken into consideration when designing components for spacecraft and satellites.

1.3 Applications of Ultraviolet Light

Despite the hazards of UV light to humans and other organisms, it sees widespread use in many different applications, from remote sensing to pathogen neutralization. UV light has been used for over 100 years to treat various medical conditions in humans, and until the invention of the UV LED several decades ago, mercury vapor arc lamps were the sole source of ultraviolet light [12]. Today, mercury lamps remain the dominant source of UV light for most applications, although improvements in the efficiencies of semiconductor-based UV LEDs and lasers are allowing them to gain traction in many applications. Common uses of UV-A wavelengths include curing of adhesives and resins,

3D-printing, optical sensing, g-, h-, and i-line lithography, and medical uses such as blood gas analysis [13]. UV-B wavelengths generally see use in indoor, artificial plant lighting in greenhouses and hydroponics gardens, as well as in medical treatments and tanning [13]. UV-C/DUV wavelengths are often referred to as "germicidal" UV, and see extensive use in applications such as water purification and surface sterilization due to the ability of high energy UV-C photons to penetrate the cell walls of microorganisms and destroy their DNA [13–15]. This beneficial property of UV-C light is currently driving its implementation in a multitude of applications such as wastewater recycling, kitchen appliances, air conditioning, and sterilization of foods and medical equipment [13]. Room-scale disinfection using UV-C light has also gained traction in the wake of the COVID-19

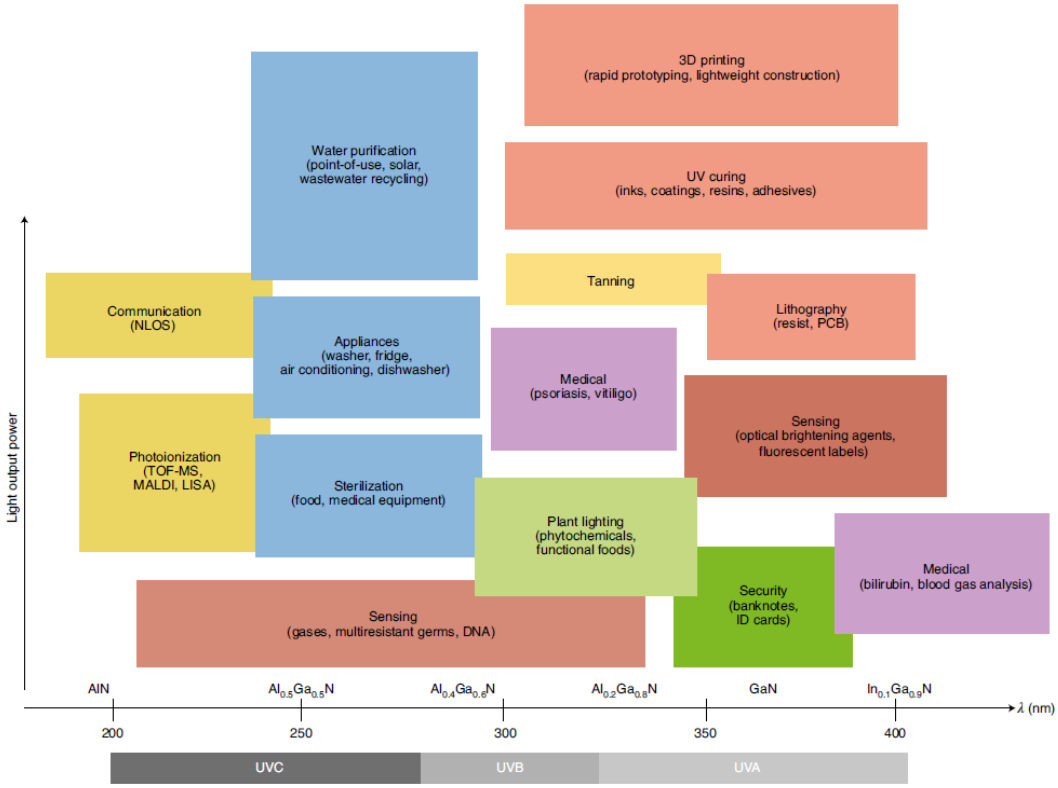

Figure 1.3.1: Applications of ultraviolet light categorized by wavelength and output power. Reprinted with permission [13].

pandemic, with airlines, transportation services, and hospitals experimenting with use of high-power UV-C light sources for sterilizing the interiors of planes, buses, trains, and hospital rooms. In addition to its germicidal applications, UV-C light also sees use in various sensing applications such as solar blind photodetectors and cutting-edge excimer laser photolithography [13,16]. As the efficiencies of UV LEDs continue to improve, most applications will slowly transition away from using mercury lamps, leading to the eventual domination of the market by UV LEDs.

1.4 The AlGaN Materials System

Ultraviolet light emission requires the use of ultra-wide bandgap (UWBG) materials, such as AlGaN, ß-Ga_2O_3, ZnO, and diamond [17,18] . However, most research on UV-LEDs is based exclusively on the ternary (three element) AlGaN materials system, a subset of the larger, quaternary AlGaInN system, as shown in Figure 1.4.1. AlGaN is a ternary alloy of binary (two element) AlN and GaN, and its direct bandgap can be tuned between that of AlN (~6 eV/200 nm) and GaN (~3.4 eV/365 nm) [2,13]. This allows AlGaN LEDs to cover the entirely of the UV-C and UV-B ranges, as well as the majority of the UV-A range through engineering of the Al content of the active region. Adding In to form a quaternary AlGaInN (four element) alloy allows this materials system to cover the entirety of the UV and visible spectrum, and even emit well into the near infrared (NIR) thanks to the 0.7 eV/1700 nm bandgap of InN as is shown in Figure 1.4.1. Compared to the other III-V materials systems shown on the right side of Figure 1.4.1, which span only from green wavelengths into the NIR, AlGaInN has the largest tunable emission range of any know semiconductor materials system, and sees the widest use by far in the fabrication of UV, blue, and green LEDs [2].

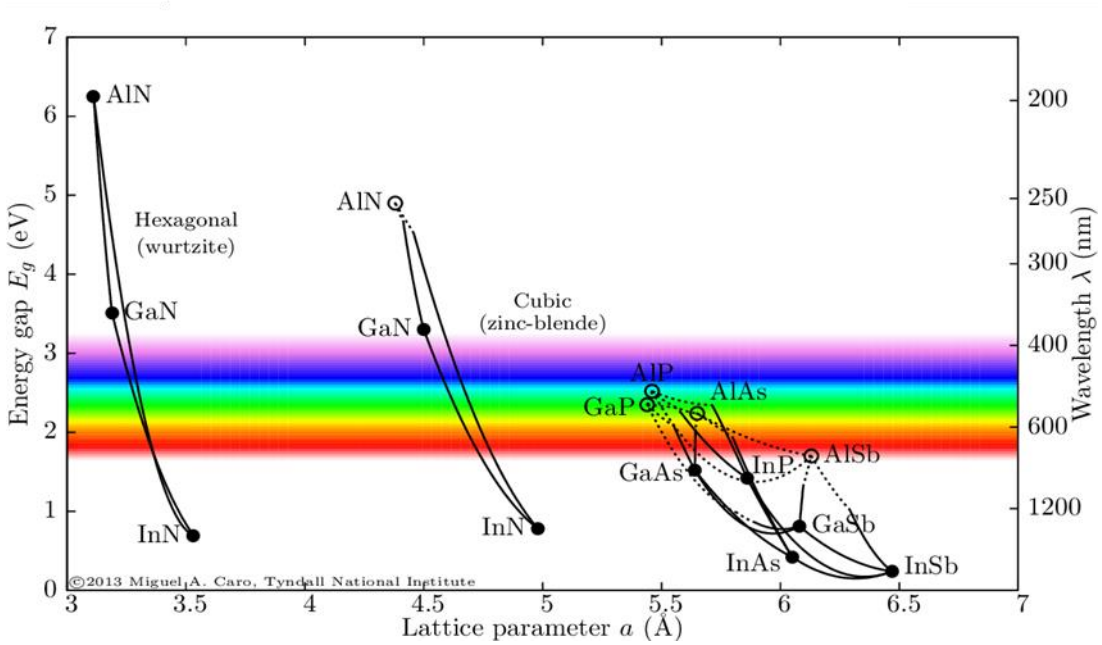

Figure 1.4.1: Bandgap vs lattice parameter for III-V semiconductors and their alloys [19].

AlGaN and AlGaInN alloys have a hexagonal wurtzite crystal structure, in contrast to the zinc-blende structures found in most other III-V semiconductors. Figure 1.4.2 shows a GaN unit cell, with Ga atoms shown in gray and nitrogen atoms in yellow. While cubic zinc-blende AlGaInN crystals can also be grown, the wurtzite form is the most thermodynamically stable and is dominant in all applications [20]. In wurtzite GaN, all Ga atoms are bonded to four N atoms, and vice versa, with an ABAB stacking order [2]. The electronegativities of Ga and N are 1.81 and 3.04 respectively [21], with electrons attracted more strongly to the to the N atom leading to formation of a dipole moment at the location of each bond. While dipole moments exist in the bonds of almost all compound materials, centrosymmetric crystals have inversion symmetry which nullifies the long-range effects of these dipolar bonds. However, wurtzite GaN is non-centrosymmetric and lacks inversion symmetry, leading to formation of a net electric dipole in each unit cell, which in turn

causes a net polarization to develop along the <0001> direction (vertical axis in Figure 1.4.2), also known as the c-axis [20,22]. This dipole induced polarization is referred to as "spontaneous polarization" (***P_{SP}***) and is partially responsible for a number of undesirable properties in GaN.

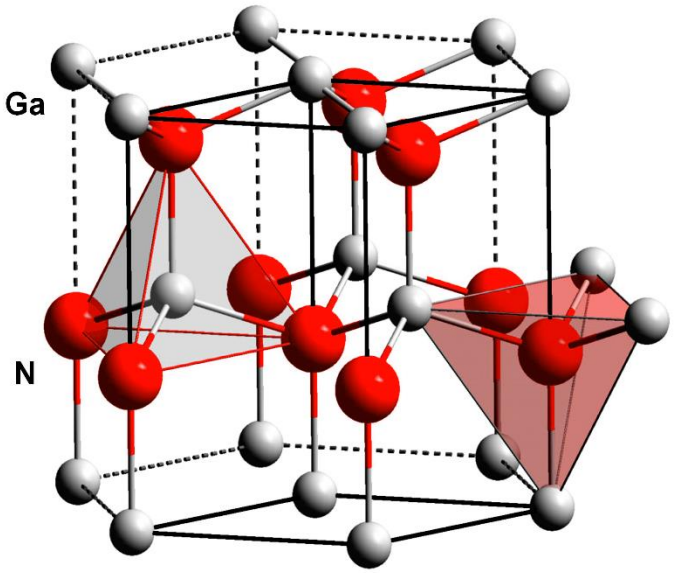

Figure 1.4.2: The wurtzite unit cell of GaN showing Ga atoms in white and N atoms in red [23].

Alloying of GaN with either Al, In, or both to form AlGaN, InGaN, or AlGaInN, is straightforward from the standpoint of crystal geometry. During growth of the crystal through use of metal organic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE), Al or In can be added in controlled amounts to form an alloy. In AlGaN for example, Al atoms will replace the Ga atoms at some of the sites in the crystal lattice, leading to formation of a crystal with electrical and optical properties between those of GaN and AlN. A material containing both Al and Ga is generally written as $Al_xGa_{1-x}N$, where x refers to the mole fraction of Al. For example, AlGaN which contains 40% Al and

60% Ga is written as $Al_{0.4}Ga_{0.6}N$. Alloying of compound semiconductors is critically important, especially for applications which rely on bandgap tuning to produce specific wavelengths for use in LEDs, lasers, and other optical devices. In a general sense, the bandgap of an AlGaN alloy can be roughly determined through linear interpolation of the bandgap values of AlN and GaN (6 eV and 3.4 eV respectively), through use of what is commonly referred to as Vegard's Law (1.5.1).

$$E_g(Al_xGa_{1-x}N) = xE_g(AlN) + (1-x)E_g(GaN) \tag{1.5.1}$$

While this formula is generally accurate, there is some deviation from this strictly linear interpolation as is evident from the bowed lines in Figure 1.4.1. In order to accurately determine the bandgaps of ternary and quaternary alloys, "bowing parameters" based on experimental data must be used to modify Vegard's Law [24]. The semi-linear interpolation approach of Vegard's law can also be used to determine other properties of alloys, such as lattice constants, thermal conductivities, extinction coefficients, and many others, with different sets of bowing parameters needed for each property.

1.5 Efficiency Limitations of Deep-Ultraviolet Light-Emitting Diodes

The efficiencies of DUV LEDs have been, and continue to be, the primary factor prohibiting their widespread adoption in many applications. Compared to GaN/InGaN blue LEDs, which often have EQEs in excess of 80% [25], AlGaN based DUV LEDs usually have EQEs in the single digits or lower [26,27], with the current record being 20% at 275 nm [28]. Modern commercial DUV LEDs have EQEs of only a few percent. The poor efficiencies of DUV LEDs can be attributed to a few primary factors, including poor carrier injection efficiency, internal polarization fields within AlGaN QWs, and poor light

extraction efficiency. Of these three issues, η_{EXT} is the most severe and the most difficult to address.

1.5.1 Carrier Injection Efficiency

As described in Section 1.1.3.1, carrier injection efficiency, η_{INJ}, quantifies the ratio of charge carriers injected into the device at the n- and p-contacts to the number of charge carriers which successfully make it to the active region for recombination. Achieving high η_{INJ} in AlGaN DUV LEDs is challenging for a number of reasons. The first is poor p-type doping of AlGaN, which leads to high p-AlGaN resistivity and low carrier concentration. Like in GaN/InGaN LEDs, Mg is used as a p-type dopant for AlGaN. The high activation energy of Mg dopant atoms of between 200 and 600 meV, means that only a very small fraction of them are ionized/activated at room temperature [29,30]. This means that even for physical doping in excess of 10^{20} cm^{-3}, hole concentrations can be lower than 10^{17} cm^{-3} at room temperature since the room temperature thermal energy (kT) of 26 meV is at best an order of magnitude lower than the activation energy of the Mg dopant atoms [29,30]. Despite significant efforts to increase the effectiveness of p-type doping, the resistivity of p-type AlGaN still remains very high compared to that of p-GaN, and actively limits the IQE of DUV LEDs. Efforts to increase hole concentration in p-AlGaN through physical doping of Mg to near degenerate levels has the downside of producing marked increases in defect density, creating point defects which can act as recombination centers in the bulk p-AlGaN outside of the QW, further limiting η_{INJ} [2]. One method that has been explored to improve the series resistance of AlGaN LEDs is the use of lower resistivity p-GaN in place of p-AlGaN. While this approach is effective at reducing series resistance and increasing the IQE of DUV LEDs, it negatively impacts η_{EXT} as p-GaN, with its lower

bandgap of around 3.4 eV, strongly absorbs DUV light. Other techniques for improving p-type resistivity, such as polarization doping [31], short period superlattices [32], and alternative p-type materials such as hexagonal boron-nitride (h-BN) [33] are also under investigation.

In addition to difficulties with p-type doping, electron overflow also decreases η_{INJ} in AlGaN DUV LEDs. As a result of the imbalance of electron and hole concentrations on the n- and p-sides of the QW/MQW, more electrons are injected into the QW than holes. This accumulation of electrons, especially at high injection current densities, eventually leads to "electron overflow," in which excess electrons leak into the p-type region, neutralizing holes and further lowering the injection rate of holes into the QW [34]. Electron overflow is usually combated through use of an electron blocking layer (EBL), which improves the confinement of electrons within the QW/MQW region, at the tradeoff of lowering hole injection efficiency. Extensive effort has been devoted to engineering of the electron blocking layer to maximize electron confinement while maintaining a minimal impact on hole injection. Recent approaches include use of AlN inserted EBLs [35], superlattice EBLs [36], and engineering of the last QB in tandem with the EBL [34].

The wide bandgap of the AlGaN used in DUV LEDs also causes contact resistance issues. It is difficult to obtain a sufficiently low p-AlGaN/metal barrier height to allow for truly ohmic I-V characteristics, which further impacts η_{INJ} [37]. Contacts with large barrier heights, termed "Schottky contacts," introduce an additional voltage drop to the device, raising the turn on voltage. High work function metals such as Ni, Au, Pt, and Pd are most commonly used, with Ni/Au being the most common [37,38]. Despite extensive investigation and optimization of different metal stacks to obtain more ohmic contacts, the

most effective approach to reducing p-contact resistance is to grow a thin layer (< 50 nm) of highly doped p-GaN on top of the p-AlGaN, which allows much lower contact resistance to be achieved. However, this reduced contact resistance comes at the tradeoff of increased absorption of DUV light by the p-GaN layer [37,38].

1.5.2 The Quantum Confined Stark Effect and Radiative Recombination Efficiency

One of the limiting problems of DUV LEDs is the quantum confined stark effect (QCSE), a phenomenon in which the high strength internal electric fields in AlGaN QWs confine the electron and hole wavefunctions to opposite sides of the QW, which reduces the electron-hole wavefunction overlap and reduces the spontaneous emission radiative recombination rate (R_{sp}). Reduction of R_{sp} directly reduces η_{RAD} by reducing the probability of radiative recombination events, meaning that a higher proportion of electron-hole recombination events are non-radiative. A number of different approaches have been investigated as a means to alleviate the QCSE, including the use of non-/semi-polar AlGaN grown on non-/semi-polar substrates [39], staggered AlGaN QWs [40], strain-compensated AlGaN QWs [41], type-II AlGaN QWs [42], and AlGaN-delta-GaN QWs [43]. Of these approaches, many have been found quite effective at either reducing internal electric field intensity or increasing electron-hole wavefunction overlap through band structure engineering.

In addition to mitigating the QCSE to improve R_{sp}, η_{RAD} can also be improved by reducing the probability of non-radiative recombination events. As described in Section 1.1.3.2, SRH recombination is the primary non-radiative recombination mechanism at low to moderate current densities. SRH recombination relies on the presence of crystal defects, which act as trap states within the bandgap, allowing electrons to recombine indirectly into

the valance band without producing a photon. In AlGaN, crystal defects are usually related to threading dislocations (TDDs) which originate from lattice mismatch between the AlGaN epitaxial layers and the substrate (usually sapphire) [44,45]. Growth of low TDD AlGaN layers has seen significant improvement over the past decade as growth techniques have advanced, and several research groups have demonstrated that IQE can be increased from less than 1% to more than 60% through a two order of magnitude reduction in active region TDD from 10^{10} cm^{-2} to 10^{8} cm^{-2} [28,46–48]. These results show that it is critically important to reduce TDD to at least 10^{8} cm^{-2} in order to achieve high IQE in DUV LEDs.

1.5.3 Emission Polarization and Light Extraction Efficiency

The most significant issue hindering the efficiency of DUV LEDs is light extraction efficiency. Conventional GaN/InGaN blue LEDs can have extraction efficiencies in excess of 80% [29], while DUV LEDs typically have extraction efficiencies of less than 10%. This is due several issues, including a large refractive index difference between AlGaN and air, which limits the escape cone for light [49], absorption of light by the p-GaN often grown to improve p-contact resistance, reabsorption of light by the QW and defects, and undesirable TM-polarization due to valence band mixing.

The high refractive index of AlGaN alloys, generally between 2.6 and 2.8 in the DUV range [50], severely limits the ability of photons generated within the QW to escape the LED into free space. Escape of photons from an LED is governed by Snell's Law, a simple relation between angle of incidence of a photon on a material interface and the refractive indices of the materials on either side of said interface. Manipulation of Snell's Law yields a formula for the "critical angle," θ_c, given below, measured with respect to the surface normal of the interface, where n_1 is the refractive index of the material in which the

light is propagating (air), and n_2 is the refractive index of the material in which the light is generated (AlGaN).

$$\theta_c = \sin^{-1}(n_1/n_2) \tag{1.5.2}$$

It is evident from equation 1.5.2 that the larger the difference between n_1 and n_2, the smaller the critical angle. Light incident upon the interface with an angle greater than θ_c will be completely reflected in a phenomenon referred to a "total internal reflection" (TIR). For light crossing an interface from AlGaN ($n{\sim}2.5$) into air ($n_{air} = 1$), the critical angle is $\theta_c = 23.6°$. The concept of a critical angle can be translated into that of an "escape cone" in three-dimensional space through rotation of the critical angle around the surface normal, giving rise to a cone outside of which all light incident on the interface will be completed reflected. The solid angle encompassed by this escape cone can, in turn, be used to calculate light extraction efficiency theoretically. Equation 1-3 gives the η_{EXT} as a function of θ_c.

$$\eta_{EXT} = 1/2\,(1 - \cos(\theta_c)) \tag{1.5.3}$$

From equation 1.5.3, a critical angle of 23.6° translates to an extraction efficiency of $\eta_{EXT} = 4.18\%$, which is extremely poor. In additional to this geometric constraint, absorption of DUV light by the p-GaN layer, which has a much lower bandgap (~3.4 eV) than the AlGaN QW, and defect sites in the epitaxial layers also plays a significant role in lowering the extraction efficiency of DUV LEDs.

Transverse magnetic (TM) polarized photons have their magnetic field component in plane/parallel with the QW layer, and have a greatly reduced effective critical angle, making them much more difficult to extract from a conventional, planar mesa LED. While

visible light LEDs emit almost no TM-polarized photons, the same is not true for DUV LEDs. The fraction of photons with TM-polarization increases with Al-content due to a phenomenon called valence band mixing. In valance band mixing, rearrangement of the valence subbands, primarily the heavy hole (HH), light hole (LH), and crystal-field split-off hole (CH) bands occurs as the Al content of an AlGaN QW is increased. In GaN and low Al-content AlGaN, most electrons recombine into the HH subband, which has a band edge closest to that of the conduction band. As Al content is increased, the HH, LH, and CH subbands move closer to one another, until the CH subband eventually rises above the HH and LH subbands at an Al content of ~70% [51]. Light emission from a CB-HH recombination event is transverse electric (TE) polarized, with the electric field component of the emitted photon in-plane with the QW (perpendicular to the AlGaN c-axis) [52]. On the other hand, light emission from a CB-CH recombination event is transverse magnetic (TM) polarized, with the magnetic field component of the emitted photon in-plane with the QW [52]. As such, as emission wavelength is decreased by increasing the Al-content of the AlGaN QW, η_{EXT} decreases due to an increase the fraction of photons with TM-polarization. This issue can be addressed, in theory, through the use of delta-QW designs, which alter the polarization properties of the QW to reduce the fraction of photons emitted with TM-polarization [43,53].

1.6 Motivations and Dissertation Organization

Many obstacles still exist in the development of high efficiency ultraviolet LEDs. In 2024, the penetration of UV LEDs, in particular DUV LEDs, into many of their potential applications remains very limited due to the low efficiencies of these emitters, especially when compared to their blue emitting counterparts. Chapter 1 has introduced relevant

background information, providing a summary of LED fundamentals and the limitations of modern DUV LEDs. Chapter 2 will provide a summary of the current state of DUV LEDs, and the different methods currently being implemented to improve light extraction efficiency. This will include discussion of fabrication approaches such as surface roughening and substrate patterning, photonic crystals and reflective contacts, microlens arrays and nanostructuring, p-AlGaN contact layers, and nanowire arrays. Chapter 3 will introduce and give detailed descriptions of experimental methods and fabrication processes for light emitting diodes in the facilities available on the campus of the Rochester Institute of Technology. Detailed process information for photolithography, dry etching, wet etching, metallization, dielectric deposition, and physical and electro-optical characterization will be provided in order to allow for replication of presented results. Chapter 4 covers the core research of this dissertation; the development of top-down fabricated, electrically driven DUV nanowire array LEDs and micro-LEDs. Also included in Chapter 4 is an finite-difference time-domain (FDTD) simulation study of light extraction efficiency which explores the effects of micro/nanostructure geometry and light polarization on extraction efficiency. While much research has been performed on epitaxially grown nanowire array DUV LEDs, no top-down fabricated, electrically driven DUV nanowire/nanostructure array LEDs have yet been demonstrated in literature. This dissertation presents the first realizations of such devices. Chapter 4 concludes with a summary of future prospects and directions for this research. Chapters 5 compiles projects not directly related to DUV LEDs, including simulation-based development of InGaN/delta-InN quantum wells for high efficiency red emission, green emitting

micropillar arrays LEDs, passive matrix micro-LED displays, nanowire quantum dot single photon emitters, and nanosphere arrays for enhanced light outcoupling for mesa LEDs.

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CHAPTER 2: Approaches for Light Extraction Enhancement in Deep-Ultraviolet LEDs

2.1 Planar Devices

As discussed in Section 1.5.3, light extraction efficiency is the most significant hurdle hindering the development of high efficiency deep-ultraviolet LEDs. As such, there have been extensive research efforts directed at improving light extraction from DUV LEDs over the past ten years. The vast majority of these efforts have focused on methods of improving light extraction from conventional mesa LEDs, with many finding moderate success. Figure 2.1.1 summarizes the current status of DUV LED research. The majority of DUV LEDs have EQEs of 1-5% [1], with the current record standing at 20% (at 275 nm), fabricated by Takano *et. al.* using a combination of efficiency enhancement techniques [2]. Typical mesa DUV LEDs conform to two paradigms. Top emitting devices are LEDs which are designed to emit light away from the growth substrate (usually sapphire), and as such must minimize the area of the mesa covered by the metal p-contact. Bottom emitting devices are LEDs designed to emit light through their growth substrate. These devices typically use reflective p-contact layers to cover the entire top of the mesa in order to minimize escape of light from the top of the LED. The methods available to increase light extraction efficiency depend on the intended emission direction of the LED and are summarized in the following sections.

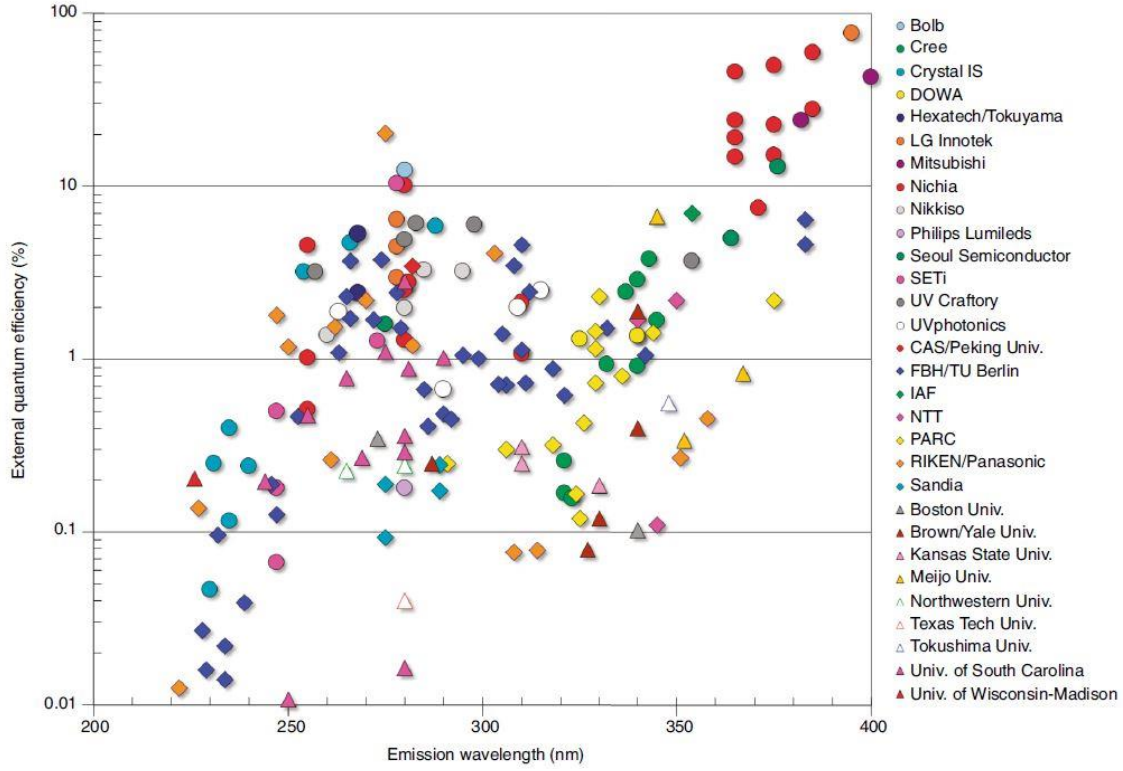

Figure 2.1.1: EQEs of planar UV LEDs developed in the past 20 years, showing the trend of EQE increasing with wavelength. The dip in EQE around 320 nm is due primarily to lack of research interest in this wavelength range. Reprinted with permission [1].

2.1.1 Substrate Patterning and Surface Roughening

Substrate patterning and surface roughening are commonly used techniques not only for fabrication of DUV LEDs but also for visible wavelength LEDs [2–9]. Substrate patterning usually consists of patterning the top of the sapphire substrate prior to growth of the AlGaN epitaxial layers. The primary purpose of substrate patterning is not actually to increase η_{EXT}, but rather to improve the quality of the AlGaN growth and reduce strain and strain related defects in the AlGaN epitaxial layers [2–9]. The added benefit of

increasing η_{EXT} comes when it is used in a bottom emitting LED, where light extraction across the sapphire/(AlGaN/AlN) interface is aided by the presence of a non-planar interface interrupted by a periodic array of micro/nanostructures. Patterning of the sapphire is usually achieved using a SiO_2 masked dry etch of the sapphire using a Cl_2 plasma to form periodic arrays of structures between several hundred nanometers and several microns in diameters as can be seen in Figure 2.1.2(a). Patterned sapphire substrates are commonly used in the fabrication of commercial LEDs and were also used in the fabrication of the highest EQE DUV LED to date, emitting at 275 nm with an approximate EQE of 20% [2]. Substrate patterning is not desirable for use in surface emitting DUV LEDs, as it decreases the reflectivity of the sapphire/(AlGaN/AlN) interface, reducing the amount of light which can be extracted from the top of the LED.

Surface roughening is also a commonly used approach for increasing light extraction in both DUV LED and visible light LEDs [10–16]. In top emitting LEDs, surface roughening is generally accomplished by performing a rough dry etch of the p-GaN surface, followed by a short hydroxyl-based wet etch which leads to formation of either etch pits or nano-pyramids, as seen in Figure 2.1.2(b). These small structures disrupt the total internal reflection (TIR) or light incident upon the p-GaN/air interface, increasing the effective escape cone of the light and increasing extraction efficiency. While it is possible to use surface roughening for top emitting DUV LEDs in the manner described above, it is more commonly used in bottom emitting devices. For example, the bottom of the sapphire substrate can be roughened using dry etching, wet etching, or mechanical abrasion in order widen the escape cone for light crossing the sapphire/air interface in bottom emitting DUV LEDs. Additionally, some devices which use laser liftoff (LLO) to separate the AlGaN

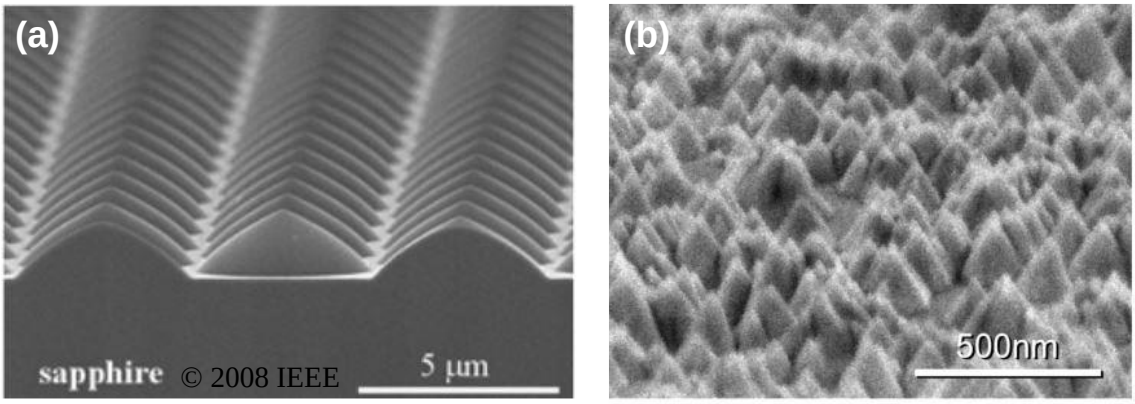

Figure 2.1.2: SEM images showing a patterned sapphire substrate (a) [17] and surface roughening of GaN (b) [13]. Reprinted with permission [13, 17].

epitaxial layers from the sapphire substrate make use of surface roughening to improve extraction of light from the n-AlGaN surface [11,13]. In these devices, the LED structure is fabricated and metallized before being removed from the growth substrate and inverted on a carrier wafer, with the n-AlGaN layer now on top [11,13]. A hydroxyl-based wet etch is then used to form the nano-pyramid structures shows in Figure 2.1.2(b), increasing η_{EXT} [11,13].

2.1.2 Photonic Crystals and Reflective Contacts

Photonic crystals have been investigated as means to either reflect or transmit light at what would otherwise be a planar interface. A photonic crystal (PC) is a periodic array of micro/nanostructures which interacts with photons in a similar manner to how an atomic lattice interacts with electrons. A photonic crystal can be designed to either reflect or transmit certain wavelengths of light by altering the size and pitch of the micro/nanostructures. This allows PCs to be used as either reflective layers in bottom emitting LEDs, or as extraction assisting layers in top emitting LEDs [18–26]. In bottom emitting LEDs, a reflective photonic crystal can be fabricated on top of the p-AlGaN layer

to reflect light out through the substrate [20]. In a top emitting LED, a transmissive photonic crystal can be fabricated on top of the p-GaN layer to aid in extraction of light from the top of the LED [23]. Figure 2.1.3 shows a photonic crystal fabricated in AlGaN using a combination of Cl_2 based dry etching and hydroxyl-based wet etching.

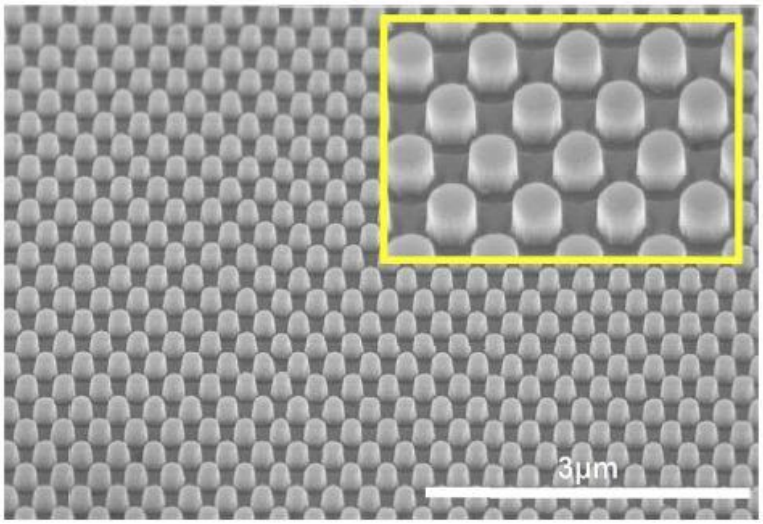

Figure 2.1.3: An SEM image of a photonic crystal fabricated in AlGaN using a combination of wet and dry etching. Reprinted with permission [23].

While PCs can in theory be more reflective than a layer of metal, one major downside is the added complexity and number of process steps required to form a reflective photonic crystal. As such, reflective metal contacts are more commonly used to increase light extraction in bottom emitting devices [2,27–33]. Optimization of metal contact reflectivity considers several factors, including thickness of the metal layers included in the contact stack, the extinction coefficients of the metals, the deposition method used, and the work function of the metals. Often times the most reflective metal for a certain wavelength cannot be used as a contact because its work function does not allow it to form an ohmic contact the n-AlGaN, p-AlGaN, or p-GaN beneath it, which negatively effects

the electrical properties of the LED and increases turn-on voltage. Common metals/metal stacks used as reflective p-contacts include Pd/Al [31], Ni/Au [29], and Ni/Al [27], while Cr/Al [28,29] and Al/Ti [30] are commonly used as reflective n-contacts.

2.1.3 Microlens Arrays and Nanostructuring

Microlens arrays have also been investigated as means to enhance light extraction from top emitting LEDs [34–43]. The advantage of microlens arrays is that they avoid the need for any sort of lithography or added process steps. Microlens arrays are typically fabricated by spin-coating nanosphere solutions onto the surface of the LED. Given the right concentration and spin speed these nanospheres will self-align to produce hexagonally close packed arrays with very good long- and short-range uniformity. SiO_2 nanospheres are often used as they have a refractive index between that of air and AlGaN, producing a sort of "graded index" profile which aids in light extraction. Polystyrene (PS) is then spin coated over the nanospheres to fill in between them and eliminate gaps between the spheres and the LED surface as shown in Figs. 2.4(a-b). The similar refractive indices of SiO_2 and PS (1.46 and 1.58 respectively) allow the resulting structures to act like lenses, disrupting total internal reflection and enhancing η_{EXT} [38].

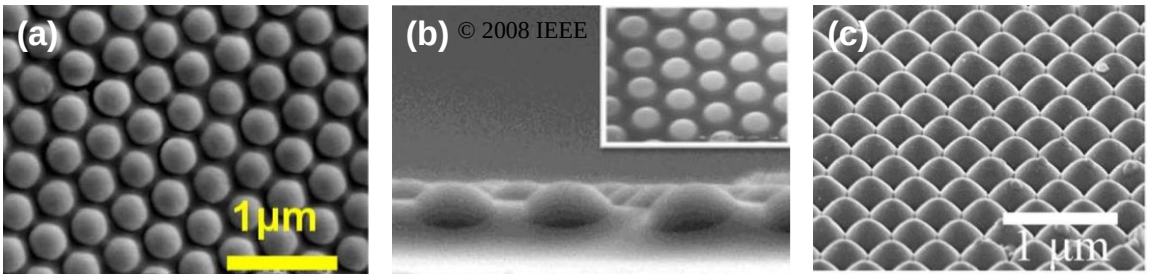

Figure 2.1.4: SEM images showing SiO_2/PS microlens arrays (a-b) [35,36] and nanostructured AlGaN (c) [44]. Reprinted with permission [35, 36, 44] © Optical Society of America, © IEEE.

Surface nanostructuring is also sometimes used to improve light extraction [44-46]. In contrast to substrate pattering, surface roughening, or photonic crystal formation, surface nanostructuring can be performed on either p-AlGaN, n-AlGaN, or sapphire, allowing it to be used in either top or bottom emitting devices. Surface roughening does not attempt to reflect or transmit light like a photonic crystal and is essentially a less refined version of the former, which serves only to disrupt total-internal reflection and widen the escape cone of light. Surface nanostructuring can be performed either by patterning and etching the p-/n-AlGaN or sapphire surfaces, or by depositing another material such as SiO_2 or Si_3N_4 and forming nanostructure arrays in that layer. An SEM image of nanostructured AlGaN is shown in Figure 2.1.4(c) and appears similar to a photonic crystal or microlens array.

2.1.4 p-AlGaN Contact Layers

Use of a p-GaN contact has a significant negative impact on light extraction in DUV LEDs [47]. The 365 nm (3.4 eV) bandgap of GaN is much lower than that of the DUV light emitted by the LED QW, and thus strongly absorbs the emitted light. Most DUV LEDs use a highly doped p-GaN contact layer to improve contact resistance due to difficulties in obtaining sufficient Mg dopant ionization in p-AlGaN. As such a trade-off exists between η_{EXT} and IQE. Recently research has been focused on replacing the p-GaN contact layer with a "transparent" p-AlGaN layer which is both transparent to the emitted light and doped sufficiently to allow for sufficiently low resistivity and formation of an ohmic p-contact [2,47–53]. As the high activation energy of Mg dopant atoms in p-AlGaN appears to be a permanent barrier to attainment of low resistance conventional p-AlGaN contact layers, complex new approaches such as polarization doping have recently been explored as means to reduce resistivity [52,54–56]. Polarization doping utilizes compositional grading during

the growth process to decrease the Al fraction of the p-AlGaN layer along the growth direction, leading to a net negative polarization charge [55]. This has been found to dramatically improve the p-type conductivity of these graded AlGaN films when compared to conventional Mg-doped AlGaN. It is likely that advancements in p-AlGaN growth will soon allow the benefits of a transparent p-AlGaN layer to supersede its current drawbacks of higher resistivity and contact resistance.

2.2 Nanowires

While many advances have been made in improving the light extraction efficiency of mesa DUV LEDs over the past decade, there remain significant challenges facing these devices. Mesa LEDs become fundamentally limited at shorter wavelengths as TM-polarized emission becomes more prevalent as described in Section 1.5.3. TM-polarized emission is much more difficult to extract from the tops of mesa LEDs, as the transverse magnetic component of TM-polarized photons drastically reduces their effective escape angle when compared to that of TE-polarized photons. Fortunately, TM-polarized light is much easier to extract through vertical surfaces, such as mesa sidewalls. Unfortunately, the dimensions of mesa LEDs are usually large enough that photons are reabsorbed by either the p-GaN layer or materials defects before they reach the edges of the mesa. The simple solution to this is to simply reduce the dimensions of the mesa so that TM-polarized photons can escape through the mesa sidewalls before being absorbed. Micro-LEDs are a perfect example of this, and generally have much higher extraction efficiencies than larger LEDs with dimensions on the order of 100+ microns. For bulk lighting applications, which

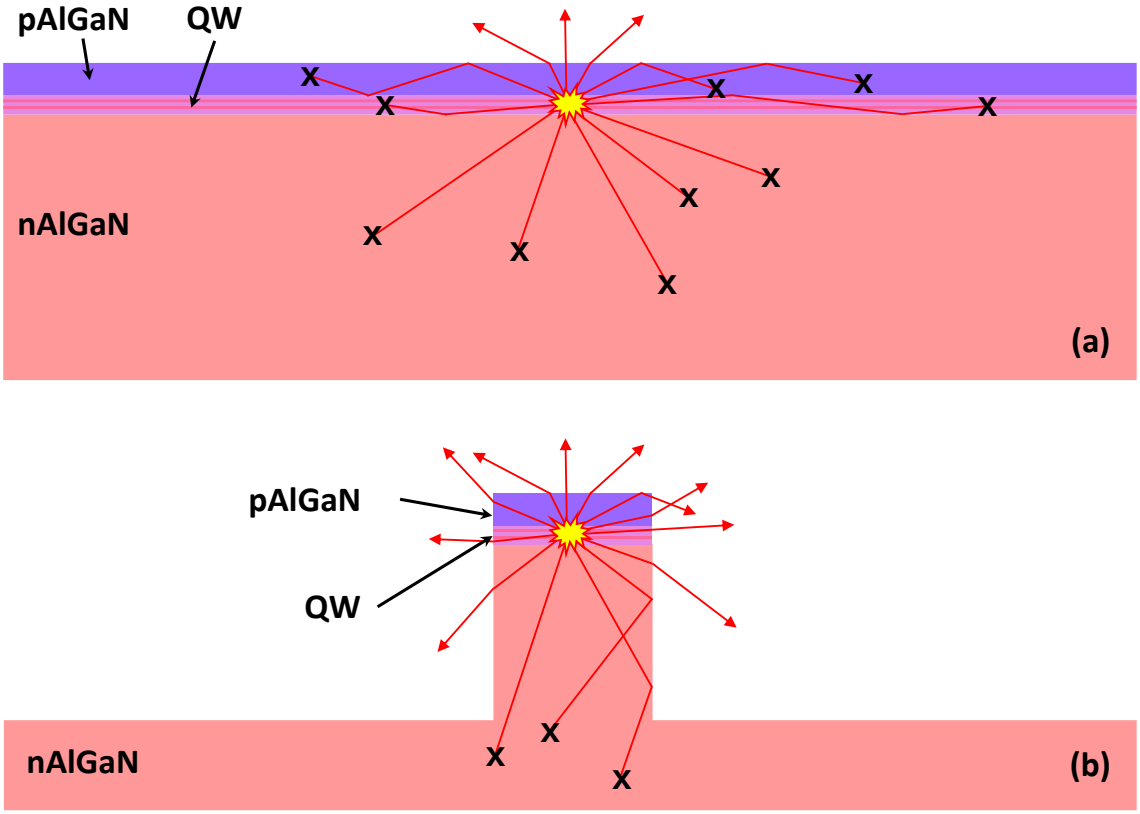

Figure 2.2.1: Schematic showing extraction (arrow) or absorption (x) of light in a planar mesa DUV LED (a), and a nanowire DUV LED (b).

make up the majority of applications for DUV LEDs, using many individually addressed micro-LEDs is very cost prohibitive. While the high costs associated with micro-LEDs can be tolerated for applications such as ultra-high resolution near eye displays and wearable devices, the same cannot be said for DUV LED arrays meant to purify water or neutralize pathogens in a hospital. As such, a simpler method of increasing the "sidewall area" of DUV LEDs is needed and can be accomplished through use of nanowire arrays. Figure 2.2.1 shows the effects of nanowire formation on extraction of light from a DUV LED. In the mesa LED in Figure 2.2.1(a), the majority of light is trapped inside the LED structure by TIR and is absorbed before it can escape through the mesa sidewalls. In the nanowire

shown in Figure 2.2.1(b), almost all light is able to escape due to the reduced lateral dimensions of the structure.

While nanowires undoubtedly enable large increases in extraction efficiency, especially for TM-polarized light, they come at the tradeoff of reduced active region area. For example, a 100x100 μm mesa LED has an active region volume of 10,000 um^2. A 100x100 μm nanowire array consisting of 1 μm diameter nanowires with a pitch of 2 μm would have an active region area of only 1,960 μm^2, less than 1/5 that of the mesa LED. As such, the reduction of active region area must be considered when making claims of improved extraction efficiency and EQE. Another factor that must be considered is the far field radiation pattern of nanowires arrays, which quantifies the direction with which light is emitted. These factors must all ultimately be considered when designing nanowire DUV LEDs, however the main focus of current DUV nanowire LED research is the optimization of light extraction efficiency. There are two methods of fabrication nanowires: bottom-up epitaxial growth, and top-down etching. The following sections discuss these approaches, giving the pros and cons of each.

2.2.1 Epitaxial Nanowires

The majority of research on DUV nanowire LEDs has thus far centered on epitaxially grown nanowires created using metal organic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE) [26,57–67]. The main advantage of this approach is that, given the ability to grow AlGaN nanowires with in-situ doping, very little additional fabrication is required. Epitaxial growth of nanowires requires extensive knowledge and optimization of growth parameters such as temperature, gas flow/atom flux rates, and growth substrate surface preparation. Epitaxial growth of nanowires results in

formation of densely packed, disordered arrays of irregular nanowires as shown can be seen in Figure 2.2.2. As previously stated, the advantage of this approach is that once the nanowires are grown, very little additional fabrication must be performed to produce an electrically driven device. Because the nanowires are so closely packed, it is possible to simply deposit a thin metal contact on top of the nanowire array to act as the p-contact. Unfortunately, the non-uniformity of these arrays makes the nearly impossible to ensure that all nanowires are electrically connected. Gaps between nanowires create discontinuities in the metal layer, which create longer resistive pathways to some regions of the area addressed by the p-contact. The metal layer must remain thin in order to be transparent to UV light and thus cannot effectively bridge the gaps between nanowires. The lack of a transparent conductive material which is transparent in the DUV range necessitates the use of metal in formation of the p-contact, and severely limits the

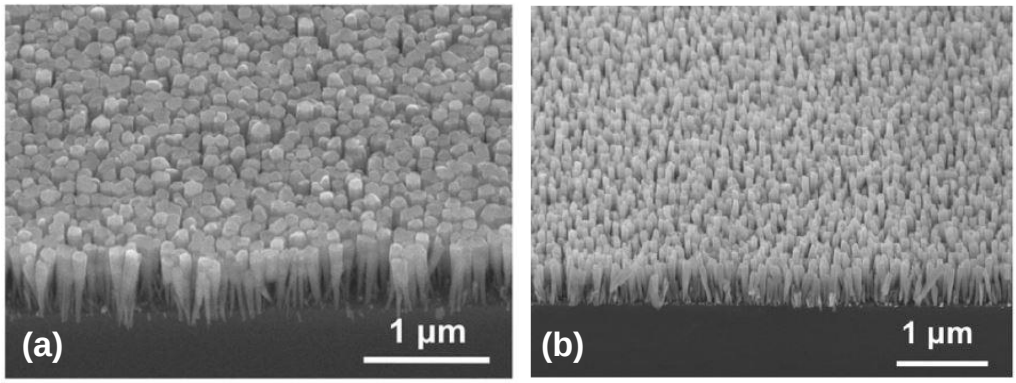

Figure 2.2.2: SEM images of epitaxial AlGaN nanowires grown using MBE (a) [58] and MOCVD (b) [66]. Reprinted with permission [58, 66].

performance of these disordered nanowire array LED. Indium tin oxide (ITO) is a transparent conductive material which can be used as a p-contact for visible light LEDs, however its bandgap of ~4 eV means it strongly absorbs DUV light and thus cannot be

used in DUV LEDs. Additionally, the close proximity of these nanowires makes light trapping a significant issue. Light emitted from the nanowire sides is easily trapped within the nanowire array with no way to escape, eliminating the key advantage nanowire LEDs are supposed to have over mesa LEDs. Selective area epitaxy (SAE) can be used to avoid many of the issues present in disordered arrays of epitaxial nanowires [68,69]. In SAE,

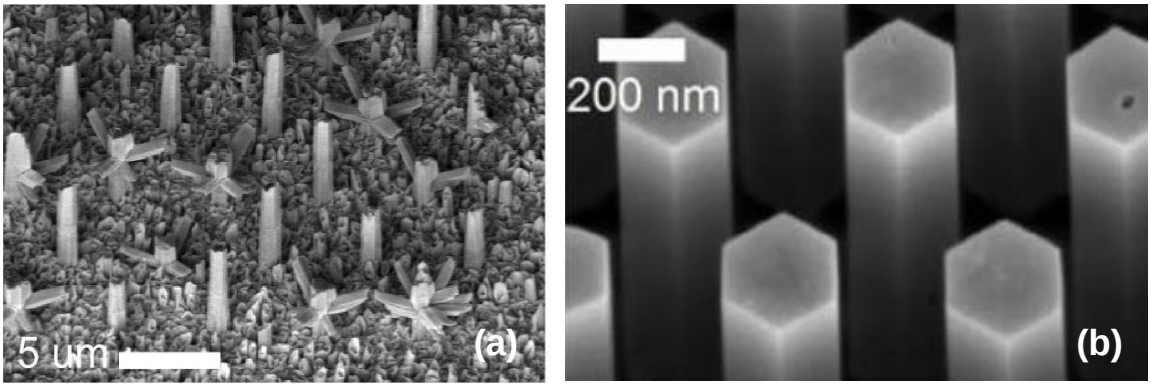

Figure 2.2.3: SEM images of epitaxial AlGaN nanowires grown using MBE and selective area epitaxy. Reprinted with permission [68, 69].

patterns are first created on the growth substrate using a material such as SiO_2, permitting growth of nanowires in some areas and preventing in others. This allows the locations in which nanowires form to be controlled, as shown in Figure 2.2.3. While this technique eliminates many of the issues with disordered nanowire growth, it significantly increases the complexity of the fabrication process [68,69].

In order to obtain nanowires with diameters less than several hundred nanometers, high resolution photolithography must be performed to create the SAE growth mask. Additionally, as can be seen in Figure 2.2.3(a), the uniformity of SAE grown nanowires is still not perfect. While DUV emitting nanowires have been created using MBE and SAE,

no electrically driven devices have yet been creating using this approach, which is still in its relative infancy compared to growth of disordered nanowire DUV LEDs [68,69]. The primary difficulty lies in electrically addressing the tops of nanowires which are spaced very far apart compared to the tightly packed, disordered arrays in Figure 2.2.2.

To date, the EQEs of epitaxial DUV nanowire LEDs have been much lower than those of mesa DUV LEDs due in part to the aforementioned issues. Reported EQEs from DUV LEDs range from 0.012% at 242 nm [58] to 0.4% at 275 nm [59]. While these results obviously cannot match those of mesa devices, it is important to keep in mind that the body of research on DUV nanowire LEDs is much smaller than that of DUV mesa LEDs. DUV nanowire LEDs are still more or less in their infancy, and recent advancements in material growth and fabrication processes will almost certainly lead to significant advancements in DUV nanowire LED EQE in the coming years.

2.2.2 Etched Nanowires

A little explored alternative to epitaxial growth of nanowires for LEDs is top-down etching. In this approach, subtractive process are used to form nanowires from a bulk epitaxial stack [70–72]. Etching allows for formation of perfectly uniform arrays of nanowires using the processes developed and perfected by the semiconductor industry over the past half century. Instead of using unreliable epitaxial growth, nanowires are sculpted from a planar epitaxial stack in the same way that mesa LEDs are fabricated. This eliminates uncertainties regarding nanowire position, spacing, and quality. To date, only a few etched nanowire LEDs have been reported, with none of these emitting within the DUV range. Figure 2.2.4(a) shows the GaN nanowires of a yellow emitting nanowire LED,

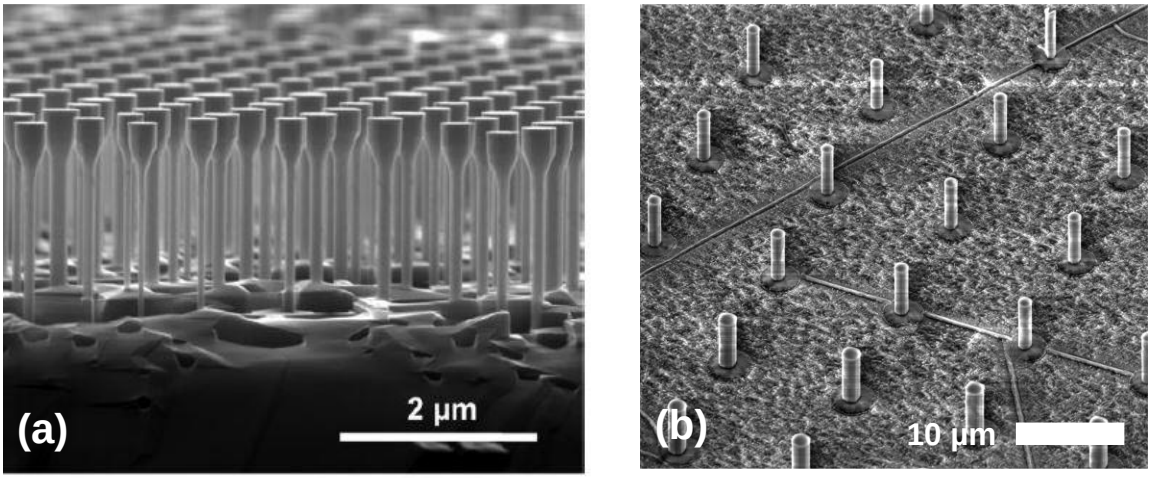

Figure 2.2.4: SEM images showing top-down fabrication GaN nanowires (a) [70] and AlGaN nanowires fabricated in the SMFL (b). Reprinted with permission [70].

which were fabricated via a combination of dry and wet etching [70]. Figure 2.2.4(b) shows AlGaN nanowires fabricated by our research group in the SMFL.

Top-down etching not only improves the average quality of nanowires, but also opens the door to potential nanowire array displays, wherein individual nanowires are addressed individually. While DUV LEDs are of little use for displays, individually addressable DUV nanowire LEDs could be of use in various on chip photonics applications in which high energy photons are required. The ability to easily control nanowire location on wafer and ensure high nanowire yield could allow for easy integration with on chip waveguides and other wafer level optical components. In many ways, etched nanowires are similar to the micro-LEDs currently being developed for ultra-high resolution near eye displays, and are, in a sense, very small, high aspect ratio micro-LEDs. One of the biggest benefits of the top-down fabrication approach is the ability to control the spacing of nanowires to eliminate light trapping. Nanowires spaced many hundreds of nanometers or even microns apart are expected to experience negligible light trapping [73,74], which may

allow them to achieve the high EQEs which have eluded epitaxially grown nanowire DUV LEDs.

While it is not the focus of this research, it is important to also briefly discuss the cost-proposition of nanowire/micropillar devices. In general, an LED can be operated either for maximum power output per unit emitting area, or for maximum power efficiency. An example of the first, maximum power, use case might be for area lighting of a warehouse or sports facility. Here, the efficiency of the LED is not as important as its ability to illuminate a large area as cost effectively as possible. If power consumption is not a primary concern, and maximum luminous output power is desired from a fixture of limited size, light output power density (LOP density) becomes the primary consideration. As the cost of an LED depends primarily on the die size (i.e. how many yielding die can be produced per wafer), a higher LOP density corresponds to a more cost-effective device. An example of the second, maximum power efficiency, use case might be in a space-based application where device production cost is irrelevant, but in which power is generated by solar panels and is extremely limited. In this case, LOP density may be inconsequential compared to the efficiency of the LED.

Consider an example in which an 100x100 μm emissive area (10,000 μm^2) is available. If this entire area can be converted into a mesa LED with an EQE of 5%, or alternatively into a nanowire array with an EQE of 30%, the relative total LOP of these two different design approaches depends on the "fill factor" of the nanowire array. This fill factor can be calculated by dividing the cross-sectional area of a single nanowire by the square of the pitch of the nanowire array (assuming a square array). If, for example, each nanowire has a diameter of 1 μm, and the array has a pitch of 5 μm, this fill factor will be

3.14%. In other words, 96.86% of the active region has been removed. Alternatively, if the nanowire diameter is 1 μm and array pitch is 2 μm, the fill factor is 19.6%, and 80.4% of the active region has been removed. It is quite evident then, that despite the EQE of the nanowires being 6x that of the mesa, the total output power of that 100x100 μm region, if formed into a nanowire array, can be significantly lower than a 100x100 μm mesa. If the mesa is assumed to output 1 W of optical power, a 1/5 μm diameter/pitch nanowire array will output 0.0314*6 = 0.19 W, while a 1/2 μm diameter/pitch nanowire array will output 0.196*6 = 1.18 W. By removing much of the active region through dry etching in order to increase the EQE of a device, the total output power of the device is signficantly reduced unless the efficiency gain is high enough to offset this loss in active region area.

In the current year (2024), the efficiencies of nanowire devices are much lower than those of mesa devices, as previously described, so from a cost consideration standpoint, they are not viable for either type of application (max power or max efficiency). It is almost certain than nanowire array LEDs, either grown epitaxially or formed using dry etching, will never become cost competitive with mesa LEDs for maximum power applications. The gap is simply too wide and massive efficiency enhancements over mesa LEDs would be required to make nanowire devices competitive. However, given further improvements in the efficiencies of nanowire and micropillar array devices, they may eventually become viable in applications in which efficiency is the primary or sole consideration. One such application may be in water purification/sterilization in remote or underdeveloped regions. For example, a remote village without access to potable water could be supplied with a small solar panel and a UV water sterilization system. In this power limited case, a

nanowire DUV LED with an EQE of 20% may be more viable than a mesa LED with an EQE of 10% depending on the maximum current and voltage deliverable by the solar panel.

While this cost-proposition analysis may paint a seemingly bleak picture for the future of nanowire and micropillar array DUV LEDs, it is important to keep in mind that both mesa and nanowire/micropillar DUV LEDs are still in their infancy compared to other light sources such as mercury lamps and visible light LEDs. Future research advancements may introduce new physical principles, growth techniques, and fabrication approaches which upset our current understanding of DUV LEDs entirely. Likewise, furthering our understanding of nanowire/micropillar devices has, and will continue to aid in the development and improvement of mesa devices, and vice versa. The DUV LED research field is ultimately a collaborative environment, and no research truly goes to waste.

The core of the research presented in this dissertation involves the development of electrically driven, etched DUV nanowire/nanostructure array LEDs. Over the last five years our research group has made significant progress in the design and associated fabrication process development for these devices. In 2021, we published the first demonstration of etched, electrically driven DUV nanowire array LEDs in *AIP Advances* [75]. Subsequent research efforts have improved upon the devices discussed in that publication by utilizing improved epitaxies, more robust dielectric spacer layers, improved wet etch passivation, and improved contact metallization. Chapter 3 will discuss in depth the fabrication processes used to fabricate DUV nanowire LEDs in the RIT SMFL, while Chapter 4 will present our simulation and experimental results for these devices.

Chapter 2 References

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CHAPTER 3: LED Fabrication and Process Development

3.1 Fabrication Process Overview

Light emitting diodes can be fabricated using the same techniques and tools that are used in mass production of silicon based integrated circuits (ICs), and can thus benefit from the decades of refinement and billions of dollars of research which have made silicon ICs one of the most scalable technologies in the world. The LEDs in this dissertation were fabricated in the Semiconductor and Microsystems Fabrication Laboratory (SMFL) at the Rochester Institute of Technology (RIT), an academic cleanroom facility serving both research groups and industrial users. This chapter will outline process flows used in fabrication of both conventional mesa LEDs and nanowire LEDs, and then give detailed information on process parameters in subsequent sections to allow for replication of the experimental work described in this dissertation.

3.1.1 Mesa LEDs

Mesa LED fabrication begins with preparation and cleaning of a 2-inch (50 mm) wafer or wafer piece. The wafers used in this study were grown by a commercial vendor (Precision Micro-optics) using MOCVD, as III-Nitride growth capabilities are not available at RIT. Wafer/piece (hereafter "sample") cleaning is performed using either an industry standard RCA clean (1:1:5 NH_4OH/H_2O_2/DI 5 min + DI 2 min + 1:1:6 HCl/H_2O_2/DI 5 min + DI 2 min) or a solvent clean where the sample is immersed sequentially in acetone (5 min), isopropyl alcohol (IPA) (2 min), and DI water (2 min). Following the clean, the sample is dried with a nitrogen gun.

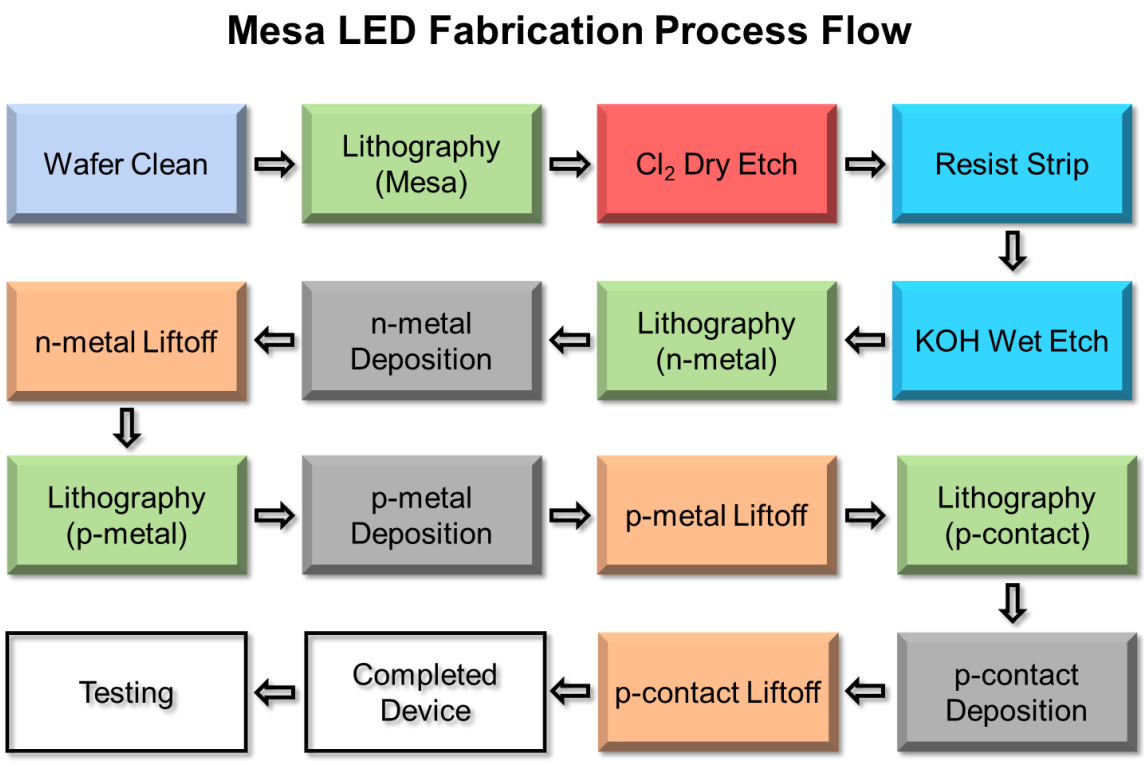

Figure 3.1.1: Mesa LED fabrication process flow with color coded process steps.

Next the mesa level lithography is performed. The sample is first baked at 170°C for 3 min to remove hydrophilic surface states and is then given sufficient time to cool (~2 min) before photoresist is applied through spin-coating. Alternatively, HMDS (hexamethyldisilazane) can be applied through vapor deposition to remove hydrophilic surface states and improve the adhesion of photoresist to the sample surface. The photoresist is then patterned using either laser direct write lithography (LDW), contact lithography, or projection lithography, depending on the desired resolution and availability of tools. The photoresist is then developed, and the resulting patterns are used to mask a $Cl_2/BCl_3/Ar$ dry etch of the underlying epitaxial layers to a depth of ~300 nm. This shallow dry etch typically results in the formation of minor micromasking (etch grass), as can be

seen in Figure 3.1.2(c), as well as damage to the sidewalls of the mesa, necessitating the use of a hydroxyl-based crystallographic wet etch which serves to remove both micromasking and mesa sidewall damage (Figure 3.1.2(d)). This hydroxyl-based etch is performed by immersing the sample in ~40% AZ400K, a KOH containing photoresist developer (~2% KOH by weight), at 80°C for ~30 min).

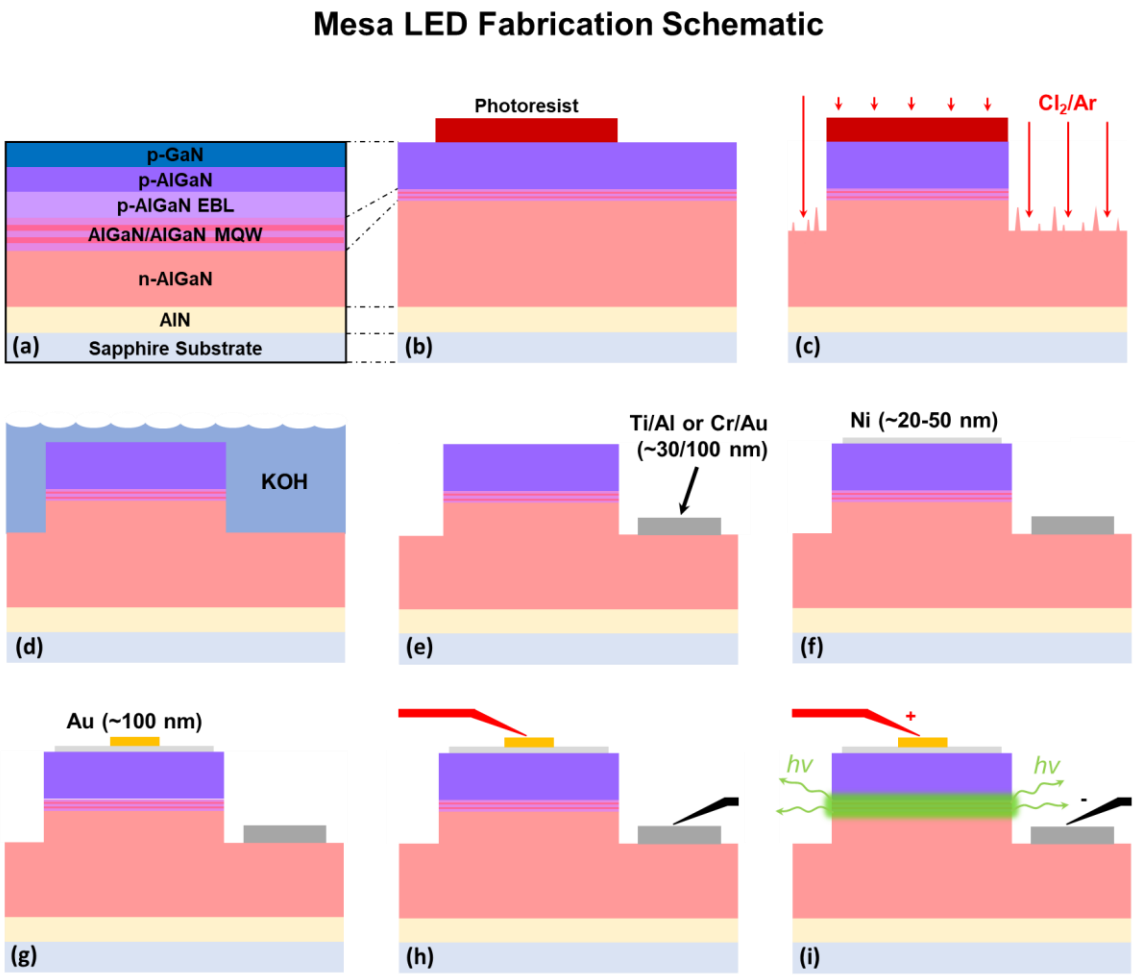

Figure 3.1.2: Mesa LED fabrication schematic showing mesa etching and metallization steps (not to scale).

The n-metal lift-off lithography is then performed, with the sample again baked and cooled before photoresist is coated. Liftoff resist (LOR) is coated first, followed by conventional photoresist. The resist is patterned and developed, and the n-metal stack, typically 30/100 nm Ti/Al or Cr/Au, is deposited using either thermal or electron beam evaporation. The sample is then immersed in N-Methyl-2-pyrrolidone (NMP) for ~24 hours to "liftoff" the metal on top of the photoresist, leaving it only in the lithographically defined locations (Figure 3.1.2(e)). This metal-liftoff process is then repeated to pattern the p-metal current spreading layer, which consists of ~20-50 nm of Ni, which serves to spread current over the entirety of the mesa surface with minimal impact on light extraction (Figure 3.1.2(f)). Finally, the p-contact metal, typically a small area of 100 nm Au, is patterned in the center of the mesa using this same liftoff process (Figure 3.1.2(g)). At this point the mesa LED is ready for testing, which is performed using a manual probe station and parameter analyzer. Two probes are brought into contact with the sample and are placed on the p- and n-contacts as shown in Figure 3.1.2(h). A positive bias is applied to the p-contact probe while the n-contact probe is held at ground in order to apply forward bias and illuminate the LED Figure 3.1.2(i).

3.1.2 Nanowire LEDs

Nanowire LED fabrication uses the same process and tools as mesa LED fabrication, but is fundamentally different. Instead of etching a large mesa structure and placing metal pads at the base (n-contact) and top (p-contact), a continuous array of nanowires is formed across the entire wafer. A universal n-contact is then deposited over the entire wafer, followed by a dielectric layer which exposes the tips of the nanowires.

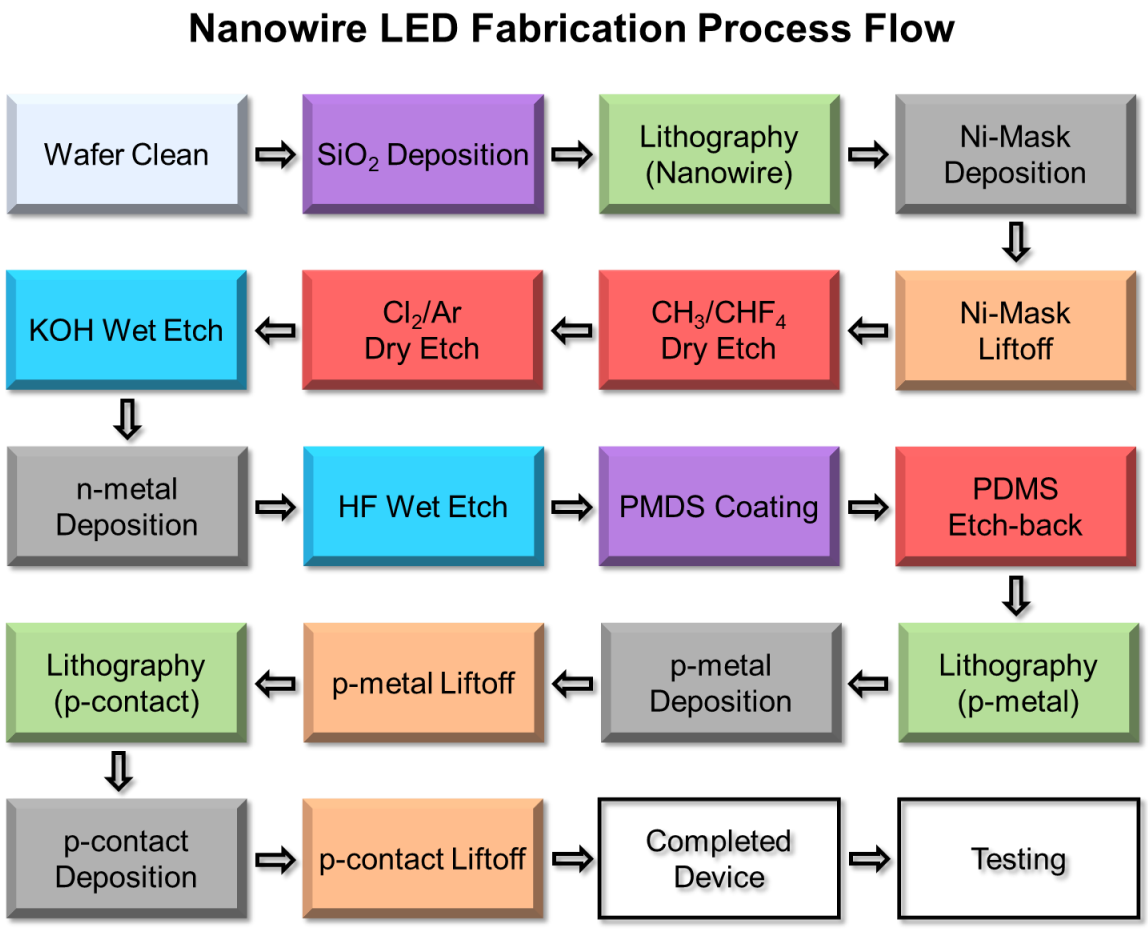

Figure 3.1.3: Nanowire LED fabrication process flow with color coded process steps.

Nanowires are then connected in parallel through patterning of the thin Ni p-contact in order to form LEDs or arbitrary size and wire count.

Nanowire LED fabrication likewise begins with preparation and cleaning of sample obtained from a commercial vendor. Sample cleaning is performed using either an industry standard RCA clean (1:1:5 NH_4OH/H_2O_2/DI 5 min + DI 2 min + 1:1:6 HCl/H_2O_2/DI 5 min + DI 2 min) or a solvent clean where the sample is immersed sequentially in acetone (5 min), isopropyl alcohol (IPA) (2 min), and DI water (2 min). Following the clean, the sample is dried with a nitrogen gun. Following sample cleaning, SiO_2, more specifically

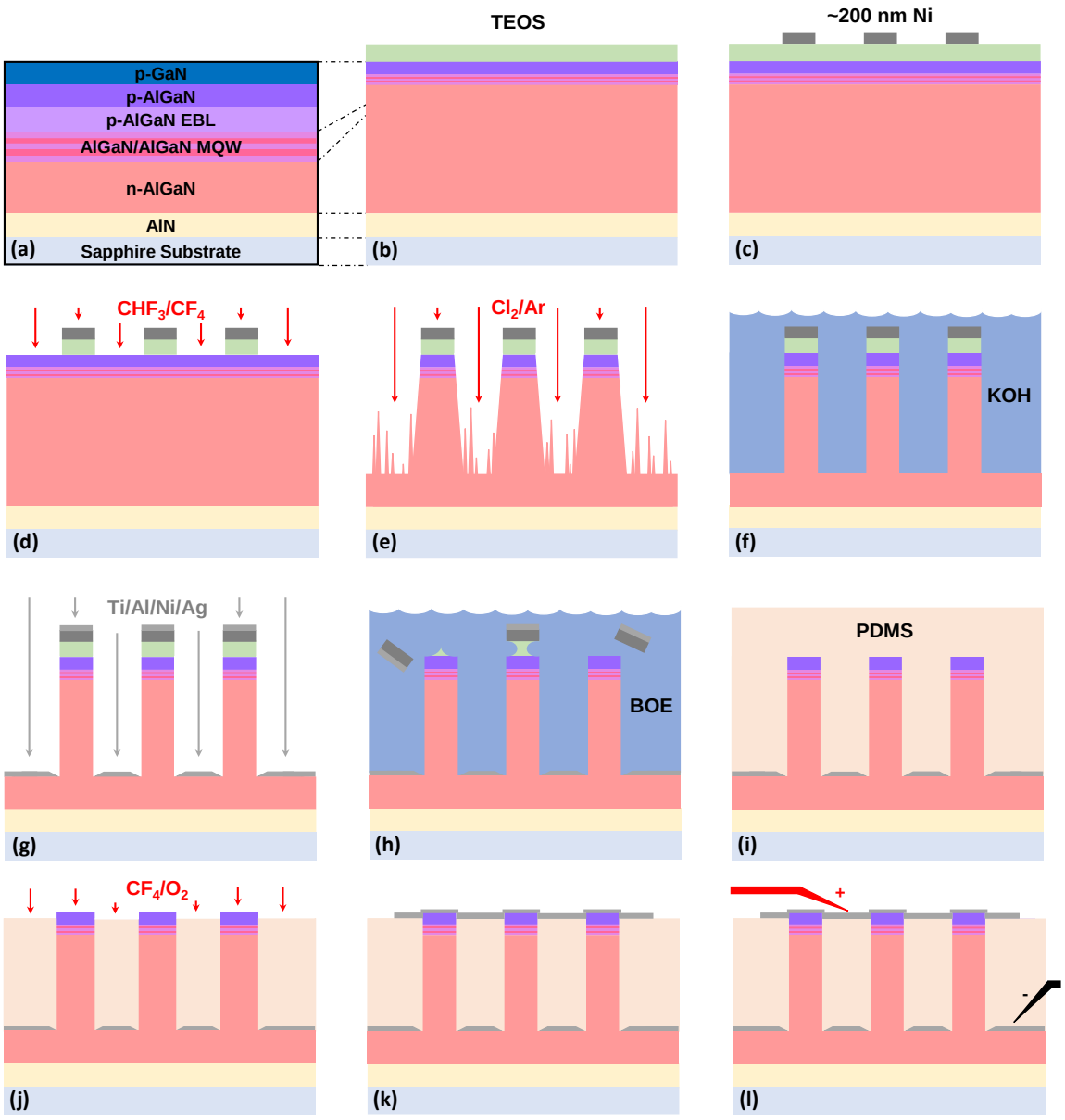

Figure 3.1.4: Nanowire LED fabrication schematic showing dry etch, wet etch, metallization, and dielectric planarization steps (not to scale).

tetraethyl orthosilicate (TEOS), is deposited across the entire sample using plasma-enhanced chemical vapor deposition (PECVD) to a thickness of ~300 nm (Figure 3.1.4(b)). The sample is then baked at 170°C for 3 min to remove hydrophobic surface states and is then given sufficient time to cool (~2 min) before application of LOR and photoresist. The resist is then patterned and developed, and Ni is deposited to a thickness

of ~100-200 nm (depending on the desired etch depth) using electron beam evaporation. The sample is then immersed in NMP for ~30 min to achieve liftoff the Ni. The Ni remaining on the sample will consist of discrete arrays of dots, ranging from 500 nm to 10 μm depending on the quality of the photolithography, which act as a double dry etch hard mask for etching of both the TEOS layer and the underlying GaN/AlGaN epitaxial layers (Figure 3.1.4(c)). The TEOS layer is then dry etched using a CHF_3/CF_4 plasma, with the etch self-terminating at the p-GaN layer as fluorine-based plasma has an extremely low etch rate against GaN (Figure 3.1.4(d)). The GaN/AlGaN etch is then performed using a $Cl_2/BCl_3/Ar$ plasma to etch to a depth of between 500 nm and 6 μm. This deep, high aspect ratio etch of AlGaN results in extensive micromasking, as shown in Figure 3.1.4(e), as well as extensive damage to the tapered sidewalls of the nanowires.

After completion of the dry etches, the sample is immersed in an aqueous hydroxyl-based solution consisting of 40% AZ400K at 80°C for up to 60 min. This crystallographic wet etch removes the micromasking and tapered base from the nanowires by attacking the semi-polar and non-polar wurtzite crystal planes of GaN and AlGaN, allowing for attainment of nanowires with perfectly vertical sidewalls, as shown in Figure 3.1.4(f). The sample, now free of micromasking, is ready for n-metal deposition. The vertical sidewalls of the nanowires allow for use of a "universal" n-metal, i.e. an un-patterned, continuous metal layer covering the entirety of the sample. This is possible because the nanowires themselves can act as a sort of shadow mask, preventing metal deposition on their own sidewalls, while allowing metal to coat the entirely of the exposed n-AlGaN at their bases. This technique only works if the metal deposition is almost perfectly directional, with the sample held stationary directly above the evaporation source.

A metal stack consisting of 30/100 nm Ti/Al/Au or Cr/Au is deposited using either thermal or electron beam evaporation, although thermal evaporation is preferred as it is the most directional (Figure 3.1.4(g)).

Following deposition of the n-metal, the sample is immersed in 10:1 buffered oxide etch (BOE) for ~5 min. The BOE rapidly etches the TEOS layer underlying the "metal cap," which consists of ~300 nm of metal after the addition of the n-metal stack onto the Ni dry etch hardmask. Removal of this metal cap is critically important, as a 300 nm metal layer will completely block the escape of light from the top of the nanowire. As the TEOS layer is etched by the BOE, the metal caps are removed from the nanowires and washed away in solution as shown in Figure 3.1.4(h), leaving "clean" nanowires with p-GaN exposed at their tips. Use of Au as the final layer of the n-metal stack is important, as Au is inert in BOE and will not etch, allowing it to protect the underlying metals, which have slow but finite etch rates in BOE.

Following removal of the metal caps, polydimethylsiloxane (PDMS) is spin-coated to a thickness of ~7 μm, covering the nanowires completely and self-planarizing to form a level surface as shown in Figure 3.1.4(i). The PDMS is then baked at 90°C for 11 min to crosslink the polymer and drive out any remaining solvent. A CF_4/O_2 plasma is then used to perform an "etch-back" of the PDMS until the tips of the nanowires are exposed (Figure 3.1.4(j)). This process is time consuming and must be performed with great caution so as not to etch the PDMS too far, which will result in shorting of the QW layer. When nearing the tips of the nanowires, a scanning electron microscope (SEM) is used to inspect the sample at 10-20 s etch time increments to determine if the nanowire tips have been exposed. The etched-back PDMS serves as an "interlayer dielectric," isolating the n-metal at the

base of the nanowires from the tips of the nanowires. Once the nanowire tips are exposed, the sample is coated with LOR and photoresist, and then patterned and developed. A thin, 20-40 nm layer of Ni is then deposited using thermal evaporation, serving as the p-contact and connecting nanowires in parallel to form nanowire array LEDs (Figure 3.1.4(k)). The sample is then tested using a manual probe station and parameter analyzer. Two probes are brought into contact with the sample, with one probe penetrating the PDMS layer to make contact to the n-metal, while the other probe is placed with extreme care to make contact to the thin p-metal layer. One disadvantage of using PDMS as an interlayer dielectric is its mechanical instability. PDMS is quite pliable at room temperature, and can be easily penetrated with an electrical probe, meaning that great care must be taken to avoid poking through the thin Ni layer when placing the p-contact probe. Once the probes are positioned, a positive bias is applied to the p-contact probe while the n-contact probe is held at ground in order to apply forward bias and illuminate the LED (Figure 3.1.4(l)).

3.2 Epitaxial Growth

The first step in the fabrication of any LED is epitaxial growth of the light emitting structure. This is usually accomplished through use of metal organic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE), techniques which allow for growth of nearly all III-V and III-Nitride materials with in-situ doping. MOCVD has seen widespread industrial adoption over the past few decades, as it is much more scalable than MBE and can support higher wafer throughputs [1]. Despite this, MBE does have several advantages over MOCVD. Unlike MOCVD, MBE has the ability to produce atomically abrupt material interfaces using physical shutters, which can instantly cut off the delivery of reactants/precursors to the sample surface. Despite exceptional advances in MOCVD

technology, the gas phase delivery of reactants characteristic of MOCVD systems can never achieve the same level of atomic abruptness as the physical deposition of MBE [2]. Additionally, because MBE system operate under extremely high vacuum, it is possible to use in situ growth characterization tools such as reflection high-energy electron diffraction (RHEED) to monitor the growth of epitaxial layers in real time. MOCVD tools, which operate under much higher reaction chamber pressure, cannot use this sort of in situ growth monitoring [2].

The lack of III-Nitride growth capabilities at RIT requires the use of external suppliers and collaborators. Precision Micro-optics, a commercial vendor based in Boston, MA, USA, provided almost all epitaxial wafers used in the research presented in this dissertation unless stated otherwise. These wafers were grown using MOCVD on either single side polished (SSP) or double side polished (DSP) sapphire wafers of thickness 430 µm (SSP) or 250 µm (DSP). A typical epitaxial stack for a DUV LED is shown in Figure 3.2.1. A 1-2 µm AlN buffer layer is first grown on a sapphire substrate to provide a

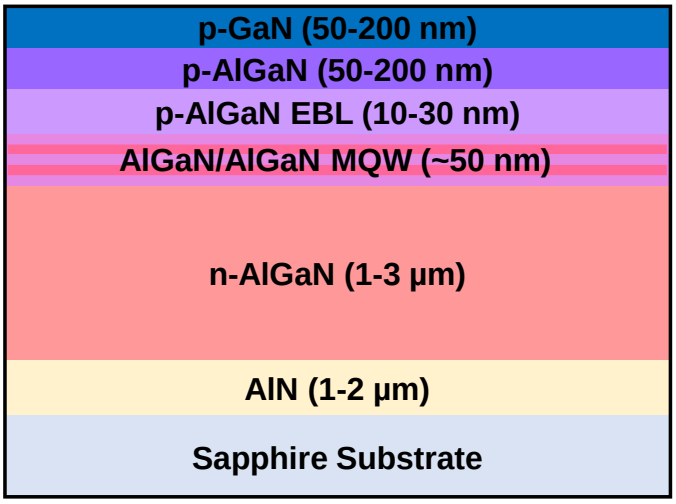

Figure 3.2.1: Representative DUV LED epitaxial stack grown either by MOCVD or MBE (not to scale).

"virtual substrate" of intermediate lattice constant, to reduce the amount of strain related dislocations, primarily threading dislocations (TDDs) generated during growth of the n-AlGaN layer. A 1-3 μm n-AlGaN layer, doped with Si, is then grown on the AlN buffer layer, followed by growth of the MQW, which consists of a series of 5-20 nm barrier layers and 1-5 nm QWs. An electron-blocking layer (EBL) is then grown, consisting of high Al-content AlGaN, to a thickness of 10-30 nm to impede leakage of electrons into the p-AlGaN. A 50-200 nm p-AlGaN layer is then grown, followed (sometimes) but a highly doped p-GaN layer to improve p-contact resistance. The compositions of the various layers vary depending on the desired emission wavelength, but QW Al composition generally varies between 40% and 70% for emission wavelengths of between 280 nm to 240 nm. Figure 3.2.1 shows a not-to-scale schematic of a representative DUV LED epitaxial stack.

3.3 Photolithography

Photolithography is a critically important process in the fabrication of LEDs and all other microelectronic devices. It is, in the simplest sense, the use of light to create patterns on a wafer or sample. This is accomplished using a photosensitive polymer called "photoresist" (PR), which is applied to the sample through a process called "spin-coating" in which the PR, usually of similar consistency to syrup, is dispensed onto the middle of the sample with a syringe or pipet. The sample is then spun at several thousand rpm for 30-60 seconds in order to spread the PR over the entire sample surface. The spin speed and acceleration determine the thickness to which the PR will coat, which is typically in the range of several hundred nanometers to around ten microns. Higher viscosity resists will coat thicker than lower viscosity resist at the same spin speed. After the sample is coated with PR, it is "soft-baked" at around 100°C for several minutes in order to drive out any

solvent remaining the thinned layer of PR. The PR layer is then exposed to ultraviolet light in order to transfer patterns onto the sample. Photoresist contains photosensitive chemicals, which undergo chemical reactions when exposed to certain wavelengths of UV light. In a "positive" PR, regions exposed to UV light will undergo chemical reactions that break bonds in the polymer chains, making those regions soluble in certain chemicals which will not dissolve the unexposed resist. Likewise, in "negative" PR, regions exposed to UV light will crosslink, becoming insoluble in chemicals which would otherwise dissolve the unexposed resist.

The wavelength of light needed to expose different resists depends on the photosensitive compound used. Photoresist is designed to be sensitive to a specific wavelength or wavelength range. Only a handful of wavelengths exist in the UV range which are suitable for use in photolithography. These include the mercury lamp emission lines (436 nm g-line, 405 nm h-line, and 365 nm i-line), as well as excimer laser emission wavelengths (351 nm XeF, 248 nm KrF, 193 nm ArF, 157 nm F_2, and many others) [3]. After the sample is exposed, it is subjected to a "post-exposure bake" (PEB), which provides the thermal energy necessary for completion of the chemical reactions initiated by UV light exposure. The sample is then immersed in a "developer," which dissolves the exposed areas of positive PRs, or the unexposed areas of negative PRs. At this point, the pattern is now present on the sample surface, and can be used to mask a wet or dry etch of the sample. A summary of the coating, baking, exposure, and development parameters for the various PRs used in this dissertation is provided in Table 3.1, while more detailed descripted of the various lithography techniques available at the SMFL are given in the following sections.

Table 3.3.1: Photoresist Process Parameters

	Type (POS or NEG)	Coat Speed (rpm)	Coat Time (s)	Coating Thickness (nm)	Soft-bake temp/time (°C/s)	Heidelberg Exp. Pwr. (mW)	PEB temp/time (°C/s)	Develop time (s)
AZ 1512	POS	3000	30	~1500	100/120	70	110/120	120
AZ 1505	POS	4500	30	~500	100/120	55	110/120	60
AZ MIR 701	POS	3000	30	~1100	100/120	220	110/60	60
LOR 5A	NA	2700	45	~600	170/300	NA	NA	+60

3.3.1 Nanosphere Lithography

While photolithography is the most commonly used technique for producing nanometer or micron-sized features on a sample, another technique known as "nanosphere lithography" can also be used. In nanosphere lithography, an aqueous solution of nanospheres (SiO_2 nanospheres in this dissertation) is spin coated onto the surface of the sample. The density of nanospheres remaining on the surface after spin coating depends primarily concentration of spheres in the coated solution. The sample can then be dry etched using the randomly positioned spheres as an etch mask capable of withstanding fairly deep etches into GaN with a $Cl_2/BCl_3/Ar$ plasma. This approach is ideal for optimizing dry etch recipes and determining etch rates for new materials as it is much

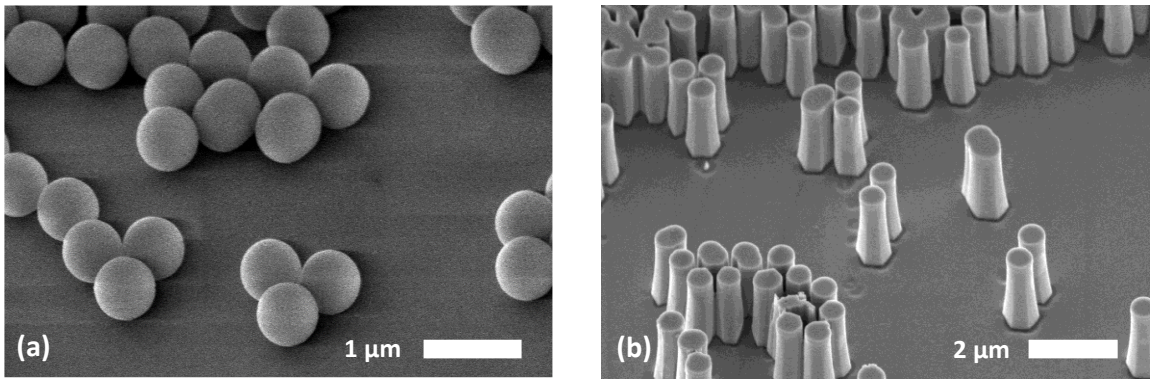

Figure 3.3.1: 700 nm SiO_2 nanospheres on a GaN surface (a). 3 µm tall GaN nanowires formed using 700 nm SiO_2 nanospheres as a dry etch mask (b).

simpler and easier to perform than photolithography. The obvious downside is that the nanospheres are located randomly on the surface of the sample, and cannot withstand very deep etches as effectively as a Ni hardmask can. Figure 3.3.1 shows nanospheres on GaN (Figure 3.3.1(a)) and nanowires formed using nanospheres as a dry etch mask (Figure 3.3.1(b)).

3.3.2 Contact Lithography

The simplest form of photolithography is contact lithography, in a which glass plate covered in patterns made of a thin layer of chrome is placed directly in contact with the sample. The UV light source is then used to illuminate this "contact mask" such that areas of the mask not covered in chrome will allow light to pass through, exposing the sample, while chrome-covered areas reflect the light, protecting those areas of the underlying sample. The chrome mask is created by first covering the entire glass plate in a thin layer of chrome. A special PR is then coated over the chrome, and extremely high-resolution electron beam lithography (or laser direct write lithography) is used to expose the resist with the desired patterns. The PR is then developed and used to mask a wet etch of the underlying chrome, which transfers the desired patterns into the chrome layer. Contact lithography is cheap, simple, and relatively fast, but has limited resolution, making it ideal of fabrication of devices with large dimensions that do not require extremely precise alignment. Two contact aligners are available in the to our research group, a Suss MA-150 mask aligner with an i-line filter, capable of features sizes down to 1 μm, and a Suss MJB4 mask aligner capable of features down to 2 μm.

3.3.3 g-line Projection Lithography

Projection lithography is similar to contact lithography in that it uses a chrome mask to define the desired patterns. In projection lithography, UV light is collimated using a condenser lens and directed onto the mask. After passing through the mask the light is focused by an objective lens and demagnified by reducing optics before exposing the sample [3]. The use of reduction optics allows the dimensions of features on the mask to be reduced in size on the sample [3]. For example, 5x reduction projection lithography can use a mask with 10 μm lines to write 2 μm lines on the sample. Projection lithography is typically achieved using a tool called a stepper, which moves the sample around on a piezo-driven stage beneath the optical column to allow different parts of the wafer to be exposed. Since most projection lithography systems use reduction optics to achieve higher resolution, it is not possible to expose the entire sample at once, and as such, a series of identical "die" are exposed on the sample by moving to beneath the optical column of the stepper using the piezo stage. Projection lithography can be extremely complex, and the optical components used in modern state of the art projection lithography systems are the most advanced in the world. Modern UV projection lithography systems use tricks such as off-axis illumination, phase shift masking, and high index immersion oils to achieve extremely high resolutions [3]. Recently, extreme ultraviolet (EUV) lithography has begun replacing UV lithography in state-of-the-art applications that require sub-10 nm resolution, for example in the foundries of Intel and TSMC. EUV lithography uses a wavelength of 13.5 nm, 10x shorter than the wavelengths used in UV lithography [3]. Two projection lithography tools are available to our research group, a GCA g-line stepper capable of processing 6-inch wafers, 4-inch wafers, 2-inch wafers, and pieces at resolutions down to

800 nm, and an ASML PAS 5500/200 stepper capable of processing 6-inch wafers at resolutions down to 250 nm.

3.3.4 h-line Laser Direct Write Lithography

Laser direct-write, or LDW lithography is a form of mask-less photolithography which uses a laser to expose photoresist. In LDW lithography, a resist-coated sample is placed on piezo-stage beneath a fixed write-head containing focusing and scanning optics for the laser. The sample is then driven by the stage along the y-axis while the laser rasters on the x-axis, turning on and off in order to expose the desired pattern on the sample in a process called stripe-exposure. The stripe width is determined by the maximum raster angle of the laser and the distance from the raster mirror and the sample surface. The maximum raster angle can be changed to allow for stripe widths of up to several hundred microns on most LDW systems. Larger stripe widths allow for faster write times, while much smaller stripe widths allow for higher resolution. LDW systems are often used as cheaper alternatives to electron beam lithography for writing contact and projection masks. The main advantage of LDW lithography is the ability to write patterns on masks, wafers, or small samples without a mask, making it ideal for rapid prototyping of new designs. However, this ability comes at the tradeoff of extended exposure times, with most patterns taking much longer to expose on an LDW system than with contact or projection lithography. For example, a 2-inch wafer that might take 10 to align and expose on a contact aligner can take up to 6 hours to expose using an LDW system depending on the minimum desired feature size. An h-line Heidelberg DWL-66+ LDW system is available in the SMFL and is capable of resolutions down to ~1 μm when using 500 nm resists. Our research group relies heavily on this system, and uses it to pattern the majority of our

samples. While the tool has a theoretical resolution of 1 μm, we have found this difficult to achieve for many types of patterns. For example, the patterning of arrays of nanowires often requires many small holes to be exposed in PR. The tool has difficulty doing this due to its inability to correct for focal point offset along across the width of the raster stripe. This leads to holes being underexposed at the edges of a stripe, and fully exposed in the middle, which translates to variable nanowire diameter across the stripe width, which is very undesirable in almost every situation. This issue can be partially compensated for by reducing the stripe width, but doing so drastically increasing the write time for our samples.

3.3.5 Liftoff Lithography

Liftoff lithography is a special technique which is often used to pattern metal thin films. In liftoff lithography, a layer of "liftoff resist" or LOR, is first coated onto the wafer and baked at ~170°C for 5 min. Photoresist is then coated onto the LOR, and the combined LOR + PR layer is then soft baked, exposed, post exposure baked, and developed. LOR is not photosensitive, and so does not change the dose required to exposure the PR. During development, once the PR layer is rapidly dissolved in exposed regions (assuming a positive PR), the developer begins to dissolve the LOR. Because LOR is soluble is developer whether it has been exposed or not, an undercut will develop as LOR is removed in unexposed regions. The longer the sample is developed, the larger the undercut will be, although an undercut of ~1 μm is typically targeted for LOR 5A, which coats to a thickness of around 600 nm. After development, and immediately prior to metal deposition, the sample is "descummed" using a low power (~50 W) O_2 plasma in order to remove any photoresist residue present in the developed regions. Following this descum step, a short (~30 second) dip in diluted (10-25%) HCl can be performed to remove any native oxide

which has formed on the GaN/AlGaN surface to improve the contact resistance of the to-be-deposited metal. The sample should be loaded into the evaporation chamber and brough under vacuum as soon as possible following this HCl dip in order to minimize the re-formation of oxides on the surface. Metal deposition, performed with either thermal or electron beam evaporation, will occur on the sample in exposed regions, and on the PR in unexposed regions. After metal deposition, the sample is placed in a solvent to strip the PR and remove the metal on top of the PR. Due to the undercut in the LOR, the metal film is not continuous and solvent is able to access the PR beneath the undercut, removing the PR and LOR and "lifting off" the metal on top of the PR. This method is extremely useful as it allows for metal layers to be patterned without the need to dry or wet etch the metal. In many cases, etching of metal films can be very difficult or even impossible depending on the sensitivity of the underlying material to the metal wet/dry etchant chemistry.

3.4 Dry Etching

GaN and its alloys are most effectively etched using a Cl_2 plasma dry etch. Dry etching is performed by supplying capacitive or inductively coupled RF-energy (or a combination of both) to a gas to ignite a plasma. Ions (usually cations) are then accelerated out of the plasma across the sheath potential and impact the sample, resulting in directional physical "sputter" etching, while neutral radicals thermally diffuse out of the plasma to the sample surface and provide anisotropic chemical etching. The volatile byproducts of etch are then removed from the etch chamber. In this way, a plasma can be used to "etch" down into a material.

Two types of dry etch are possible and are differentiated by the way in which RF energy is supplied to the plasma. In a capacitively coupled plasma (CCP) dry etch, a radio

frequency (usually 13.56 MHz) electric field applied between two parallel plates, stripping the electrons from neutral gas molecules/atoms. These electrons are then heated by the alternating RF electric field and gain sufficient thermal energy to cause impact ionization of additional gas molecules/atoms, igniting a plasma once the ionization ratio passes a certain threshold which depends on the gas mixture and pressure. A plasma sheath develops between the plasma cloud and the chamber sidewalls/electrodes in order to balance the flux of electrons and cations to the chamber sidewalls. More information on sheath formation and physics can be found in [4]. In a system with equally sized top and bottom electrodes, the sheath width and potential drop will be symmetric, causing cations to be accelerated out of the plasma towards both electrodes with equal energy. By electrically isolating the lower (sample holding) electrode and making it smaller, while also enlarging the upper electrode and tying it to the chamber sidewalls, it is possible to make the lower electrode much smaller than the upper. This makes the sheath width much larger over the lower electrode and increases the sheath potential and kinetic energy of cations accelerated into the sample. In this way, sputter etching of the top electrode and chamber sidewalls can be minimized while increasing the physical etch rate at the sample surface. The primary downside of this approach is that plasma density and sheath potential are directly coupled to one another, such that increasing the RF energy delivered to the plasma increases the electron/cation density while also increasing the sheath potential and physical etch rate. In a CCP etcher, it can thus be difficult to achieve high chemical to physical etch ratios, limiting the flexibility of these systems.

In an inductively coupled plasma (ICP) dry etch, RF energy is supplied by time varying electric currents produced by electromagnetic induction. The induction coils in an

ICP etcher are electrically isolated from the etch chamber by a dielectric window, usually glass or another ceramic material, which allows RF energy to be supplied to the plasma cloud without affecting the sheath potential. In most ICP etchers, a secondary RF power supply is also connected in CCP configuration, so that sheath potential can be controlled as well. This allows the density of the electrons/cations in the plasma to be controlled independently from the sheath potential, offering increased parameter space flexibility to the etch process. One major benefit of ICP etching is the ability to operate with very high plasma density over a wide range of pressures, which can allow almost purely chemical plasma etching to be performed.

A number of dry etch tools are available in the SMFL, including two CCP tools, two hybrid ICP/CCP tools, and an ICP oxygen asher. Dry etching of GaN and AlGaN in the SMFL is performed with a Plasmatherm Apex ICP plumbed with Cl_2, BCl_3, Ar, He, O_2, and N_2. Etch rates of between 200 and 700 nm/min can be achieved for GaN and AlGaN depending on the etch parameters, which are summarized in Table 3.4.1. Dry etches are typically masked using photoresist, SiO_2, or in the case of GaN, Ni. In addition to dry etching of GaN, SiO_2 and PDMS etches are often used in our LED fabrication, and generally use some type of fluorine-based plasma. The etch parameters for SiO_2 and PDMS are also summarized in Table 3.4.1. Dry etches are also used to remove organic materials

Table 3.4.1: Dry Etch Process Parameters

	Gases	Gas flow (sccm)	Pressure (mtorr)	Plasma Power (W)	Tools
GaN/AlGaN	$Cl_2/BCl_3/Ar$	32/8/5	10	75/300 RF/ICP	Plasmatherm Apex ICP
SiO_2	$CHF_3/CF_4/O_2$	70/60/8	130	200 RF	Trion Minilock CCP, Trion Phantom CCP
PDMS	CF_4/O_2	40/20	100	275 RF	Trion Minilock CCP
O_2 Ash	O_2	20-300	100-300	400-900 ICP	Trion Phantom CCP, Trion Apollo ICP Asher
O_2 and F Ash	O_2/CF_4	20-100/5	100-300	150 RF	Trion Phantom CCP
Descum	O_2	20	120	50 RF	Trion Minilock CCP, Plasmatherm Apex ICP

such as photoresist from wafers, these “ash” and “descum” etch parameters are also given in Table 3.4.1.

3.5 Wet Etching

Wet etching of GaN and AlGaN is critically important following a plasma dry etch, especially for high aspect ratio structures such as nanowires. The lack of a lattice matched growth substrate for GaN and AlGaN means that the dislocation related defect density is very high in GaN and AlGaN. These dislocations can reduce the dry etch rate in their locality, forming micro masked etch grass structures as described in Section 3.1.2. Additionally, the sidewalls of high aspect ratio GaN and AlGaN structures usually exhibit an undesirable tapered profile following dry etch, as well as significant surface damage, which contributes to increased surface recombination and reduced IQE. For these reasons, a crystallographic, hydroxyl based wet etch is required to remove etch grass, straighten structure sidewalls, and remove dry etch damage. The effectiveness of hydroxyl-based etch chemistries has been extensively documented, and is currently used in industrial scale fabrication of GaN power electronics and LEDs [5–10]. These chemistries do not etch Ga-polar surfaces, such as the c-plane (0001) of wurtzite GaN and AlGaN alloys, instead rapidly etching the semi-polar r-planes $(10\bar{1}1)$ until the non-polar $(10\bar{1}0)$ plane is revealed, which is then etched more slowly [11]. This unique crystallographic etch rate variation is due to differences both the surface polarity as well as the surface energy/dangling bond density of the surface. Surfaces which develop higher densities of electronegative dangling bonds (such as the c-plane), will repel hydroxyl ions in solution, preventing them from accessing the surface and lowering the etch rate [5,7,11]. This allows these chemistries, typically based on KOH or tetra-methyl ammonium hydroxide (TMAH), to rapidly etch

structures unprotected by the c-plane, such as etch grass, as well as the tapered sidewalls of nanowires and other high aspect ratio structures. Immersion of dry etched GaN and AlGaN samples in these chemistry can lead to complete removal of etch grass and attainment of perfectly vertical, crystallographically smooth sidewalls in between 10 to 30 min. Figure 3.5.1 shows two samples before and after a 30 min etch in 2 wt.% KOH at 80°C. The difference between Figs. 3.5.1(a) and (b) and Figs. 3.5.1(c) and (d) demonstrates the effectiveness of the wet etch at removing etch grass and producing crystallographically smooth sidewalls.

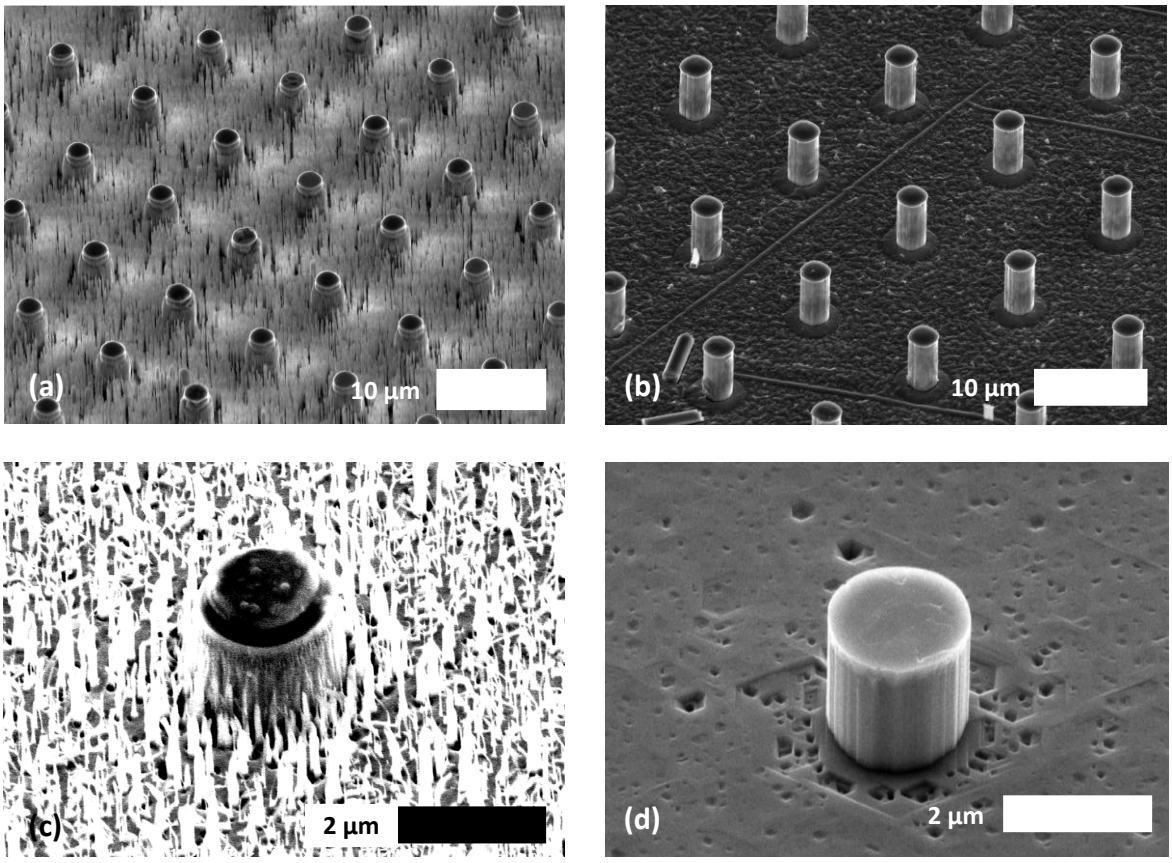

Figure 3.5.1: GaN nanowires before (a, c) and after (b, d) a 30 min etch in 2 wt.% KOH at 80°C.

All nanowire LED samples fabricated in the SMFL are subjected to a KOH-based etch to remove etch grass, straighten nanowire sidewalls, and remove dry etch damage. Most planar mesa LEDs are also wet etched, although this step is less necessary for these structures, which are only dry etched to a depth of a few hundred nanometers and exhibit negligible micromasking. The wet etch is performed by mixing 1:4 or 2:3 AZ400K (a photoresist developer containing 2 wt% KOH) and DI water to create a 20% or 40% AZ400K solution. The solution is mixed in a Pyrex griffin beaker and heated on a hotplate to a temperature of ~80-90°C. The sample to be etched is placed in Teflon dipper and suspended several millimeters over the surface of the mixed solution. Al foil is then used to seal the top of the beaker around the handle of the dipper to prevent evaporation of the heated solution. A PID thermocouple is then inserted through the Al foil into the solution to control the heating of the solution. The solution is stirred with a Teflon coated stir bar at 300-500 rpm to maintain uniform concentration throughout and ensure delivery of fresh etchant to the sample surface. Once solution has reached the temperature setpoint of between 80°C and 90°C, the sample holding dipper is lowered into the solution without removing the Al foil until the sample is submerged ~1 cm below the surface.

Etch times of 5-10 minutes are generally sufficient for removal of most etch grass, while most unwanted post-dry-etch tapering can be removed in 20-40 min. Extended etch times have been found to slowly reduce the diameters of nanowires and micropillars, offering the useful capability to achieve diameters smaller than those attainable with our in-house lithography capabilities. However, this “shrinking” of the nano and microstructures was found to only be possible in the absence of the dry etch mask. When a dry etch mask, either Ni or TEOS, is left on smaller structures during KOH etching,

diameter reduction is prevented entirely as the etch solution is denied access to the "corner" of the structure where the vertical m-plane, which etches very slowly, meets the horizontal c-plane, which does not etch. Slow etching of the m-plane has been found to initiate from the top of the structure at this c/m-plane interface, so when the c-plane is covered in an inert metal or dielectric, this etch mechanism is effectively terminated. More information on the shrinking of GaN/AlGaN nanowires and micropillars can be found in our group's 2023 publication "*Analytical Study of KOH Wet Etch Surface Passivation for III-Nitride Micropillars,"* by Matthew Seitz *et al* [12].

After completion of the etch, the foil and thermometer are removed, and the sample is transferred into a beaker of room temperature DI water. After ~5 min in DI water, the sample is transferred to a fresh beaker of DI water and is agitated for an additional 2 min to ensure complete removal of any etch byproducts from the sample surface. The sample is then removed from the DI water and quickly dried with N2. Our group has extensively characterized the effects of AZ400K/KOH concentration and solution temperature on the both the etch rate and etched surface roughness of GaN and AlGaN. In general, lower AZ400K concentrations produce smoother etched surfaces and are more desirable when surface passivation is required but come at the expense of lower etch rates. Temperature was found to have little effect on surface roughness, primarily effecting etch rate. Temperatures of 80-95°C were found to be ideal, with etch rate showing a general logarithmic relationship with temperature. 80-85°C was found to be the easiest to use, as higher temperatures cause increased evaporation of the solution, leading to a messier, less controllable process. Etch rates decreased significantly below 75°C, and while room temperature AZ400K solutions are capable of etching GaN and its alloys, room

temperature etches rates are so low that days or weeks of immersion are required to produce any noticeable etch progress [8]. For example, a quick, rough etch aimed at removing etching grass from a mesa LED sample could be performed in 40% AZ400K at 90°C in about 5 min, while a slow, smooth etch of high aspect ratio nanowires or micropillars could be performed in 10-20% AZ400K at 80°C in 45-120 min. More details on KOH etching of GaN, AlGaN, and InGaN can be found in our group's 2019 and 2023 publications *"Effect of KOH passivation for top-down fabricated InGaN nanowire light emitting diodes,"* by Matthew Hartensveld *et al.* [5], and "*Analytical Study of KOH Wet Etch Surface Passivation for III-Nitride Micropillars,"* by Matthew Seitz *et al* [12].

In addition to crystallographic KOH etching of GaN and AlGaN, several other wet etches are often performed during fabrication of LEDs in the SMFL. Etching of SiO_2, deposited either by plasma enhanced chemical vapor deposition (PECVD) or atomic layer deposition (ALD), is etched using 10:1 buffered oxide etched (BOE). BOE is used instead of 49% HF because it provides a slower, more controllable etched rate. In the SMFL BOE contains a 6:1 volume ratio of 40% aqueous NH_4F (the buffering agent) to 49% aqueous HF. This "stock" BOE is then diluted 10:1 in DI water to provide an even slower, more controllable etch rate. This solution will etch densified TEOS and ALD SiO_2 at 100-140 nm/min depending on etch bath age. In addition to wet etching of SiO_2 and TEOS, an Al wet etch is sometimes used. This etch is performed in a bath consisting of ~5% HNO_3, 70% H_3PO_4, 5% CH_3COOH, and 20% DI water heated to 85°C. Etch rates of around 300 nm/min against evaporated and sputtered Al films are generally obtainable with this chemistry. Etching of Ni can be performed in 25% HCl at room temperature with etch rates of ~50-100 nm/min. It is of note that Ni films which have been used as an etch mask for

Cl_2 plasma etches in excess of several minutes are inert in HCl solutions due to the formation of Ni_xCl_y compounds on the surface of the metal during plasma etching [13]. These films can be removed by Ar sputter etching at the end of the Cl_2 etch process, but this workaround has not been characterized in depth.

3.6 Thin Film Deposition

Thin film deposition encompasses deposition of both metals and dielectrics such as SiO_2. Metal deposition is generally accomplished through use of either thermal evaporation, electron beam evaporation, or sputtering, while dielectrics can be deposited through room or low-pressure thermal growth (for example tube furnace thermal SiO_2 or low-pressure chemical vapor deposition (LPCVD) Si_xN_y), plasma enhanced chemical vapor deposition (PECVD), atomic layer deposition (ALD), sputtering, or electron beam evaporation (in rare cases). Thin film deposition is a critical capability in semiconductor device manufacturing and is equally important in the fabrication of mesa and nanowire LEDs. During fabrication of LEDs in the SMFL, metal contacts and etch masks are deposited through either thermal or electron beam evaporation, while dielectrics such as tetraethyl orthosilicate (TEOS) and Si_3N_4 are deposited as passivating layers using PECVD. Indium Tin Oxide, a transparent conductor, is also sometimes deposited using sputtering.

3.6.1 Thermal Evaporation

In thermal evaporation, small metal pellets or wire segments are placed in a "boat," which is generally 5-10 cm in length and several centimeters wide with a small depression in the middle. Evaporation boats are typically made of a refractory metal such as W, Mo,

or Ta to allow them to withstand the temperatures needed to melt the metal being evaporated. Boats may also be coated with alumina or other ceramics to control wetting of metal melt and extend the life of the boat. The boat is clamped between two electrodes capable of supplying hundreds of amps of current. The sample is then placed above the boat and the entire system is pumped down to high vacuum, generally around $1\text{-}5x10^{-7}$ torr using a combination of a roughing pump and either a cryo-pump or a turbo-pump. Once sufficiently high vacuum is achieved, resistive heating is used to heat the boat by flowing current through it. The heat is transferred to the metal within the depression on the boat, which has a lower melting point than the boat material. When the metal melts, its vapor pressure increases, allowing metal atoms to escape the surface of the melt and producing a measurable flux of metal atoms at the sample surface. A crystal detector is placed near the sample and measures the instantaneous deposition rate and total run to run deposition thickness. As metal is deposited on the sample and crystal simultaneously, the mass of the crystal increases, changing its resonant frequency and allowing instantaneous mass change to be measured and converted to a deposition rate by knowing the density and Z-ratio of the metal. Deposition rates can range from 0.1 to 100 Å/s, with higher melt temperatures leading to higher deposition rates. The distance between the sample and the boat plays a key role in determining the deposition rate, which scales roughly with the inverse cube of r, the source-sample distance. Halving r will result in a roughly 8x increase in deposition rate. The custom-built thermal evaporator in the SMFL has a source-sample distance of roughly 40 cm, and deposition rates of between 0.5 and 5 Å/s are usually targeted. The physics governing the finer details of metal evaporation are quite complex and are beyond

the scope of this explanation. More information on metal evaporation physics can be found in [14,15].

3.6.2 Electron Beam Evaporation

In electron beam evaporation, metal is placed in a water cooled "crucible," made of either carbon or a refractory metal such as W or Mo. The sample is then placed above the crucible and the system is evacuated to at least $1x10^{-5}$ torr. An electron beam is then generated with the vacuum chamber and steered into the crucible using a set of electromagnets. The electron beam strikes the metal in the crucible, causing intense heating at the site of impact and melting the metal. The electromagnets are used to raster the beam across the surface of the metal to melt a wider area and increase deposition rate. The evaporating metal atoms then deposit on the sample, and deposition rate is measured with a crystal monitor similarly to thermal evaporation. Electron beam and thermal evaporation are similar in many ways but have a few key differences. While thermal evaporation requires very large electric current to heat a boat and metal the metal contained in it, electron beam evaporation can be used to evaporate metals at a much lower vacuum pressure by causing localized heating of the target metal. It is thus more effective for evaporating high melting point metals such as Ni and Ti. In most electron beam and thermal evaporation systems, the crucibles or boats are placed a carousel system which can be rotated to allow for evaporation of multiple different metals without venting the chamber. Samples can be mounted on a rotating "planetary" system within the vacuum chamber to achieve a more isotropic, non-directional deposition if required.

3.6.3 Sputtering

In addition to evaporation, sputtering can also be used to deposit metal on a sample. In sputtering, a plasma, generally composed primarily of inert Ar^+ ions, is generated between two electrodes. A metal target is placed over one of the electrodes, while the sample is mounted over the other electrode such that it is facing the target. As in CCP dry etching, an RF electric is applied between the two electrodes striking and sustaining a plasma. In contrast to CCP plasma etching, the sample holding electrode is made much larger than the target holding electrodes, such that cations (usually Ar^+) are selectively accelerated into the target instead of the sample. The ions impact the target surface, transferring their momentum to metal atoms which are ejected from the target surface and deposited on the sample. Sputtering is often used when deposition of conformal or semi conformal films is required. Sputtering can also be performed at much higher pressures than evaporation, making it much faster due to lack of the extended pump times which are needed for electron beam and especially thermal evaporation. One downside of sputtering is that large, expensive sputter targets are required, making it difficult to use of deposition of rare, expensive metals such as Au and Ag.

3.6.4 Dielectric Deposition

Dielectric deposition is also very important in the fabrication of more complex mesa and nanowire LEDs. Dielectrics such as silicon dioxide (SiO_2), silicon nitride (Si_3N_4), and aluminum oxide (Al_2O_3) are used for electrical isolation of different metal levels, hard mask materials for dry etches, and sacrificial layers for liftoff of unwanted metal as described in Section 3.1.2. These materials can be deposited is several ways. The most basic method of dielectric deposition is chemical vapor deposition (CVD), in which the

sample is placed in a quartz tube through which precursor gases such as silane (SiH_4), ammonia (NH_3), aluminum chloride ($AlCl_3$), oxygen (O_2), and nitrogen (N_2) are flowed. The quartz tube is heated to a very high temperature (usually > 700°C), heating the gases inside the tube such that they react/decompose on the sample surface, forming a thin film of the desired dielectric.

Plasma enhanced chemical vapor deposition (PECVD) is more commonly used in the SMFL and is similar to CVD in many ways. In PECVD, precursor gases are mixed in a vacuum chamber and ionized using RF electric fields. The combination of hot reactive ions and neutral radicals produced in the plasma allows dielectric films to be deposited at much lower temperatures, usually 350°C but sometimes as low as 200°C. This allows for deposition of dielectrics on temperature sensitive samples such as integrated circuits and quantum well epistructures. SiO_2 and Si_3N_4 are commonly deposited via PECVD, but other films, such as the SiO_2 derivative tetraethyl orthosilicate (TEOS) can also be deposited.

Atomic layer deposition (ALD) uses pulsed gas flow and high temperatures to build extremely ordered, high quality thin films one atomic layer at a time. ALD is completely conformal and can easily coat overhanging surfaces with near mono-crystalline thin film. The major disadvantage of ALD is its deposition rate of only several nanometers per minutes or less. While this makes ALD nearly useless for creating thick dielectric films, it is ideal for formation of very thin films which require very tight tolerates, such as gate dielectric layers for transistors.

3.7 Interlayer Dielectric Application and Planarization

A critical step in the fabrication of nanowire and micropillar LEDs is the deposition, planarization, and etch back of the interlayer dielectric. This dielectric “interlayer” isolates

the n-metal at the bases of the nanowires from the p-metal at the tops of the nanowires and provides a platform for deposition of the p-metal. Without this layer, electrical operation of etched nanowire and micropillar LEDs would not be possible. Our group has used two distinct approaches, discussed in the following sections, for interlayer formation.

3.7.1 PDMS Etchback

Polydimethylsiloxane, or PDMS is a polymeric organosilicate which is transparent in the DUV range and inert in most wet etch chemistries and solvent. In nanowire LED fabrication, PDMS is spin coated onto the sample following nanowire formation and n-metal deposition. PDMS coats to a thickness of ~7 μm, and self-planarizes nanowires and other structures. After it is spin coated, an 11 min bake at 90°C is performed to drive out any remaining solvents and crosslink the polymer chains. The PDMS layer is then "etched-back" to expose the tips of the nanowires as described in Section 3.1.2. A CF_4/O_2 plasma is used to etch the PDMS in short increments, with SEM and AFM used to determine when the nanowire tips are exposed. After the nanowire tips are exposed, the p-metal can be deposited on top of the PDMS to form nanowire array LEDs. While PDMS works reasonably well as an interlayer dielectric for nanowire LEDS, it is not optimal for a number of reasons. Etch back of PDMS can often prove difficult as the polymer surface tends to roughen after extensive dry etching. This leads to formation of particulate-like structures on the surface of the material which can adversely affect SEM imaging and subsequent devices performance. The coating thickness of PDMS is also affected by the density of the arrays over which it coats, as well the position on the sample. It will coat thicker over denser arrays and in the central regions of the sample. This causes the density of arrays and their position on the sample to impact the clear time (the amount of dry

etching required to expose the tips of structures). As the tolerance for a successful clear on a single array is very tight due to the p-GaN layer of the epistack being only several hundred nanometers thick, is becomes impossible to simultaneously clear (but not over clear) all arrays. In general, less than 20% of the arrays on a given sample can be successfully cleared at once, severally limiting the number of functioning, testable devices. Additionally, while PDMS is fairly chemically and thermally robust, it remains a non-rigid polymer, making testing of devices difficult as it is very easy to puncture the PDMS layer while attempting to probe p-metal on top of it. This also makes wire bonding impossible for devices which use a PDMS interlayer dielectric. As such, a more robust approach is needed.

3.7.2 TEOS Planarization and Etchback

An alternative to spin on dielectrics like PDMS is to use dielectrics such as SiO_2 and Si_3N_4, which are deposited conformally via low pressure chemical vapor deposition (LPCVD) or plasma enhanced chemical vapor deposition (PECVD). These materials are used extensively in semiconductor devices and exhibit excellent thermal and mechanical stability. Unfortunately, the conformal deposition of these materials leads to significant surface topology on the surface of the overcoating dielectric layer which is not removed during the dielectric etch back process. This topology often manifests as “hills” over each nano/microstructure, which corresponds “valleys” between them, as can be seen in Figure 3.7.1. During the subsequent etch back used to expose the tip of the structures, this topology is preserved and can cause the dielectric layer to experience etch punch through at the bottom of the valleys, causing shorting of the p-contact layer and the n-GaN/n-contact. Additionally, conformal dielectric deposition can also results in discontinuities

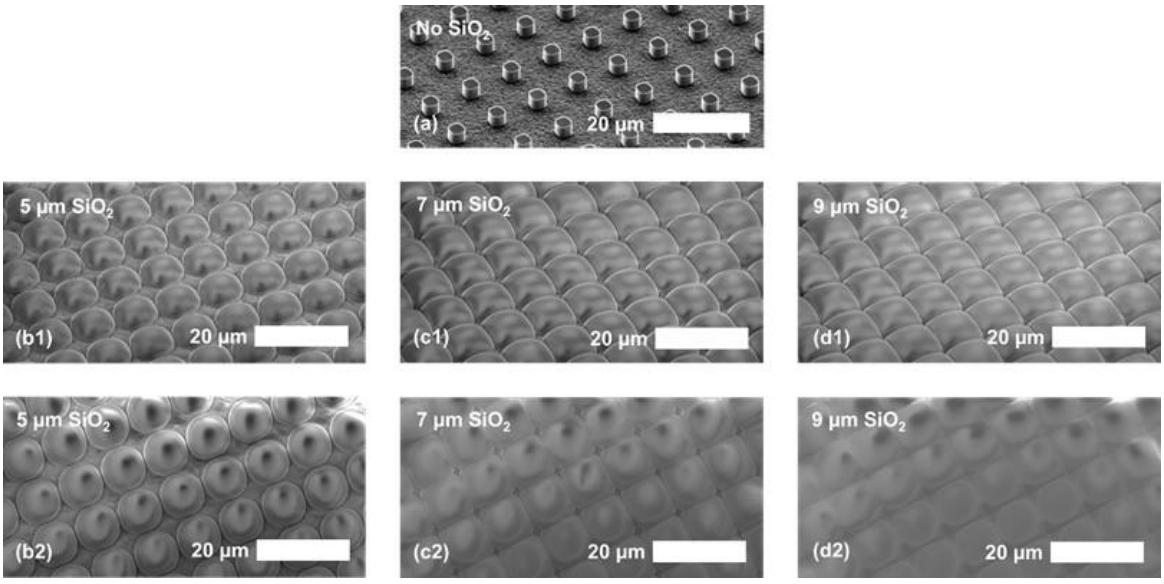

Figure 3.7.1: SEM images showing micropillars (2.5 µm diameter, 2 µm height, 10 µm pitch) following dry etching and KOH treatment (a), and subsequently after 5 µm (b), 7 µm (c), and 9 µm (d) of conformal TEOS deposition. Images a, b1, c1, and d1 were taken at 45° off normal, while b2, c2, and d2 were taken normal to the sample surface [18].

in the dielectric surface, which increases the sheet resistance of the continuous p-contact and can even cause opens to form if the p-contact layer is too thin.

These surface topology issues would normally be addressed using chemical mechanical planarization (CMP), a technique employed extensively in industrial damascene processes, particularly during the fabrication of upper the metallization layers of integrated circuits. Unfortunately, CMP is not available in the SMFL, and does not work well with irregularly shaped pieces like the ones our group uses. In lieu of CMP, an older technique based on plasma etchback of the dielectric can be performed. This method makes use of a sacrificial, self-planarizing photoresist layer and a modified TEOS dry etch which etches TEOS and photoresist at equal rates. By coating the planarizing photoresist over a topologically complex TEOS surface, the magnitude of surface features can be significantly reduced. The subsequent planarizing dry etch then removes the photoresist

and the SiO_2 at equal rates, eroding the SiO_2 surface features as the photoresist is removed. This allows the surface feature height (h) of the SiO_2 surface to be reduced by orders of magnitude after only a few planarization cycles. This process is briefly summarized in Figure 3.7.2. As opposed to chemical mechanical planarization/polishing (CMP), which utilizes a combination of corrosive chemicals and mechanical abrasion to remove surface features [16,17], this technique can be used on samples of any size and shape, and can be performed in almost every research cleanroom with dielectric deposition and dry etching capability.

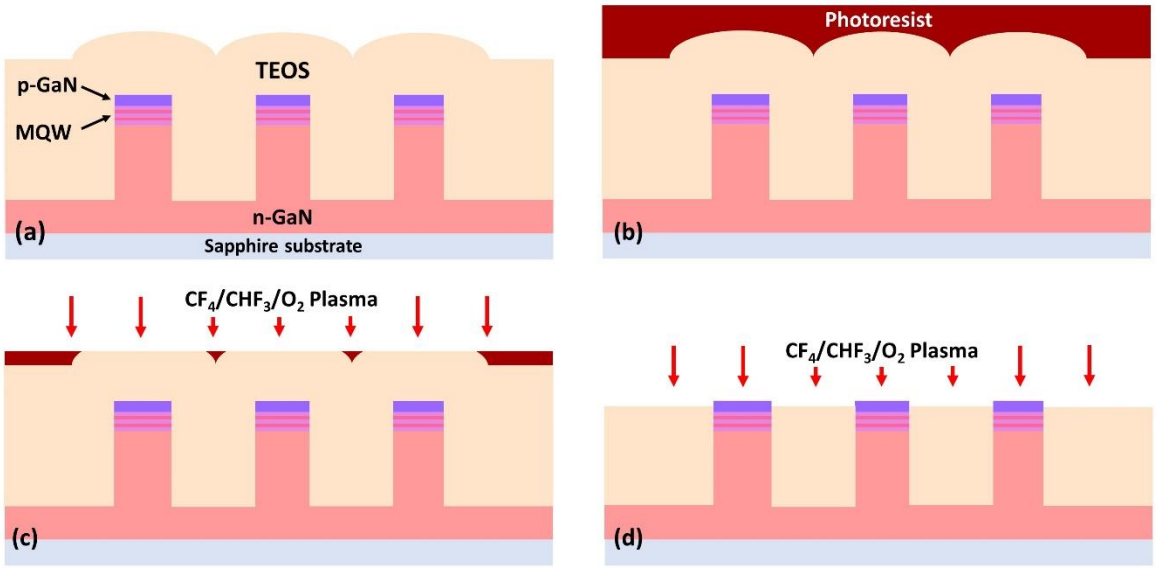

Figure 3.7.2: Cross-sectional diagram of the dielectric planarization process. (a) TEOS deposited conformally over GaN nanowires via PECVD. (b) Coating of a self-planarizing photoresist layer over the TEOS surface. (c) Etch back of the photoresist and TEOS using a CF4/CHF3/O2 plasma which etches both materials at ~70 nm/min. (d) Planarized SiO2 etched back to expose the p-GaN tips of the nanowires [18].

Starting with a sample on which micropillars have been previously fabricated (as shown in Figure 3.7.1(a)), TEOS (or another dielectric such as SiO_2 or Si_3N_4) is deposited in via PECVD to a thickness greater than the height of the micropillars (Figure 3.7.2(a)).

Photoresist is then coated, resulting in a mostly planarized surface. Photoresist is very effective at planarizing over short-range surface topology, such as the features formed arrays of tightly spaced nanowires or micropillars (see Figure 3.7.1), but is less effective at long range planarization between widely spaced structures/devices. Figure 9(b) shows a cross-sectional representation of a perfectly planarized photoresist layer over a “domed” TEOS surface (see Figure 8(b-d)). A fluorine plasma etch is then used to etch back the photoresist and TEOS at equal rates (Figure 9(c)). This etch must be carefully optimized in order to target a 1:1 selectivity between photoresist and TEOS. This etch was performed at in a Trion Minilock RIE at 130 mtorr, 200 W capacitive RF power, and with gas flow rates of 70/60/11 sccms $CHF_3/CF_4/O_2$. This process of coating photoresist and removing it with specialized 1:1 dry etch can be performed as many times as necessary to achieve the desired degree of planarization, but 2-3 cycles have generally been found to be sufficient.

Once a sufficient level of planarization is attained, any TEOS dry etch can then be used to further etch back the TEOS layer until the tips of micropillars are exposed, as shown in Figure 3.7.2(d). At this point, the planarization process has achieved its purpose of enabling the use of a conformally deposited SiO2 layer as an interlayer dielectric, and a p-contact layer can be safely deposited to connect multiple micropillars in parallel. Without initial planarization to remove the surface topology of the as deposited SiO2, deep trenches with sharp discontinuities would exist in the interlayer dielectric, making formation of a continuous p-contact layer difficult and risking potential shorting of the n and p contacts in a worst-case scenario. Figure 3.7.3 shows the effects of 1, 2, and 3 planarization cycles on the TEOS surface over an array of 2.5/2/10 μm (width, diameter, pitch) GaN

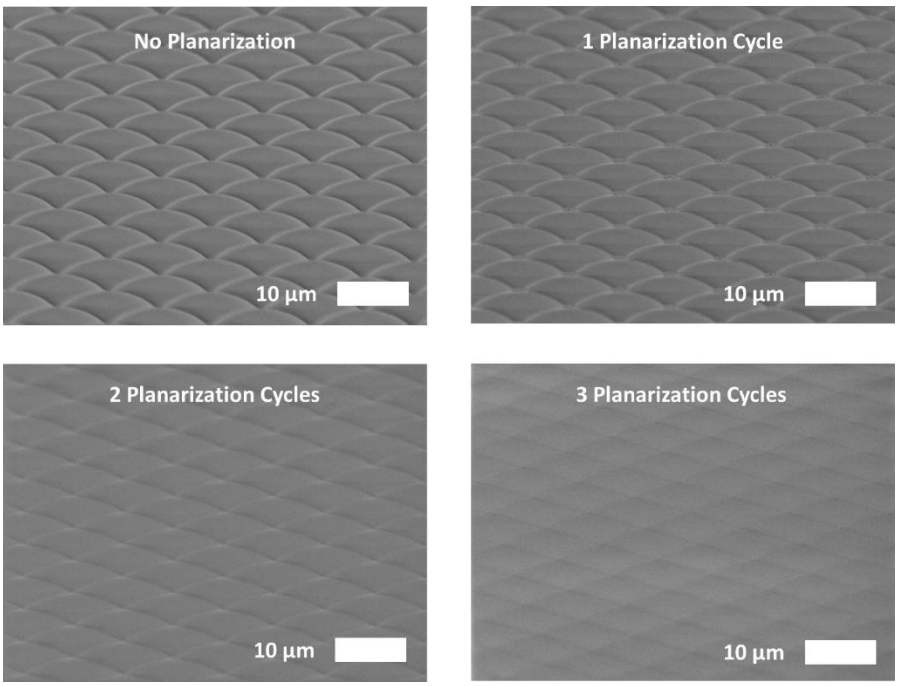

Figure 3.7.3: SEM images of micropillars (2.5 µm diameter, 2 µm height, 10 µm pitch) after 0 planarization cycles, h = 1.62 µm (a), 1 planarization cycle, h = 610 nm (b), 2 planarization cycles, h = 76 nm (c), and 3 planarization cycles, h = 24 nm (d) [18].

micropillars. The initial surface feature height was measured at ~1.6 µm, and was decreased to 610 nm, 74 nm, and 24 nm after 1, 2, and 3 planarization cycles respectively. These results show that this photoresist planarization etchback process is extremely effective at flattening short range surface topology over arrays of nano and microstructures. The development and optimization of this process in the SMFL is critical to the further development of DUV nanowire and micropillar array LEDs. Further information and details on this process are provided in Chapter 4.

3.8 Physical Characterization

Inspection of samples between fabrication process steps is critical in determining whether the previous process steps were completed correctly. Visual inspection with the

naked eye is often sufficient to determine if a step has been successful, but in many cases more advanced inspection techniques, such as optical microscopy or thin film interferometry must be used. Observation of samples is performed between every process step to check for particle contamination. The results of many procedures, such as photoresist development, dry etching, wet etching, and metal liftoff can be easily verified using an optical microscope. Other processes, such as TEOS and other transparent thin film deposition, can only be characterized using thin film interferometry, in which a variable wavelength light source and photodetector are used to determine the thickness of transparent thin film via the phenomenon of thin film interference. Many of the structures fabricated in the SMFL are too small to be seen even with high magnification microscope objectives and require more advanced tools such as scanning electron microscopes (SEMs) and atomic force microscopes (AFM) to be properly inspected.

3.8.1 Scanning Electron Microscopy (SEM)

Scanning electron microscopy uses electrons to image samples at much higher resolutions than are achievable with optical microscopy. The resolution of an optical microscope is limited to no less than half the wavelength of the light used, which, for normal white light is around 250 nm. Electron microscopes avoid this issue by using a beam of electrons to image a sample. Although electrons are massive particles unlike photons, they still have a characteristic wavelength determined by the De Broglie equation. The observed wavelength of an electron depends on its velocity relative to the observer, but is generally between 10 and 40 pm for the electrons in an SEM, more than 5000 times shorter than the wavelength light used in optical microscopy. This gives scanning electron microscopes a theoretical resolution of less than 1 nanometer, although this is nearly impossible to achieve

with all but the most advanced SEM tools. An SEM works by accelerating a beam of electrons in a vacuum using an electric field of between 1 and 30 kV to more than 20% the speed of light. The electron beam is focused onto a sample using a series of electromagnets which can be manipulated to change the spot size from several microns down to several nanometers. The electrons impact and penetrate the sample surface, imparting their kinetic energy to electrons in the sample, ejecting them from the sample surface where they are collected by an electric field and counted by a detector. Differences in sample surface geometry and composition change the flux of "secondary electrons" which are ejected from the sample, creating differences in the signal intensity measured by the secondary electron detector. In this way, each "point" on the sample surface is seen as a monochromatic pixel

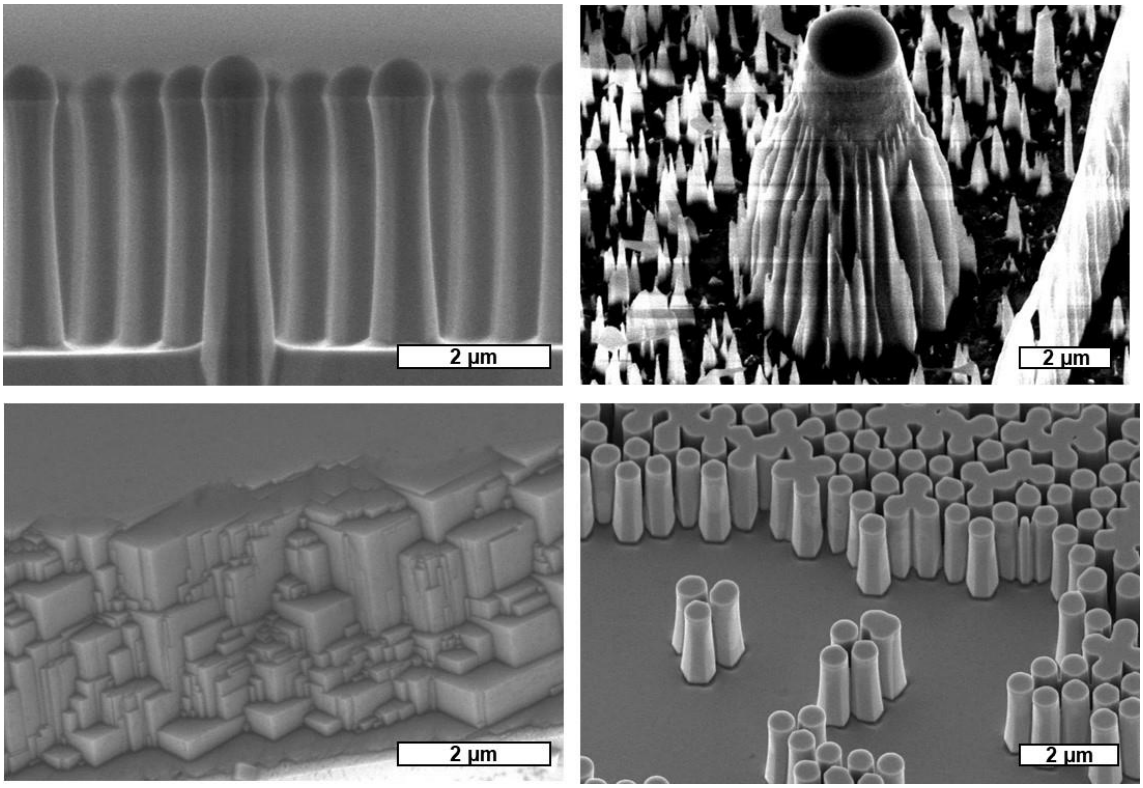

Figure 3.8.1: Off-normal SEM images of various GaN structures.

of different brightness by the detector. By scanning the electron beam over the sample thousands of times per second, millions of pixels can be captured and assembled into an image. SEMs can allow for imaging of features as small as several nanometers, or very high-resolution images of larger features which would be barely resolvable in an optical microscope. SEMs are invaluable tools in the fabrication of nanowire LEDs and other devices with dimension smaller than 50 μm. SEMs also allow for off-normal images of samples as shown in Figure 3.8.1, which are critical for observing features which cannot be seen by imaging normal to the surface of the sample. Nanowire in particular benefit immensely from SEM imaging, as SEMs are more or less the only tool capable of measuring the heights of nanowires more than a few microns tall.

3.8.2 Atomic Force Microscopy (AFM)

When extremely precise step height measurements are required, atomic force microscopy (AFM) is used. AFM operates by tapping an extremely small probe, usually made of silicon, against a sample surface with high frequency. A constant force is maintained between the probe and the sample surface using a piezoelectric probe arm, and probe deflection is measured using a laser which measures the distance to a mirror mounted on the probe arm. Probe deflection is used to create a topographic map of the sample surface with sub-nanometer accuracy. AFM can be used to measure step heights of up to several microns with much greater accuracy and reliability than SEM, and can also be used to measure surface roughness. Additionally, AFM can be used to measure step heights in organic or insulating samples, which experience severe charging in an SEM. For example, when performing etch back of PDMS or TEOS, AFM is used to determine when the nanowire tips are exposed, as SEM causing charging off the PDMS layer which makes it

near impossible to see the nanowires. Figure 3.8.2(a) shows the surface of a nanowire LED sample prior to exposure of the nanowire tips, while Figure 3.8.2(b) shows the same sample after the PDMS has been etched back an additional 100 nm to expose the nanowires.

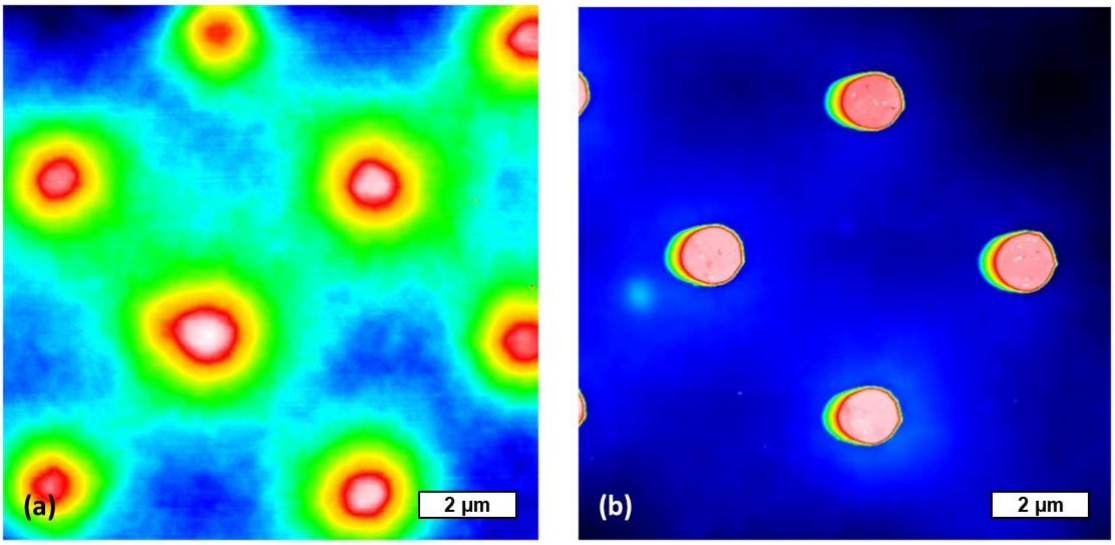

Figure 3.8.2: AFM maps of a nanowire sample before (a) and after (b) the nanowires tips are exposed by etching back the PDMS.

3.9 Electrical and Optical Characterization

Following complete fabrication of an LED device, electrical and optical testing is performed to characterize the current voltage characteristics, turn-on voltage, emission wavelength and linewidth, and emission power. Samples are tested on a manual probe station mounted on an air table to mitigate vibrations. A vacuum stage with 3-axis control is used to secure the sample and position it beneath a microscope (also with 3-axis control). Tungsten electrical probes are then brought into contact with the n- and p-contacts of the LED devices, and current is supplied to the device using a Keysight B1500 Parameter Analyzer. The B1500 can supply up to 100 mA of current at up to 100 V with femto-amp

resolution. An Ocean Optics Flame S UV-Vis spectrometer is used to measure the emission properties of the LEDs. An optical fiber connected to the spectrometer is positioned in close proximity to the probed devices, generally with 2 mm, using a pair of flexible clamp tipped arms. The microscope is focused onto the probed devices, and the reflected light from the microscope spot is used to optimize the optical fiber position to achieve the highest possible intensity. All lights are then turned off in the room and the electroluminescence (EL) properties of the LED are recorded by performing a voltage sweep which illuminates the LED. Power measurements are performed by placing the Newport power meter with nanowatt sensitivity directly above the probed devices, generally within 2 cm of the LED. The emission power normal to the LED surface is then captured. While this is not an ideal method of measuring emission power and cannot be used to determine EQE since the entirely of the emitting light is not captured, it is the best that can be done for a device probed at the wafer-level, as unpackaged LEDs cannot be easily characterized using an integrating sphere.

Photoluminescence (PL) measurements are also performed on samples prior to completion of the fabrication process, in order to benchmark metrics such as emission wavelength, linewidth, and intensity prior to fabrication of nanostructures. A Horiba HeCd 325 nm laser with a maximum output power of 30 mW is used to produce photoluminescence in samples with emission wavelengths greater than ~350 nm. This system is unfortunately limited to use for near-UV and visible light LEDs, as its 325 nm emission wavelength is not capable of producing PL in DUV LED samples. The light emitted from the optically excited samples is then measured by a built-in photodetector, allowing for determination of emission wavelength, emission linewidth, defect emission,

and many other material related properties of the sample. In addition to this laser PL system, we also sometimes use a small, handheld mercury lamp to perform qualitative PL on DUV samples. The mercury lamp has emission lines down to ~250 nm, allowing it to induce weak photoluminescence from DUV LEDs which can be measured using the Ocean Optics spectrometer. This allows for very basic characterization of DUV samples prior to completion of device fabrication, which is often very useful in determining any sort of emission wavelength shift that occurs following fabrication of nanostructures on the sample.

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CHAPTER 4: Deep-Ultraviolet Nanowire Array Light Emitting Diodes

4.1 Electrically Driven Nanowire Array LEDs Emitting at 286 nm

4.1.1 Introduction

III-nitride DUV LEDs are of significant interest for use in a wide range of applications, including water purification, sterilization of surfaces and medical tools, UV curing, 3D printing, sensing, and many others [1–6]. The majority of these applications currently rely on mercury arc lamps for generation of DUV light, which are bulky, short-lived, and produce hazardous mercury waste when disposed of [1,3,6]. In comparison, DUV LEDs offer compact form factors, long lifespans, narrow emission linewidth, tunable emission wavelength, high switching speeds, and much better environmental compatibility [1,3–5]. Despite these numerous advantages, DUV LEDs have not yet seen widespread adoption in most of their potential applications due to their poor efficiencies relative to blue, green, and red LEDs. In comparison to GaN/InGaN blue LEDs, which often have external quantum efficiencies (EQE) greater than 80% [7], AlGaN-based DUV LEDs emitting below 280 nm usually have EQEs in the single digits [1,2], with the current record being 20% at 275 nm [8]. Despite recent advances such as improved p-type doing [1,2], reduced dislocation density [1,2,9], and improved quantum well (QW) design [1,2], which have allowed for attainment of internal quantum efficiencies (IQE) in excess of 60% [1,10], light extraction efficiency (η_{EXT}) remains much lower (< 20%) for DUV LEDs than for blue LEDs (> 90%) [1,11]. The poor extraction efficiencies of DUV LEDs are due to several factors including absorption of emitted light by the p-GaN layer [12–14], loss of light into the substrate [14], and the prevalence of

transverse-magnetic (TM) polarized light which is much more difficult to extract from conventional LED structures and becomes more dominant at shorter wavelengths [12,14,15].

Many different approaches have been investigated as means for improving the η_{EXT} of DUV LEDs, including transparent p-AlGaN layers [8,16], highly reflective contact metallization [8,17], surface roughening and nanostructuring [18–22], photonic crystal out-coupling [8,16], and nanowire formation [2,12,14,15,23,23–36], as discussed in Chapter 2. While all of these studies have successfully improved η_{EXT} in some way, only nanowire formation has been found more than marginally effective at enhancing the extraction of TM-polarized light. TM-polarized light, which propagates primarily in the plane of the epitaxial stack (epistack) due to having a very narrow c-axis escape cone, has very low η_{EXT} in mesa-like LED structures which have lateral dimensions in the tens or hundreds of microns [12,14,37–39]. In nanowires, which have lateral dimensions on the order of hundreds of nanometers to several microns, TM-polarized light can easily escape into free space, drastically increasing the extraction efficiency of TM-polarized light [12,14,40]. It is for this reason that nanowires are of great interest as a means to enhance the EQE of DUV LEDs, especially those emitting at the lower end of the DUV range (< 240 nm) where band-mixing effects lead to TM-dominant emission [2,12,14,15]. In addition to enhancing η_{EXT}, nanowires have also been shown to reduce dislocation density in the active region [2], improve dopant concentration due to enhanced surface doping [27,41,42], and allow for growth on, or transfer to, different substrates, even including flexible substrates [23,43–45]. To date, the vast majority of studies involving AlGaN-based DUV nanowire LEDs have focused on epitaxial nanowires grown using metal organic

chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE) in a "bottom-up" fabrication process [23–36]. In comparison, no functional, electrically driven DUV nanowire LED has yet been fabricated using a "top-down" approach, where dry-etching is used to form nanowires from a bulk epistack. This approach is also of great interest, as it has several advantages over bottom-up processes, including improved nanowire uniformity, improved control of nanowire morphology, simplified fabrication of electrical contacts, and improved manufacturing scalability.

Here we demonstrate the fabrication and characterization of top-down fabricated electrically driven nanowire array LEDs emitting at 286 nm with a narrow, 9 nm linewidth. In addition to being the first demonstration of DUV emitting nanowire array LEDs using a top-down approach, we also describe what is, to the best of our knowledge, the first discovery of a unique "inverse taper" phenomenon which develops in high Al-content AlGaN nano/microstructures during hydroxyl based wet etching.

Nanowire arrays were fabricated using a Cl_2/Ar dry etch followed by a heated hydroxyl-based wet etch, resulting in a novel "inverse taper" profile in which the nanowire base diameter is smaller than the top diameter. Polydimethylsiloxane (PDMS) was used as an interlayer dielectric, electrically isolating the n- and p-metal contacts at the bases and tops of the nanowires respectively. Electrical testing returned an average turn-on voltage (V_{th}) of ~7 V, in line with that of other nanowire DUV LEDs [23–29,31,32,36], while power measurements showed emission power to be linearly dependent on current density, also in keeping with the results of prior works [24–32,34,35]. The onset of efficiency droop was found to occur at around 16 A/cm^2, representing a moderate improvement compared to other reported results in which peak EQE usually occurs at less than 5 A/cm^2 [23–26,31].

Preliminary finite-difference time-domain (FDTD) simulations also revealed that the unique inverse-taper profile of these nanowires could produce significant enhancements in the η_{EXT}, especially for TM-polarized light, with increased taper angle correlated directly to increased η_{EXT}. These results are very promising, and show that top-down fabricated nanowires may have significant advantages over epitaxially grown nanowires with respect to light extraction.

4.1.2 Nanowire Array LED Fabrication

Nanowire array LEDs were fabricated on a 50 mm AlGaN on c-plane sapphire wafer purchased from a commercial vendor. The epistack consisted of a 1.35 µm AlN buffer layer followed by a 20x $Al_{0.85}Ga_{0.15}N$/AlN superlattice, 260 nm of u-$Al_{0.7}$-$Ga_{0.3}$-N, µm of n-$Al_{0.5}Ga_{0.5}N$, a 5x $Al_{0.5}Ga_{0.5}N/Al_{0.4}Ga_{0.6}N$ multiple quantum well (MQW), a 25 nm n-AlGaN EBL, 50 nm of p-AlGaN, and 200 nm of p-GaN. A simplified, not to scale version of this epistack can be seen in Figure 4.1.1(a). Following standard RCA cleaning of the wafer, 100 nm of SiO_2 was deposited using plasma enhanced chemical vapor deposition (PECVD). 200 nm thick Ni was then deposited using electron beam

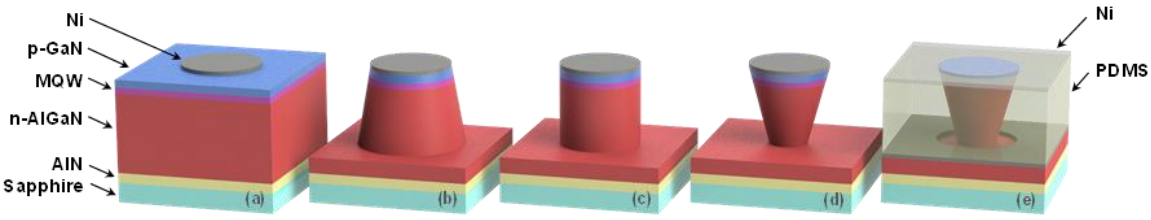

Figure 4.1.1: Fabrication process schematic, ab**b**reviated, not to scale. (a) Bulk epistack following patterning of the Ni dry etch hardmask (SiO_2 layer omitted). (b) Single nanowire following dry etching of the SiO_2 and AlGaN/GaN epistack (micromasking omitted). (c) Single nanowire following immersion in 40% AZ400K (aqueous) at 80°C for ~5 min. (d) Single nanowire following immersion in 40% AZ400K (aqueous) at 80°C for ~60 min. (e) Single nanowire following deposition of the n-metal contact, removal of the metal cap, coating and etch-back of the PDMS, and deposition and patterning of the Ni p-contact.

evaporation and patterned via a photoresist liftoff process, as can be seen in Figure 4.1.1(a). A CF_4/CHF_3 reactive ion dry etch (RIE) was then used to etch the SiO_2 layer using the patterned Ni as a hardmask and the underlying p-GaN as an etch stop. A Cl_2/Ar inductively coupled plasma (ICP) dry etch was then used to etch the GaN/AlGaN epistack to a depth of ~2.5 µm, utilizing Cl_2/Ar gas flow rates of 40/10 sccms, a chamber pressure of 30 mtorr, and ICP and CCP RF powers of 500 W and 225 W respectively. This ICP dry etch formed structures with "normal taper" as shown in Figure 4.1.1(b), where the base of the structure is wider than the lithographically defined top diameter. Micromasking was found to be extensive following this second dry etch, as can be seen in Figure 4.1.2(a), and is likely due to a combination of factors including physical defects in the epistack, sputtering of exposed SiO_2 [46], and lower volatility of certain etch byproducts [47].

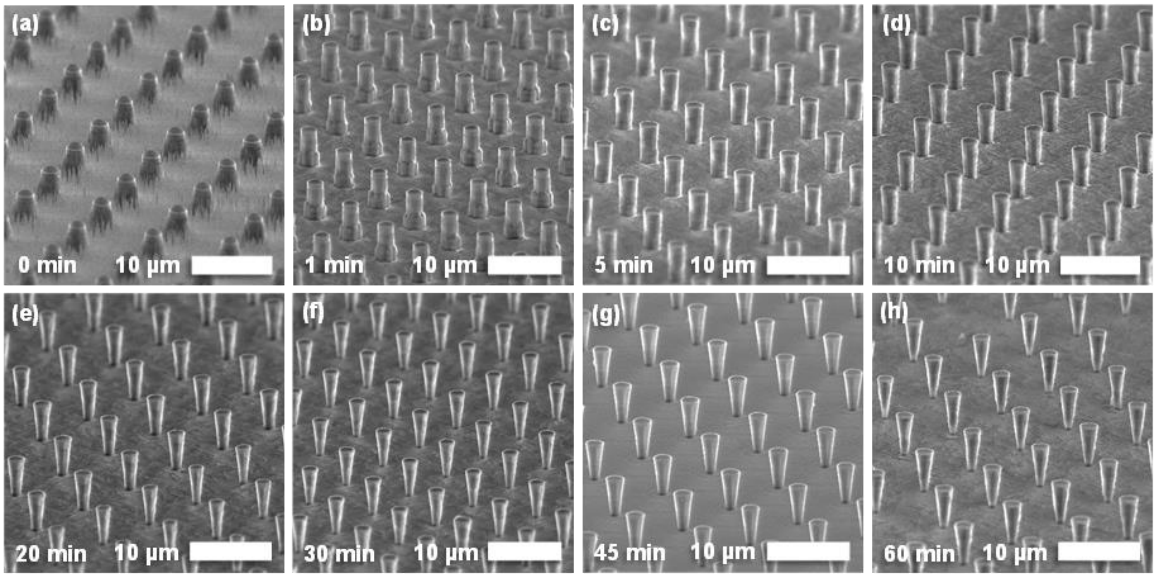

Figure 4.1.2: SEM images showing AlGaN nanowires at various points in the fabrication process. Nanowires after dry etch (a), and 1 min (b), 5 min (c), 10 min (d), 20 min (e), 30 min (f), 45 min (g), and 60 min (h) in 0.8 wt.% aqueous KOH at 80°C.

Following the dry etch, a multipurpose, hydroxyl-based wet etch was performed in order to remove the micromasked structures, alter the sidewall profile of the nanowires, and passivate the sidewall surfaces. The wafer was immersed in 40% AZ400K (aqueous), a positive photoresist developer containing 2% KOH by weight, at 80°C for a total of 60 minutes. SEM images were taken of the nanowires after 0, 1, 5, 10, 20, 30, 45, and 60 minutes in the etch solution (Figure 4.1.2). As has been demonstrated extensively in other literature [45,48–55], this hydroxyl-based wet etch effectively removed all micromasked structures and straightened the sidewalls of the nanowires. This can be more clearly seen in Figure 4.1.3. Micromasking, which is extremely dense following dry etch (Figure 4.1.3(a)), is entirely removed after only 5 min in the aforementioned KOH solution (Figure 4.1.3(c).

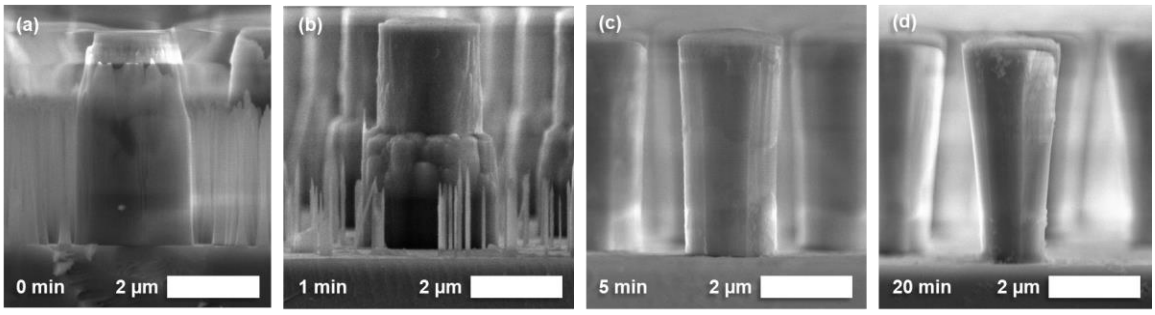

Figure 4.1.3: SEM images showing AlGaN nanowires at various points in the fabrication process. Nanowires after dry etch (a), and 1 min (b), 5 min (c), and 20 min (d) in 0.8 wt.% aqueous KOH at 80°C.

Extended wet etches in this solution have been found to produce an “inverse taper” profile in AlGaN nanowires with high Al-content, in which the bases of the nanowires will eventually narrow to a point if left in the etch solution indefinitely. This phenomenon is shown in Figure 4.1.2(d-h) and Figure 4.1.3(d). SEM measurements of the nanowire

sidewall taper angle α, defined as the angle between the nanowire sidewall and the nanowire axis, reveal that vertical sidewalls (α = 0°) are obtained after ~5 min in the etch solution, with α increasing to 5° after 20 min and 10° after 60 min, as shown in Figure 4.1.4. This phenomenon is not observed in GaN or low Al-content AlGaN, where extended hydroxyl-based etches effectively self-terminate once vertical sidewalls are achieved while the top of the structure remains protected. We attribute this phenomenon, apparently unique to high-Al content AlGaN, to alteration of the surface energy/polarity of the semi-polar $(20\bar{2}1)$ and $(10\bar{1}1)$ wurtzite planes by inclusion of the alloying Al atoms, although the exact cause remains unknown and requires further investigation [45]. The roughly linear relation between α and etch time shown in Figure 4.1.4 indicates that α would continue to increase beyond 10° with etch times in excess of 1 hour. Unfortunately, the diameters of the nanowires studied (~2 μm) prevented us from confirming this, as etch times longer than 1 hour cause the nanowires to detach from the substrate.

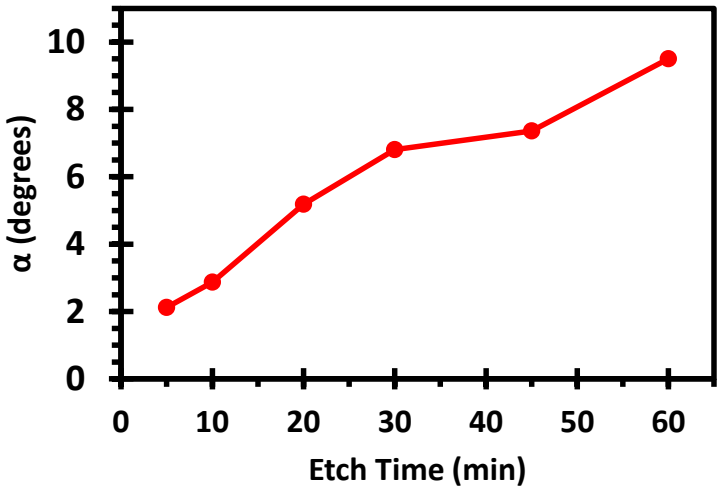

Figure 4.1.4: Nanowire taper angle as a function of etch time. Taper angles beyond 10° could not be measured due to the size of the nanowires.

After completion of the wet etch, a self-masked, universal n-metal contact was deposited using highly directional thermal evaporation. The n-metal stack consisted of 10 nm Ti in contact with the n-AlGaN, followed by 200 nm Al, 30 nm Ni, and 100 nm Ag in order to achieve an ideal ohmic contact to the n-AlGaN [56–58]. The inverse taper profile of the nanowires allowed the n-metal to be deposited without the use of any lithographic patterning, with the wider tops of the nanowires shadowing their bases and preventing deposition of metal on the nanowire sidewalls (Figure 4.1.1(e)). This process allows for simplification of the fabrication process as well as reduced series resistance of each nanowire array, as current is allowed to reach the bases of nanowires in the middle of each array without traveling through the more resistive n-AlGaN. Following n-metal deposition, the wafer was immersed in 10:1 buffered oxide etch (BOE) in order to remove the 500+ nm thick metal caps on top of each nanowire, which consisted of the 200 nm Ni dry etch mask as well as the self-masked n-metal stack (~340 nm). 10:1 BOE rapidly etches the 100 nm thick SiO_2 layer beneath the Ni hardmask layer, separating the thick metal caps from the tops of the nanowires and allowing them to be removed in the etch solution. Removal of the metal caps is critical as it allows light to escape from the tops of the nanowires which would otherwise be completely reflected by a 500 nm thick metal layer.

Following deposition of the n-metal and removal the metal caps in 10:1 BOE, polydimethylsiloxane (PDMS), a silicone polymer, was spin-coated to a thickness of ~7.7 μm and cured at 90°C for 30 minutes. PDMS was chosen as the interlayer dielectric due to its transparency in the DUV range as well as its thermal stability and chemical inertness. After curing, the PDMS was etched-back using a CF_4/O_2 RIE dry etch in order to expose the p-GaN tips of the nanowires. Ni was then deposited using conformal electron

beam evaporation to a thickness of 20 nm over the entirely of the wafer, and patterned using a photoresist-masked etch in heated phosphoric acid to form the p-contact. Due to the use of a continuous, universal n-contact, individual nanowire array devices were defined by connecting multiple nanowires through patterning of the p-contact Ni layer. Figure 4.1.1(e) shows a nanowire following this final step, with a thin Ni atop the PDMS interlayer dielectric making contact to the top of the nanowire.

4.1.3 Device Characterization

Electrical testing of the completed nanowire array LEDs was performed using a manual probe station and a Keysight B1500A parameter analyzer. The light emission properties of the LEDs were characterized using an Ocean Optics Flame-S spectrometer and a Newport 843-R power meter. Electrical contact was made to the nanowire array LEDs by probing the n- and p-contacts and applying forward bias across them. Contact was made to the n-contact metal by penetrating the flexible PDMS layer with the first probe tip to avoid the need to dry etch contact cuts in the PDMS. Contact was made to the thin p-contact metal on top of the PDMS by carefully lowering the second probe tip onto the metal surface, applying only enough pressure to make electrical contact but not enough to deform or puncture the underlying PDMS. Electroluminescence (EL) measurements were taken by positioning an optical fiber connected to the Ocean Optics spectrometer within a few millimeters of the probed devices and applying either voltage sweeps or constant voltage across the probes.

Figure 4.1.5 plots the EL spectra of a 30x30 (~300 x 2300 μm^2) array nanowires for current densities up to 2.8 A/cm^2. Each nanowire is ~ 5 μm tall with a top diameter of 2.2 μm and a taper angle of $\alpha \sim 10°$, with all nanowires positioned in a square array with a

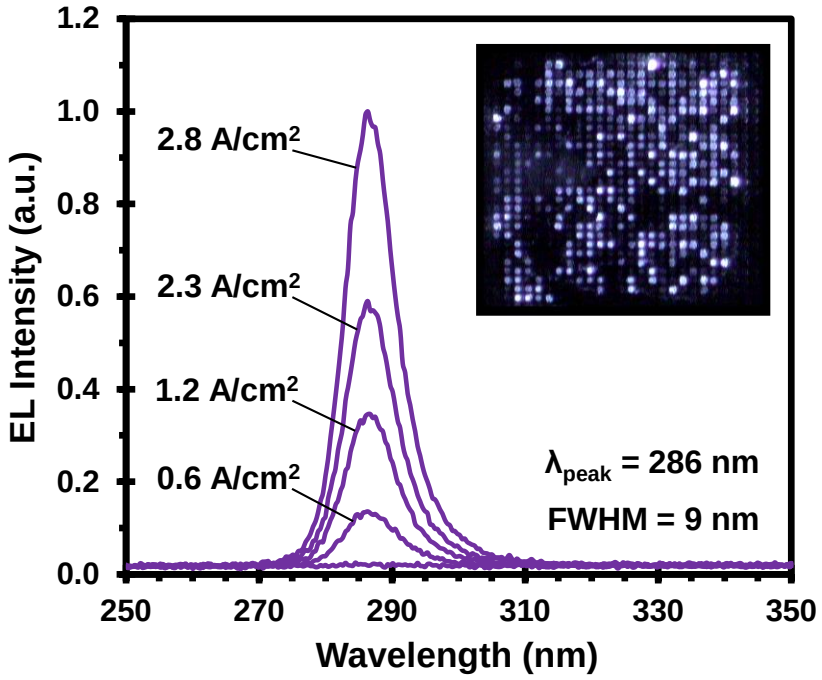

Figure 4.1.5: EL spectra of a 30x30 nanowire array LED at various current densities. λ_{peak} is located at 286 nm and all spectra have a linewidth of 9 nm. The inset shows an optical image of the illuminated nanowire array.

pitch of 10 μm for a fill factor of ~ 15.2%. The emission peak (λ_{peak}) is centered at 286 nm, a redshift of ~16 nm from the EL λ_{peak} of the bulk epistack at 270 nm. This redshift is expected due to reduction of the quantum confined Stark effect (QCSE) following formation of nanowires, which reduces epitaxial strain in the MQW [59–63]. The EL spectra all exhibit a narrow linewidth of 9 nm, independent of current density. The inset of Figure 4.1.5 shows the illuminated array at a current density of 2.8 A/cm^2, captured with a CCD camera. It is obvious from this image that not all nanowires are emitting light, and that those that are emit at different intensities. This is also shown in Figure 4.1.6, in which a different array of nanowires is illuminated by voltages between 6 and 12 V. We attribute this to several factors. First, the etch-back of the PDMS film was found to expose the tips

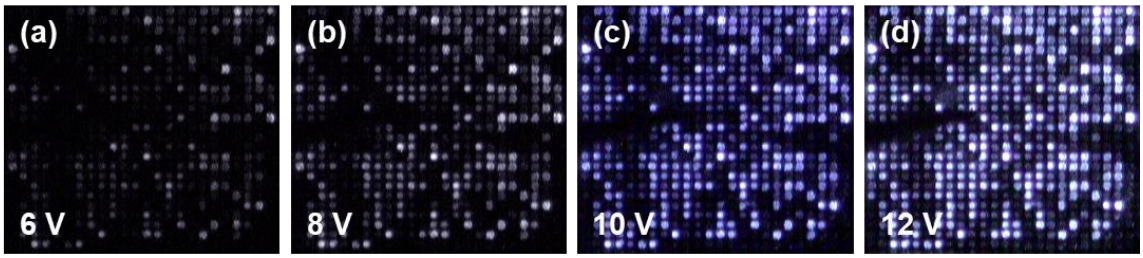

Figure 4.1.6: EL spectra of a 30x30 nanowire array LED at 6, 8, 10, and 12 V, showing the inconsistent manner in which individual nanowires illuminate.

of nanowires in sparser arrays first, due to the PDMS coating thicker over more dense arrays of nanostructures. This prevented the illumination of some of the much denser arrays, while the peripheral nanowires in some sparser arrays, such as the one shown in the inset of Figure 4.1.6, failed to illuminate due to the thinner PDMS at the array edges causing shorting of the active region by the p-contact metal. Second, the photoresist mask (SU-8 mr-DWL-5) exhibited poor adherence to the Ni coated PDMS surface during the wet etch of the 20 nm Ni p-contacts, allowing the phosphoric acid etch chemistry to penetrate beneath the photoresist etch mask in some areas, damaging or destroying the Ni layer and preventing illumination of nanowires in these regions. Third, non-uniformities in nanowire diameter due to lithography resolution limitations and statistical variation in the quality of the Ni p-contact to the top of each nanowire lead to variations in the brightness of each nanowire. These issues could be addressed through use of planarized SiO_2 as in interlayer dielectric in place of PDMS, as will be discussed in section 4.5.2.

The I-V characteristics of the 30x30 nanowire array LED are shown in Figure 4.1.7(a). Threshold voltage is ~ 7V, which is comparable to results obtained for other planar and nanowire DUV LEDs [1,2,23–29,31,32,36]. Efficiency measurements were performed by placing the power meter directly above the probed devices and measuring power output

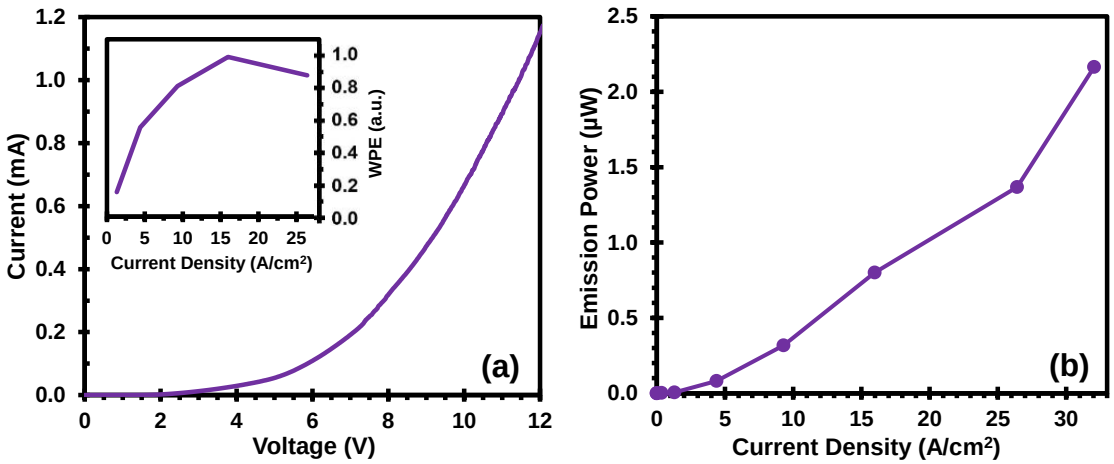

Figure 4.1.7: (a) Linear I-V characteristics of a 30x30 nanowire array LED, showing a V_{th} of approximately 7 V. The inset shows the normalized WPE of the LED, with peak WPE occurring at 16 A/cm^2 and minimal efficiency droop at higher current densities. (b) Emission power as a function of current density.

as a function of current density. Output power density was found to be linearly related to current density, increasing from 50 μW/cm^2 at 0.35 A/cm^2 to 35 mW/cm^2 at 32 A/cm^2 as shown in Figure 4.1.7(b). This is consistent with the results of other works, which often report similar or lower emission power densities for larger arrays of tightly packed, disordered epitaxial nanowires [24–32,34,35]. It is important to note that the power meter could be placed no closer than 3 cm from the wafer surface due to constraints of the test setup. As emission power was not measured using an integrating sphere, our results are not representative of the true emission power of the tested devices. The 1 cm diameter detector, positioned 3 cm from the emitting devices, covered ~1.4% of the emission hemisphere above each tested device, and can thus be expected to have captured ≥ 1.4% of the total emissive power. As it is impossible to accurately measure output power without an integrating sphere due to the complex far field radiation patterns of nanowire LEDs, our results only intended to be qualitative in nature. The EQE of our unpackaged devices is

estimated to be between 0.0067% and 0.48%, although exact and accurate determination of the EQE requires packaging of the LED and use of an integrating sphere. Reported results for epitaxial nanowire array DUV LEDs generally range between 0.005% [36] and several percent [25,35], while the EQEs of planar DUV LEDs are generally between 1% and 5% [4,21,22].

The inset of Figure 4.1.7(a) shows the wall plug efficiency (WPE) as a function of current density, with peak WPE occurring at ~16 A/cm^2. These results are in agreement with existing literature, which shows, in general, that the onset of efficiency droop occurs at higher current densities and is generally less severe for nanowire DUV LEDs than for planar DUV LEDs [2,23,64–67]. A droop onset of 16 A/cm^2 is also moderately higher than has been reported for other DUV nanowire LEDs (< 5 A/cm^2) [23–26,31]. We propose that the later onset of droop in DUV nanowire LEDs, especially in our devices, may be due in part to the lower volume of electrons available in a single tapered nanowire, which reduces the ratio of electrons to holes entering the active region. While the density of free electrons in the n-AlGaN remains unchanged, the reduced n-AlGaN volume of each nanowire, especially in nanowires with inverse taper, reduces the number of electrons which enter the active region during forward biasing of the nanowire array. This serves to reduce carrier overflow and non-radiative recombination of carriers in the p-AlGaN and p-GaN regions, pushing the onset of efficiency droop to higher carrier densities. While this theory requires further verification, it could, if true, allow for engineering of the n-AlGaN volume of nanowires in order to reduce the carrier overflow which occurs in all GaN/AlGaN-based LEDs due to poor hole mobility and concentration in Mg-doped GaN/AlGaN [66,67].

4.1.4 Conclusions

This initial demonstration of electrically driven top-down fabricated DUV nanowire array LEDs is the first of its kind. While electrically driven, epitaxially grown nanowire array LEDs emitting in the DUV regime can be found in literature, our results are the first report of successful fabrication of DUV nanowire arrays LEDs via a top-down approach (as of their 2021 publication). A narrow linewidth of 9 nm, coupled with late-onset efficiency droop at 16 A/cm^2 make these preliminary devices and fabrication process suitable for potential high-power applications in which high current densities are required. In contrast to extensive existing work on epitaxially grown DUV-emitting nanowires, the top-down fabrication approach outlined here offers numerous benefits including improved nanowire uniformity, greater control over nanowire morphology and array geometry, simplified formation of electrical contacts, and improved manufacturing scalability. The inverse taper profile of the nanowires used in our devices were also shown through simulation to produce significant enhancements in η_{EXT} compared to nanowires with vertical sidewalls. These simulation results are discussed in section 4.3.

Despite the promising results of this preliminary work there are still many issues which must be addressed in order to bring the efficiency of these devices more in line with planar DUV LEDs. These prototype devices had very poor yield, due primarily to difficulties with the PDMS interlayer dielectric and associated etch back process. Section 4.4 describes a solution to this issue based on planarization of conformally deposited PECVD SiO_2. Use of a rigid dielectric like SiO_2 allows for the possibility of wire bonding and packaging of DUV LEDs, something which cannot be done when using PDMS. DUV nanowire/micropillar array LEDs described later in this chapter utilize an AlGaN/delta-

GaN epistructure developed by Dr. Cheng Liu and previous members of our research group [68]. The results presented in this section were published in *AIP Advances* in 2021 [79].

4.2 Flexible DUV Nanowire Array LEDs Emitting at 292 nm

4.2.1 Introduction

AlGaN DUV LEDs are usually fabricated as planar mesa devices due to the maturity of the fabrication process. Nanowire DUV LEDs, while more difficult to fabricate, offer higher η_{EXT} and improved IQE, which together produce significant enhancements in EQE [12]. Nanowire LEDs can be formed through a bottom-up growth approach, which allows for large reductions in defect density through use of specialized growth substrates, further enhancing their IQEs when compared to planar LEDs [2]. Though nanowire LEDs have a number of beneficial properties, a reliable process to remove them from the growth substrate has not yet been developed, as it has for planar LEDs [69]. LEDs removed from the growth substrate offer new possibilities for flexible electronics and photonics, and enable reuse of the epitaxial substrate. Previous work on flexible nanowire LEDs typically involves embedding the nanowires in a flexible polymer for support, followed by mechanical exfoliation with a razor blade [70]. As a requirement for this process, the nanowires must be grown to at least 20 μm tall, and even then, the approach still suffers yield issues [71]. Therefore, a more reliable and stable process is needed to realize flexible DUV LEDs.

Our group's earlier work demonstrated that hydroxyl-based chemistries can wet etch GaN and remove dry etch induced damage, as the OH^- ions in these solutions exhibit a unique crystallographic etching in wurtzite GaN and AlInGaN allows [53]. Hydroxyl based chemistries also allow for formation of vertical GaN nanostructures with perfectly smooth sidewalls [53]. These chemistries do not etch Ga-polar surfaces, such as the c-plane (0001) of wurtzite GaN and AlInGaN alloys, instead rapidly etching the semi-polar $(10\bar{1}1)$

plane until the non-polar ($10\bar{1}0$) plane is revealed, which is then etched more slowly [72]. This phenomenon can be applied to transform a flared cone into a straight-walled nanowire/micropillar without reducing its height or top diameter. The prior section (4.1) describes our discovery of novel phenomenon in which this well studied etch process produces an "inverse" taper profile when used to etch high Al-content AlGaN. Here we extend the work presented in section 4.1 to more thoroughly study hydroxyl-based etching of high Al-content AlGaN with a focus on removing AlGaN nanowires from their substrate for potential use in flexible electronics. Etch rates and sidewall angle dependence on etch time are investigated in order to better understand the physical mechanisms responsible for formation of an inverse taper profile in high Al-content AlGaN nanowires. We demonstrate that this inverse taper phenomenon can be leveraged to enable liftoff of relatively low aspect ratio AlGaN nanowires from the substrate with much greater yield than existing methods.

4.2.2 Nanowire Formation

An AlGaN epitaxial stack grown using metal organic chemical vapor deposition (MOCVD) on a sapphire substrate with a Ga-polar c-plane orientation was used as the basis for the nanowires formed in this study. The epitaxy used here was identical to that used in section 4.1. The epistack consisted of a 1.35 µm AlN buffer layer followed by a 20x $Al_{0.85}Ga_{0.15}N$/AlN superlattice, 260 nm of u-$Al_{0.7}Ga_{0.3}N$, 5 µm of n-$Al_{0.5}Ga_{0.5}N$, a 5x $Al_{0.5}Ga_{0.5}N/Al_{0.4}Ga_{0.6}N$ multiple quantum well (MQW), a 25 nm n-AlGaN EBL, 50 nm of p-AlGaN, and 200 nm of p-GaN. A simplified cross-section of this epistack is shown in Figure 4.2.1(a). The sample was first subjected to a solvent clean consisting of a 5-minute immersion in acetone followed by a 5-minute immersion in isopropyl alcohol, and a

5-minute rinse in DI water. The sample was then coated with lift-off resist (LOR) and photoresist and patterned with 1 - 2 µm openings using laser direct write lithography. Ni was deposited with a thickness of ~200 nm and lifted-off, forming the Ni dots of the dry etch hard mask (Figure 4.2.1(b)). Following the hard mask patterning, nanowires with heights of ~2.5 µm were formed using a Cl_2/Ar inductively coupled plasma (ICP) dry etch. This dry etch utilized Cl_2/Ar gas flow rates of 40/10 sccms, a chamber pressure of 30 mtorr, and ICP and CCP RF powers of 500 W and 225 W respectively. The initial nanowire etch profile produced by the ICP dry etch was cone-like, with the base of the nanowire having a larger diameter than the top (Figure 4.2.1(c)). The sample was then etched in 40% AZ400K (0.8 wt% KOH) heated to 80°C for a total of 70 min. In contrast to work with visible nanowire LEDs [53], the AlGaN nanowires developed a distinct "inverse taper" rather than maintaining a vertical sidewall profile independent of etch time (Figure 4.2.1(d-e)). This inverse taper phenomenon was observed for different samples with high

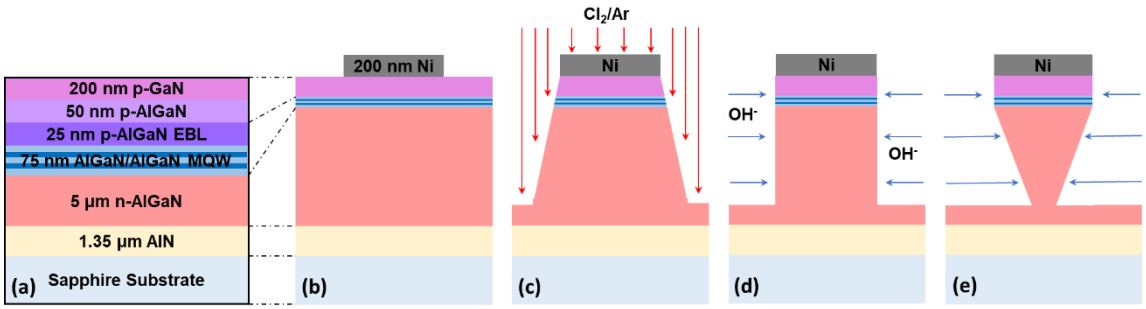

Figure 4.2.1: (a) Simplified DUV LED epitaxial layer stack (not to scale). Nanowire formation process showing (b) deposition of the Ni hard mask, (c) the Cl_2/Ar dry etch, (d) 5 min of wet etching in 40% AZ400K at 80°C, and (d) 70 min of wet etching in 40% AZ400K at 80°C.

Al-content (50% Al), but was *not* observed for AlGaN containing less than 20% Al. The etch appears to be crystallographic as evidenced by formation of a hexagonal axial cross section for all wires, but the selectivity of the wet etch against the various wurtzite crystal planes appears different for this high Al-content material. As with hydroxyl-based etching of GaN, the Ga-polar c-plane has a negligibly slow etch rate. The nanowires do not decrease in height as the etch progresses, and in instances where the Ni hard mask has delaminated, the tops of the wires are not attacked by the etch chemistry. The Ga polar surface of the c-plane repels the hydroxyl groups, resulting in a negligibly slow etch rate, while the non-polar planes $(10\bar{1}1)$ are readily etched.

The height, base, and top dimensions of the nanowires were used to calculate the taper angle α, which increased to ~11° after 70 minutes in the etch solution. Taper angle was found to be independent of wire diameter for nanowires of the same height. As described in section 4.1, it was again also found that if an AlGaN nanowire is etched long enough, the diameter of the base will approach zero, causing the nanowire to detach from the substrate and fall over. As taper angle is independent of nanowire top diameter and increases at the same rate independent of nanowire diameter, it is evident that nanowires with a smaller top diameter will detach from the substrate sooner than those with larger top diameters. Figure 4.2.2 shows nanowires with top diameters of 2 μm after etch solution, while Figure 4.2.2(c) shows nanowires with top diameters of 2 μm after 70 min in etch solution which have detached from the substate. Whether a nanowire will detach from the substrate after an arbitrary time in the hydroxyl-based etch chemistry depends upon the top diameter and height of the nanowire, as these parameters in conjunction with the undercut

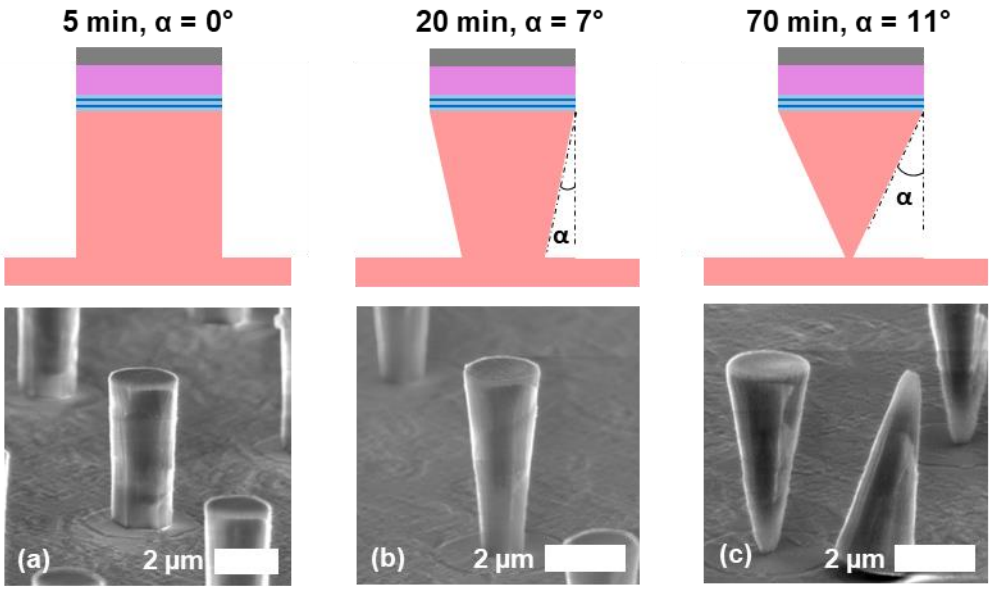

Figure 4.2.2: Nanowires with 2 µm top diameters following 5, 20, and 70 min of KOH etching, with taper angles of 0°, 7°, and 11° respectively.

angle determine the base diameter of the nanowire. The undercut and resulting inverse taper profile are likely caused by the polarity-selective nature of the hydroxyl based etch, with Ga polar surfaces repelling the hydroxyl groups while the N-polar, semi-polar, and non-polar planes are more easily etched. The relevant wurtzite crystal planes are shown in Figure 4.2.3. The top surface of the nanowire is the Ga-polar (0001) plane (Figure 4.2.3(a)), which remains unaffected by the etch by repelling the hydroxyl groups in the etch solution. The ICP dry etch is engineered to form nanostructures with relatively straight sidewalls which expose the non-polar $(10\bar{1}0)$ plane. With conventional GaN LEDs an equal Ga:N ratio exists and a controlled etch peels back layers of this plane, following a cavity etch model and reducing the diameter while maintaining a vertical wire [72]. The cavity model of the progressing wet etch can be thought of as the inverse of growth [50,73–75]. Incorporation of the Al into the hexagonal crystal structure modifies the 1:1 Ga:N ratio, with Al atoms occupying Ga sites in the crystal lattice. The hydroxyl-based etch must

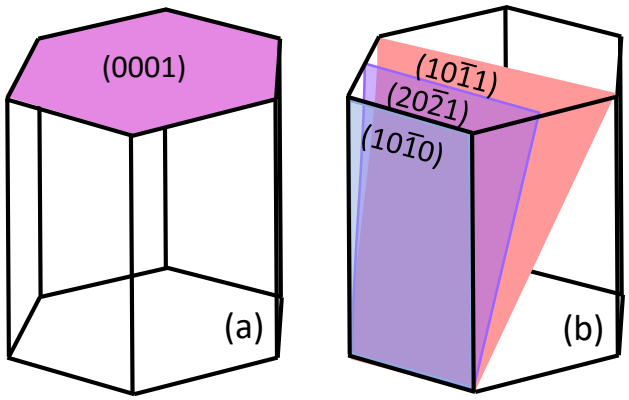

Figure 4.2.3: (a) Wurtzite unit cell highlighting the (0001) c-plane surface, (b) wurtzite unit cell highlighting the (10$\bar{1}$0) m-plane and semi-polar planes attacked by the AZ400K etch.

therefore overcome a larger energy barrier in order to remove Al atoms from the surface due to the Al-N covalent bond having a stronger binding energy (11.5 eV/atom) than the Ga-N covalent bond (8.9 eV/atom) [76]. In our nanowires it appears that the (10$\bar{1}$0) plane exposed after ~5 min of etching approximation of the (10$\bar{1}$0) is etched toward the (10$\bar{1}$1) plane [75].

4.2.3 Nanowire Liftoff and Characterization

This unique inverse taper morphology can be applied to aid in removal of nanowires from the substrate via a novel liftoff process to enable flexible device applications. The AlGaN nanowires shown in Figure 4.2.2 with top diameters of 2 μm were used to demonstrate this. In order to better identify the prior location of the nanowires on the substrate following mechanical removal, a directional deposition of Ni was performed which leaves a circular "shadowed" area beneath the tapered wires (Figure 4.2.4(a)). PDMS was then spin-coated onto the substrate to a thickness of 1 mm and acts as both mechanical supporting layer for the nanowires as well as a flexible host substrate following removal of the wires from the growth substrate, as shown in Figure 4.2.4(b).

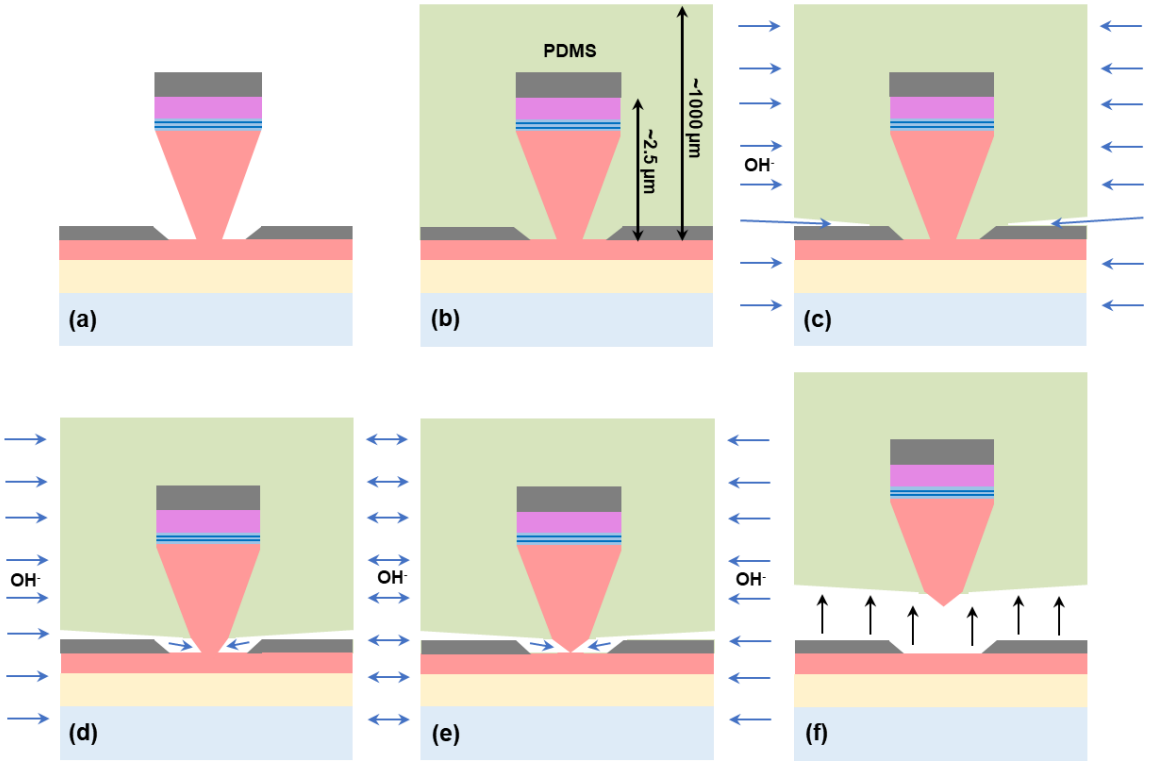

Figure 4.2.4: Cross sectional schematic of the nanowire removal process. (a) Directional Ni deposition. (b) PDMS coating. (c-e) Extended duration room temperature KOH etching. (f) Liftoff of nanowire embedded in PDMS.

Following application of the PDMS, the sample was cured at 90°C for 1 hour to increase the nanowire-PDMS adhesion and improve the mechanical stability of the PDMS film. The sample was then submerged in 100% AZ400K at room temperature to release the embedded nanowires from the host substrate. The AZ400K will not attack the PDMS or the AlGaN substrate, but slowly works its way along the interface between them, delaminating the PDMS from the underlying AlGaN and further etching the bases of the nanowires as shown in Figures 4.2.4(c-e). The narrow bases of the wires are further etched until the wires are nearly or completely removed from the underlying AlGaN layer, allowing the PDMS film in which they are embedded to be separated from the substate

with minimal force application. Were the nanowires not embedded in PDMS they would tip over onto the substrate, as shown in Figure 4.2.2(c). The PMDS acts as a mechanical support layer, maintaining the orientation and relative positions of the nanowires. After the AZ400K etch is complete, the PDMS film can be easily peeled from the original substrate as shown in Figure 4.2.5(a). The bases of the removed nanowires can be seen sticking through bottom of the peeled PDMS film in Figure 4.2.5(b). Figure 4.2.5(c) shows the apertures in the Ni layer produced by shadowing from the nanowires during direction Ni deposition. These holes in the Ni layer atop the remaining n-GaN show the prior positions of the removed nanowires. Nanowires with diameters of ~ 2 μm were successfully removed from the host substrate in this way, and the separated film exhibited exceptional flexibility despite containing thousands of rigid nanowires.

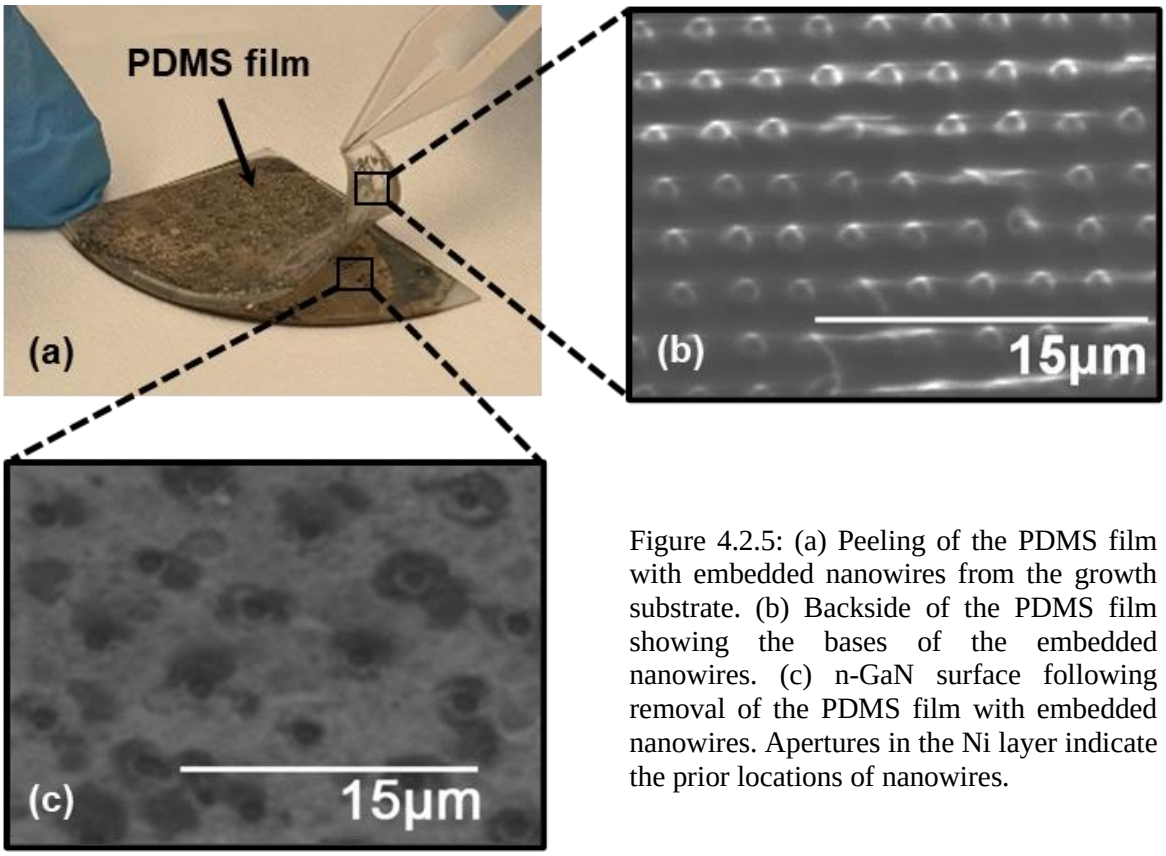

Figure 4.2.5: (a) Peeling of the PDMS film with embedded nanowires from the growth substrate. (b) Backside of the PDMS film showing the bases of the embedded nanowires. (c) n-GaN surface following removal of the PDMS film with embedded nanowires. Apertures in the Ni layer indicate the prior locations of nanowires.

Repeated flexing of the PDMS film does not appear to disturb the location and orientation of the embedded nanowires or damage the nanowires in any way. The AZ400K etching is found to be critically important for successful removal of the nanowires from the substrate. Without the extended AZ400K etch to delaminate the PDMS from the substrate and further reduce the base diameters of the nanowires, it is not possible to remove the nanowires using this method. The mechanical shear force applied to the wires by peeling the PDMS film from the substrate was found insufficient to separate the wires from the substrate. This novel AZ400K etching and PDMS liftoff process enables removal of very short nanowires from the substrate without the damage incurred by conventional mechanical exfoliation techniques. As the nanowires are fully removed from the substrate without leaving broken stubs, it may be possible for the AlN growth substrate to be reused for epitaxial growth of additional LEDs.

Optical characterization of the nanowires was performed before and after removal from the substrate in order to examine the effects of the liftoff process on the light emission properties of the nanowire emitters. Figure 4.2.6 shows the PL emission spectra of the nanowires before and after removal from the substrate. Emission at 292 nm is observed from the AlGaN nanowires embedded in the PDMS host substrate, indicating that the nanowires are intact and that the PDMS film is transparent to DUV light. In addition to its flexibility and chemical inertness, PDMS exhibits a low absorption coefficient across the DUV emission range and an index of refraction of n=1.46 which aids light extraction from the nanowires [77]. A distinct 25 nm redshift of the emission peak from 267 nm to 292 nm is observed following removal of the nanowires from the substrate. In addition to this 25 nm redshift, the nanowires show a significant increase in longer wavelength emission

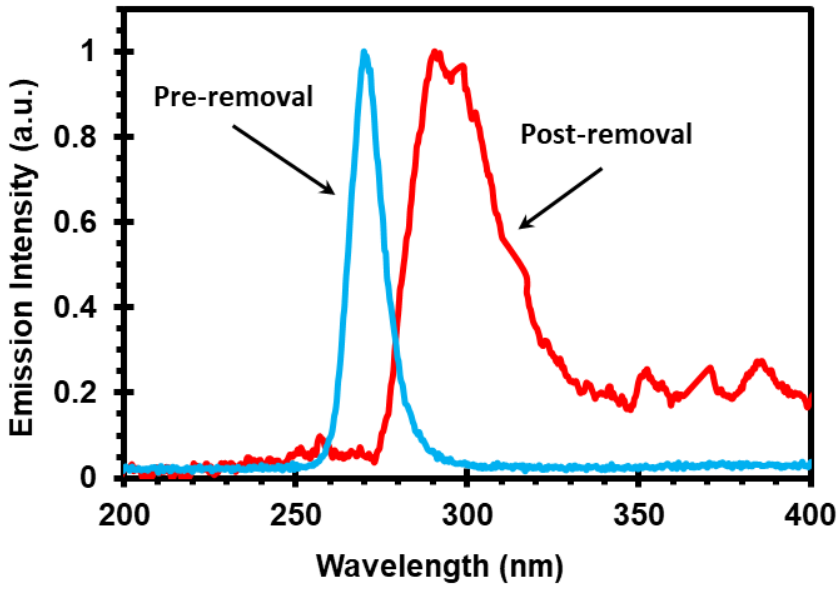

Figure 4.2.6: PL emission spectrums of the bulk epi (blue) and the nanowires embedded in the PDMS film (red). The pre- and post-removal curves have peaks at 267 nm and 292 nm respectively.

following removal from the substrate, which can be attributed to luminescence of defects in the PDMS film. AlGaN nanowires removed from their growth substrate are expected to show this behavior, with red shift of the emission peak caused by reduction of the quantum confined stark effect (QCSE) [78]. Lattice mismatch induced strain causes powerful piezoelectric polarization electric fields to develop in the QW active region which raise the electron and hole ground states further from their respect band edges, shifting the location of the ground state emission peak. Removal the nanowires from the substrate reduces this strain, reducing the internal electric fields in the QW and flattening the energy bands in the quantum wells, red shifting the emission spectrum by moving the electron and hole ground states closer to their respective band edges. Once the nanowires are removed from the substrate, they can either be transferred to an alternative substrate (and the PDMS removed via dry etch) or remain embedded in the PDMS which can act as a virtual, flexible substrate.

4.2.4 Conclusions

This work represents the first demonstration of a flexible DUV emitter. The novel "inverse taper" phenomenon discovered by our group and described in section 4.1 is critical facilitating removal of nanowires from the substrate. Hydroxyl-based wet etching of the AlGaN nanowires was used to form the inverse taper profile, with taper angles of around 11° achieved after 70 minutes in etch solution. The formation of this undercut can eventually lead to complete removal of the nanowires from the underlying substrate as the etch progresses. This undercut enables a unique PDMS liftoff process capable of removing the nanowires from the growth substrate while maintaining their orientations and relative positions. The AlGaN nanowires removed from the substrate and embedded in PDMS show a 25 nm red shift in peak emission wavelength from 267 nm to 292 nm due to a reduction of the QCSE through strain relaxation. These initial results are very promising, and demonstrate that alternative methods to conventional razor blade exfoliation are possible for fabrication of flexible nanowire optical devices. While these nanowires were not electrically driven and were instead driven via DUV PL, development of an electrically driven device using this nanowire removal approach should not be difficult. Deposition of a flexible conductive p-contact layer on the tops of the nanowires prior to thick PDMS film application and subsequent deposition of a flexible conductor on the bases of the embedded nanowires (as shown in Figure 4.2.5(c)) could allow for realization of a flexible electrically driven device. The results presented in this section were published in *Journal of Physics: Photonics* in 2021 [45].

4.3 Simulation Analysis of DUV LED Light Extraction Efficiency

4.3.1 Introduction

The prior two section, 4.1 and 4.2, describe the design, fabrication, and characterization of DUV emitting AlGaN nanowire arrays. These devices are the first of their kind formed using a top-down fabrication approach. Of particular note is our discovery of a unique inverse tapers profile which develops in high Al-content AlGaN during extended hydroxyl based wet etching. This novel phenomenon offers several unique advantages over nanowires and micropillars with vertical sidewalls, such as the ability to utilize a "self-masking" un-patterned n-metal deposition as described in section 4.1, and nanowire liftoff process described in section 4.2. Etching of GaN and InGaN with hydroxyl-based chemistries such as potassium hydroxide (KOH) and tetramethylammonium hydroxide (TMAH) has been well studied, and is even used in industrial power electronics and LED manufacturing to remove dry etch damage and improve device efficiency [48,49,51,53–55,79,80]. GaN and InGaN etch crystallographically in hydroxyl-based solutions, with the non-polar and semi-polar wurtzite planes etching rapidly while the polar c-plane has a negligibly slow etch rate [49,51,53,79,80]. High AR dry etched GaN and AlGaN structures generally have a "normal taper" profile where the base of the structure is slightly flared and has larger dimensions than the lithographically defined top diameter of the structure. Hydroxyl-based etches can be used to remove the unwanted flared bases of top-down fabricated nanowires and microstructures based on c-plane epitaxy as the etch will effectively self-terminate when a surface becomes perfectly vertical. In contrast to the well-studied behavior of this etch in GaN and InGaN, self-termination of the etch does not appear to occur in n-doped AlGaN

with Al-content of ~50-70%, leading to development of an inverse taper profile with taper angle α which continually increases until the base of the structure narrows to a point and detaches from the substrate. Figure 4.3.1 shows cross-sectional schematics and scanning electron microscope (SEM) images of our fabricated AlGaN nanowire structures with normal taper (no KOH etching), no taper (5 min KOH etching), and inverse taper (60 min KOH etching). KOH etching was performed in 40% AZ400K (a photoresist developer containing 2 wt% KOH) heated to 80°C. Details of this fabrication process were discussed in sections 4.1 and 4.2.

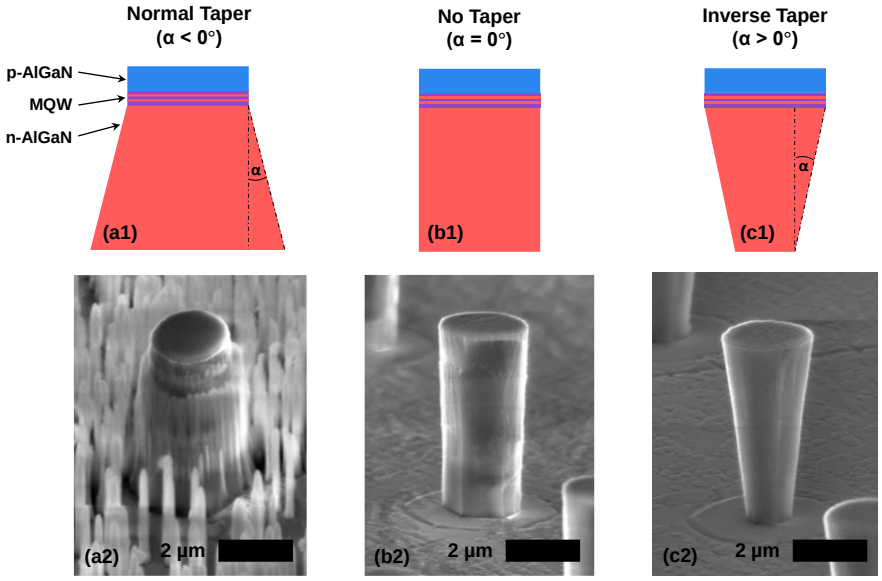

Figure 4.3.1: Cross sectional schematics showing structures with normal taper (a1), no taper (b1), and inverse taper (c1), along with representative SEM images of each structure (a2-c2).

The core goal of this dissertation research is to improve the light extraction efficiency (η_{EXT}) of DUV LEDs, as poor η_{EXT} is currently the most significant obstacle inhibiting their widespread adoption in many potential applications. The prior sections do not mention η_{EXT} extensively for the reason it is extremely difficult/impossible to measure empirically

without (very expensive) specialized equipment. The best efficiency measurements our group can make are general approximation of wall plug efficiency (WPE). As described in section 4.1, this is done by measuring the light output power of an LED using a 2D power meter, and dividing this value by the product of the current and voltage supplied during the light output power measurement. A better approximation of WPE could be obtained by packaging the LED and utilizing a integrating sphere and calibration standard to measure light output power. Our group is currently working to develop this capability, but even with these tools at our disposable, deconvolution of η_{EXT} from IQE would be very difficult and time consuming. As such, a more straightforward method of determining the η_{EXT} of our devices is desired. In this section, the effects of an inverse taper profile on the η_{EXT} of nanowires and micropillars emitting at 270 nm is explored using finite-difference time-domain (FDTD) simulations in order to understand and study the η_{EXT} effects of inverse tapered structures (Figures 4.3.1(c(1,2)) over those with vertical sidewalls (Figures 4.3.1(b(1,2)).

Previous simulation-based studies of DUV LEDs have shown that nanowires and other vertical structures can produce significant improvements in η_{EXT} when compared to conventional mesa structures with lateral dimensions (generally 20 – 1000 μm) far exceeding the mesa height (generally 100 – 500 nm) [12,14,15,40,81–84]. These enhancements are shown to be much more pronounced for TM-polarized light, which has electric field vectors parallel to the epitaxial c-plane making it difficult to extract from mesa structures [12,37]. Nanowires and micropillars with lateral dimensions (generally 100 nm – 2 μm) equal to or much smaller than their height (generally 100 nm - 5 μm) allow TM-polarized light to easily escape through their sidewalls where the electric field vectors

of TM-polarized photons are perpendicular to the AlGaN/air interface. For example, Ryu *et al.* showed through FDTD simulation that the η_{EXT} of TM-polarized light could be increased from 0.1% to more than 60% at 280 nm through use of nanorod structures with diameters of around 300 nm and heights of 1 μm, an astonishing 600-fold improvement [83]. Likewise, Ooi *et al.* showed that nanowires could improve TM- and TE-polarized η_{EXT} from 0.2% to 48% and 2% to 41% respectively, when compared to mesa LEDs emitting at 230 nm [12]. Given that differences in η_{EXT} between nanowires/micropillars and mesa LEDs are already well understood, this section focuses on the effects of nano and microstructure geometry, that is, the shapes and sizes of these structures, on TM- and TE-polarized η_{EXT}. Many different parameters are considered, including structure height, diameter, taper angle, and polarization direction. We categorize structures based on their dimensions (D_s) as either nanostructures (100 nm < D_s < 1 μm), or microstructures (D_s > 1 μm). It is important to note that while FDTD simulations are used extensively for studying the light extraction properties of LEDs and lasers and the absorption properties of solar cells and photodetectors, FDTD results should generally not be used to make empirical claims about the properties of real devices. The most effective use of FDTD simulations in making qualitative comparisons between simulated structures to determine their various performance characteristics relative to one another. This qualitative comparison approach is utilized here in order to compare the light extraction properties of various nano and microstructures.

4.3.2 Simulation Methodology

Three-dimensional (3D) FDTD simulations were used to explore the extraction efficiencies of AlGaN nano and microstructures at an emission wavelength of 270 nm.

270 nm was chosen as it lies at the center of DUV emission ranges studied by our group and is one of the most commonly explored DUV wavelengths, alongside 230 nm and 280 nm. 3D FDTD simulation has been used extensively to explore the propagation of light within the complex, multi-material structures found in LEDs, lasers, solar cells, and photodetectors [12,14,15,40,81–84]. This method models the propagation of electromagnetic waves in the time domain within an arbitrarily defined spatial domain through direct solution of Maxwell's curl equations. In this sense, it is far more accurate, albeit slower, than ray tracing approaches because it allows for the interaction and interference of electromagnetic waves as well as the interaction of waves with the propagation medium and material interfaces. The spatial domain is divided into a nonuniform Yee mesh, with increased mesh resolution near material interfaces and reduced mesh resolution in bulk material to optimize simulation time and accuracy. More details on the FDTD method can be found in Refs. [85] and [86]. Our simulations were performed using Synopsys Fullwave, a commercial FDTD software package designed specifically for modelling the propagation of light in complex structures [87]. To set up a simulation in Fullwave a structure is first designed using a specialized 3D computer aided design (CAD) software called Rsoft-CAD which is a part of the Fullwave software package. Different material types and properties can be assigned to each part of a structure to allow for the construction of complex, multi-material objects. Dipole sources are then placed manually with the structure, followed by monitor planes and volumes which can be set to capture a wide range of data including electric field intensity and luminous flux (power). TM-polarized light, which has its electric field component perpendicular to the c-axis ($\boldsymbol{E} \perp$ c-axis), is produced by a double weighted z-oriented dipole, while TE-polarized

light, which has its electric field component parallel to the c-axis ($\boldsymbol{E} \parallel$ c-axis), is produced using two single weighted dipoles, one with x-orientation and one with y-orientation.

Figure 4.3.2 shows a cross-sectional representation of a simulated structure, which has its axis aligned with z-axis. Diameter is varied from 100 nm to 1.5 μm, height from 100 nm to 3.5 μm, and taper angle α from -10° to 25° (Figure 4.3.2 shows α > 0°). All structures have a circular cross section and fixed p-AlGaN and MQW layer thicknesses. A simulation domain in the shape of a rectangular prism is defined using perfectly matched layer (PML) boundary conditions, which act as perfectly absorbing interfaces to prevent reflection of incident electromagnetic waves. The bottom of the domain is located 200 nm below the surface of the bulk n-AlGaN, while the sides and top of the domain are located 500 nm from the foremost surfaces of the structure. The x, y, and z-oriented dipoles are placed on the axis of the structure directly in the center of the MQW layer. A cubic monitor with dimensions of 20 nanometers is placed to enclose the dipole sources and measure the

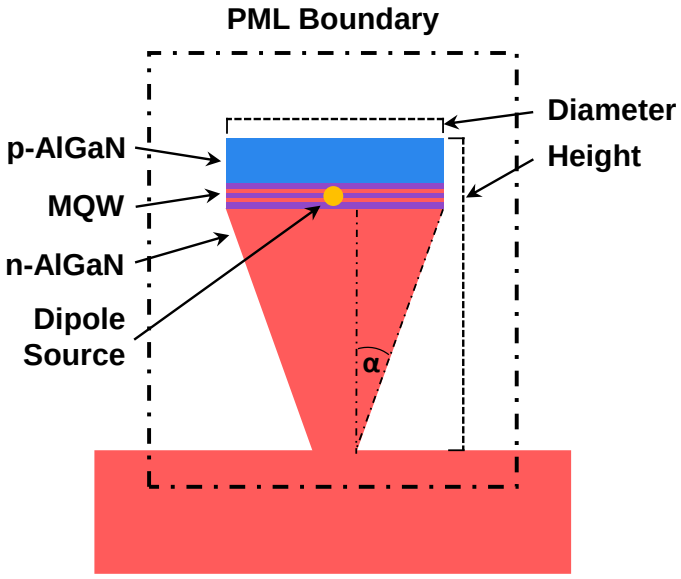

Figure 4.3.2: Cross sectional schematic showing a generalized representation of a simulated nanowire.

full luminous flux of the dipoles while six planar power monitors are located just inside the domain boundaries to measure the luminous flux which escapes from the structure. Additional planar monitors are placed to intersect the structure along its axis in order to record electric and magnetic field intensities within the structure and in the space surrounding it. Extraction efficiency is determined by taking the ratio of luminous flux measured by various planar monitors to the full flux of the source.

4.3.3 Simulation Results for Microstructures Emitting at 270 nm

Results show that narrower, taller structures yield higher η_{EXT}, and that the extraction efficiency of TM-polarized emission is larger than that of TE-polarized emission in these high AR structures. Figure 4.3.3(a) shows the η_{EXT} of 1 μm, 2.5 μm, and 4 μm tall structures with diameters of 1 μm as a function of taper angle. Structures with no taper ($\alpha = 0°$) exhibit extraction efficiencies of 40-45% for TM-polarized emission, and 28-40% for TE-polarized emission. η_{EXT} increases significantly with increasing taper angle as is shown in Figure 4.4.3(a). This effect is most pronounced in taller structures (dashed and dotted lines), with extraction efficiencies of 98% being reached for TM-polarized emission from 4 μm tall, 1 μm diameter structures at a taper angle of 7°. Shorter, 1 μm tall structures require larger taper angles to reach these higher η_{EXT} values, but TM and TE extraction efficiencies of up to 92% and 78%, respectively, are likewise obtainable for these shorter structures at a taper angle of 20°. Figure 4.4.3(a) plots the extraction efficiencies of shorter structures for larger taper angles than for taller structures due to geometric limitations. While a 1 μm tall structure can be tapered to more than 25° before separating from the substrate, a 4 μm tall structure can only be tapered to slightly more than 7° before separation occurs. The maximum taper angle of a structure with diameter D and height H

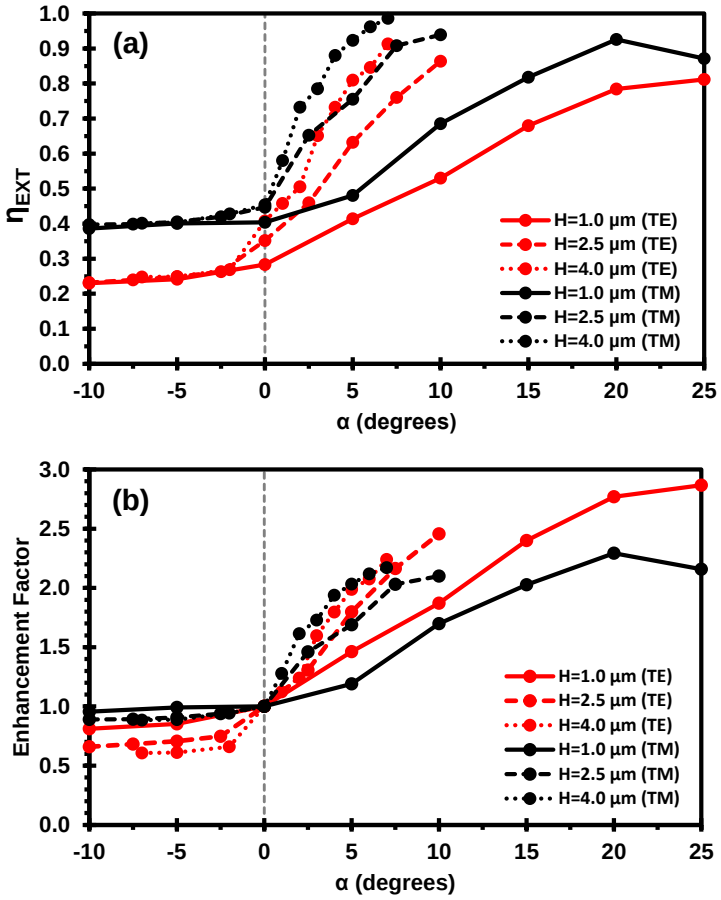

Figure 4.3.3: η_{EXT} (a) and η_{EXT} enhancement factor (b) for TE (red) and TM (black) polarizations as a function of taper angle α for 1 μm tall (solid), 2.5 μm tall (dashed), and 4 μm tall (dotted) structures with diameters of 1 μm at λ = 270 nm.

is given by $\alpha = \tan^{-1}(D/2H)$ when α is defined as shown in Figure 4.3.2. The maximum taper angled plotted in Figures 4.3.3(a) and 4.3.3(b) are 7° for 4 μm tall structures, 10° for 2.5 μm tall structures, and 25° for 1 μm tall structures. While positive taper angles are shown to produce significant increases in both TE- and TM-polarized η_{EXT} taper angles ($\alpha < 0°$) appear to have the opposite effect, with all simulated negative taper angles producing small reductions in η_{EXT}. Interestingly, the extraction efficiencies of all three structure heights shown in Figure 4.3.3(a) appear to quickly converge to the same values of ~39% for TM-polarized emission and 23% for TE-polarized emission at α = -10°. These

results further reinforce the need to eliminate the flared bases ($\alpha < 0°$) of dry-etched light emitting structures in order to improve η_{EXT}. Figure 4.3.3(b) plots enhancement factor as a function of α in order to give a more qualitative representation of the change in η_{EXT} which could be expected for non-zero taper angles with structures with $\alpha = 0°$. The data in Figure 4.3.3(b) is produced by dividing the values for all $\alpha \neq 0°$ by the extraction efficiency at $\alpha = 0°$ for each height and polarization.

While Figure 4.3.3 shows that η_{EXT} can be improved by using structures with a positive taper, Figures 4.3.4 and 4.3.5 show cross-sectional electric field intensity plots which allow for better understanding of *why* positive taper improves extraction efficiency. The electric field intensities shown in Figures 4.3.4 and 4.3.5 are captured by a monitor placed to bisect the simulated structures along their axis, with Figure 4.3.4 showing the results for TE-polarized emission and Figure 4.3.5 showing the results for TM-polarized emission. The structures shown in Figures 4.3.4 and 4.3.5 are the same structures for which η_{EXT} data is presented in Figure 4.3.3. Taper angles of -10°, 0°, 10°, and 20° are shown for 1 µm tall structures, -5°, 0°, 5°, and 10° for 2.5 µm tall structures, and -2°, 0°, 2°, and 5° for 4 µm tall structures. These cross-sectional electric field intensity plots allow for visualization of the optical modes which develop within these structures and identification of the directions in which light most efficiently extracted. It is immediately evident from Figure 4.3.4 when comparing taper angles of 0°, 10°, and 20° that the optical modes which develop within the structures become more complex as taper angle is increased.

For the TE-polarized emission shown in Figure 4.3.4, the electric field intensities in free space near the sidewalls of all structures with no taper ($\alpha = 0°$) are effectively zero, indicating that almost no light is able to escape from the sidewalls of these structures.

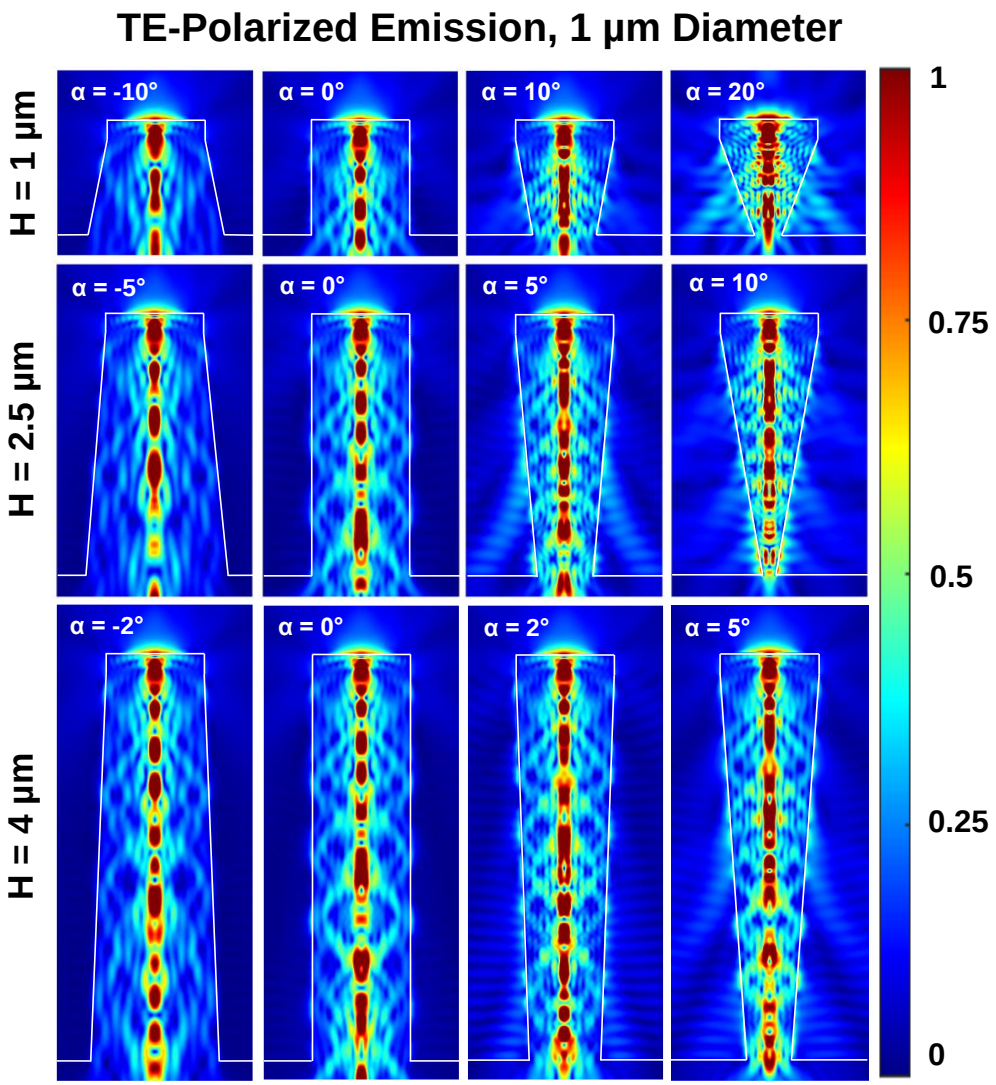

Figure 4.3.4: Cross-sectional electric field intensity plots for 1 µm, 2.5 µm, and 4 µm tall structures with diameters of 1 µm and taper angles between -10° and 20° for TE-polarized emission at $\lambda = 270$ nm.

Results are similar for negative taper angles. In contrast, structures with positive taper exhibit much higher field intensities in the adjacent free space, indicating that extraction is able to occur more readily through the sidewalls of tapered structures even for TE-polarized emission, which prefers top extraction. It can also be seen that the direction in which light

escapes from tapered structures in non-uniform, and appears to be influenced by the taper angle, structure height, and the location of optical modes on the axis of the structure. This effect is easiest to see in the 2.5 μm tall structure with a taper angle of 5°, in which two "beams" can be seen projecting downward from near the midsection of the structure at an angle of ~30°. From Figure 4.3.5, which shows TM-polarized emission, similar effects can

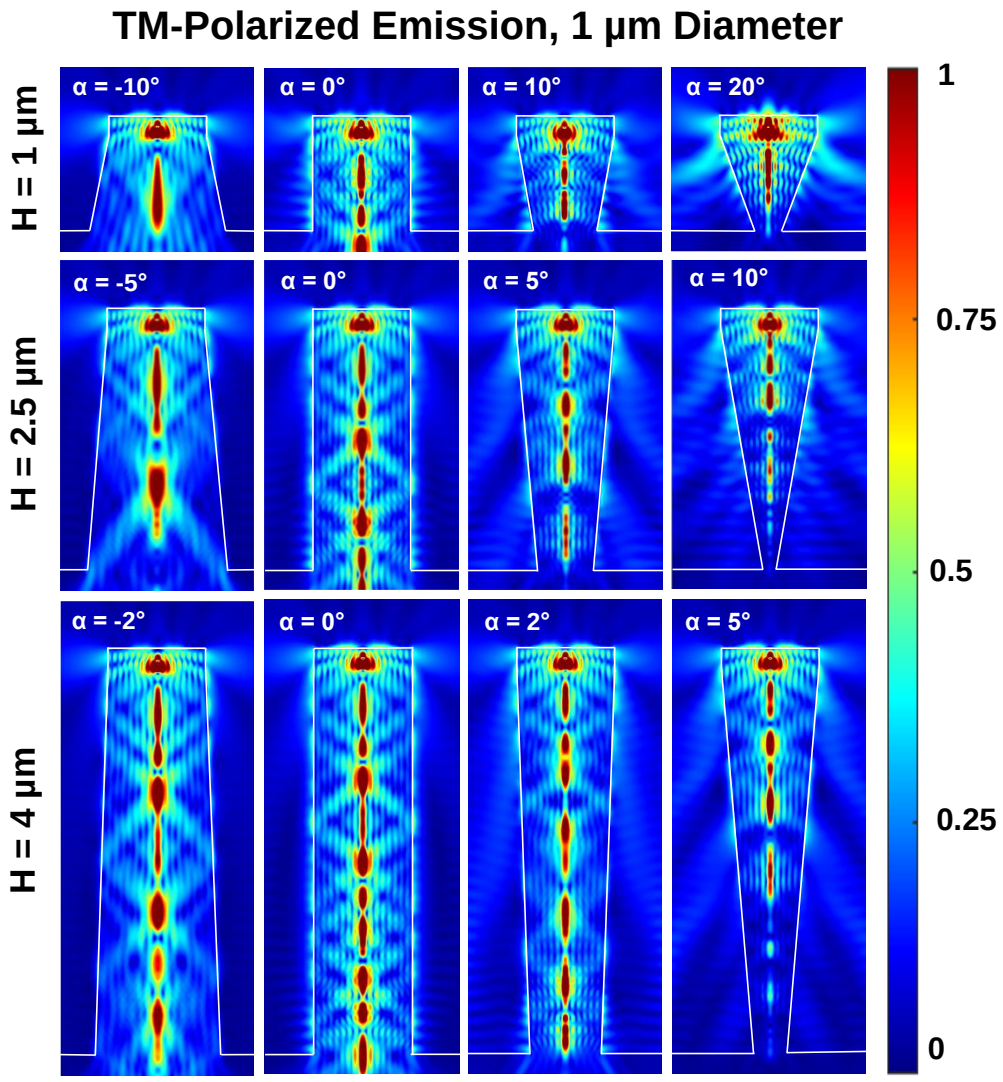

Figure 4.3.5: Cross-sectional electric field intensity plots for 1 μm, 2.5 μm, and 4 μm tall structures with diameters of 1 μm and taper angles between -10° and 20° for TM-polarized emission at λ = 270 nm.

be observed, however, in contrast to the TE-polarized emission shown in Figure 4.3.4, there are several notable differences. In the case of the TM-polarized emission shown in Figure 4.3.5, sidewall emission is significant even in structures with no taper. This trend is expected since light which has transverse *magnetic* polarization with respect to the c-plane (the horizontal top surface of a structure) will have transverse *electric* polarization with respect to a vertical interface such as a structure sidewall. Likewise, the electric field intensity above the TM-emitting structures shown in Figure 4.3.5 is effectively zero, whereas the TE-emitting structures shown in Figure 4.3.4 have distinctively non-zero field intensity in the free space directly between them. While TM-polarized emission *can* be effectively extracted from vertical structures with no sidewall taper as shown in Figure 4.3.5, positive taper angles can further enhance its extraction. The higher taper angle structures shown in Figure 4.3.5 demonstrate that large increases in free space field intensity can be produced by taper angles as small at 2°. As described for the TE-polarized emission in Figure 4.3.4, variation of structure height and taper angle appear to affect the spatial distribution of sidewall emitted light in Figure 4.3.5. For example, distinct regions of high electric field intensity can be easily seen for the 1 μm tall structure with 20° taper in Figure 4.3.5. At very large taper angles in which the base of the structure is narrowed nearly to a point, the light lost into the substrate is massively reduced, an effect which can be best seen by comparing the 4 μm tall structures with taper angles of 0° and 5°. In the structure with no taper, high electric field intensities can be seen in the substrate at the base of the structure, while in the structure with 5° taper, the field intensity is effectively zero through the substrate. The reduction of substrate light loss is due to the tapered sidewalls

acting to confine emitted light to the upper portions of the structure where it can be extracted after one or multiple reflections instead of being lost into the substrate.

Figure 4.3.6 presents the far field radiation plots of the structures shown in Figures 4.3.3-4.3.5 in a polar format. The vertical axis of these plots represents the surface normal of the simulated structures, with each dashed line representing a 30° deflection from this surface normal. The red and black curves represent the intensities of TE and TM polarized radiation, respectively, which has escaped through the tops of the structures and is incident upon a monitor which is coplanar with the top of the simulation domain. As such, Figure

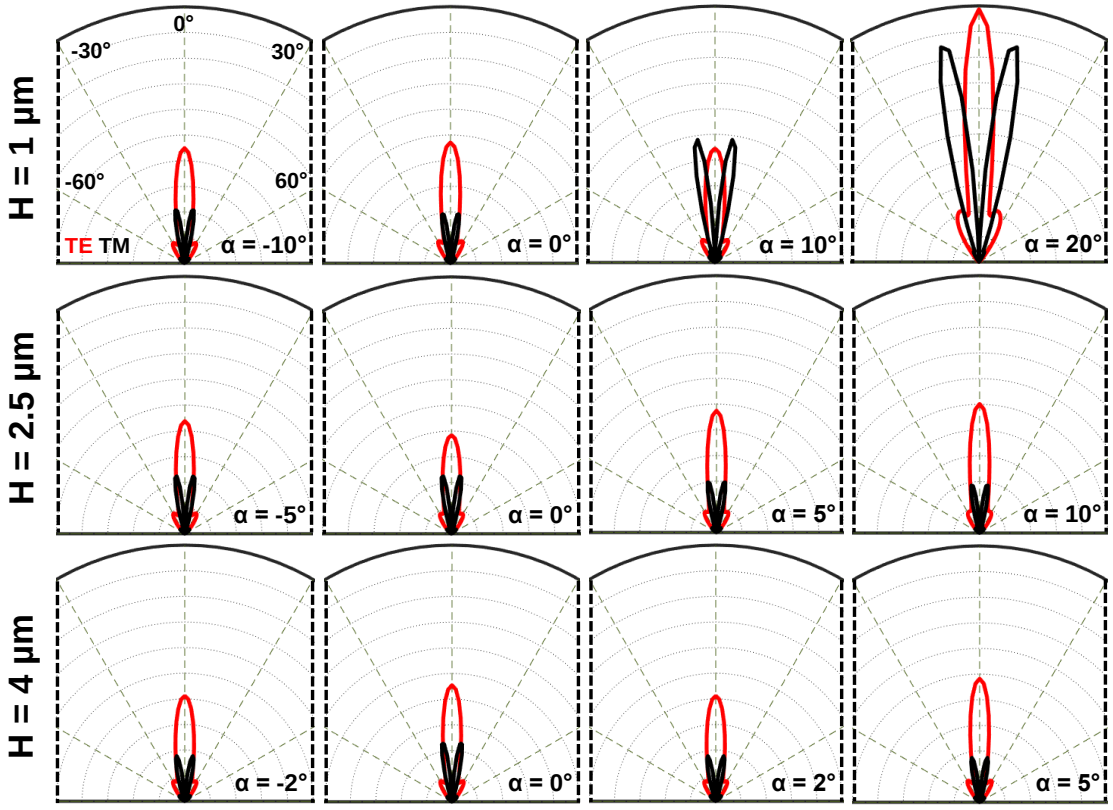

Figure 4.3.6: Far-field emission patterns for TE-polarized (red) and TM-polarized (black) light, for 1 µm, 2.5 µm, and 4 µm tall structures with diameters of 1 µm and taper angles between 10° and 20° at λ = 270 nm (the same structures whose electric field intensity plots are shown in Figures 4.3.4 and 4.3.5).

4.3.6 only represents the distribution of light which has escaped from the tops of the structures, and does not consider sidewall emission. The far field patterns appear generally uniform for all structures, with a Lambertian emission pattern for TE-polarized light and a "rabbit ears" emission pattern for TM-polarized light, both of which are consistent with existing literature [12,83,84]. The peak intensity of TE emission is generally 2-3x higher than that of TM-polarized emission, which is consistent with the well documented poor η_{EXT} TM-polarized light. However, this consistency breaks down for 1 μm tall structures with taper angles of 10° and 20°, in which the maximum intensity of TM-polarized emission approaches or exceeds that of TE-polarized emission. The increase in TM-polarized emission intensity in these two structures is due to their high taper angles relative to the other simulated structures, which serve to reflect downward emitted light back toward the top surface of these structures. The optical modes within these structures are also altered by their high taper angles which likely also contribute to modification of their far field radiation patterns. While the majority of light is extracted from the sidewalls of these structures, Figure 4.3.6 shows that modification of the top-emitted far field radiation patterns is also possible in structures with high taper angles. Existing literature has shown that narrower, taller structures improve light extraction efficiency [12,83], but it remains of interest to explore the effects of height and diameter in tapered structures.

Figure 4.3.7 shows TM (a) and TE (b) extraction efficiency as a function of structure height for diameters of 0.5 μm (dotted), 1 μm (dashed), and 1.5 μm (solid) for a fixed taper angle of 10°. It is immediately evident that, in keeping with existing literature, η_{EXT} increases with the height of the structure. Of note are the very low extraction efficiencies of structures with ARs less than unity (height/diameter). These low extraction

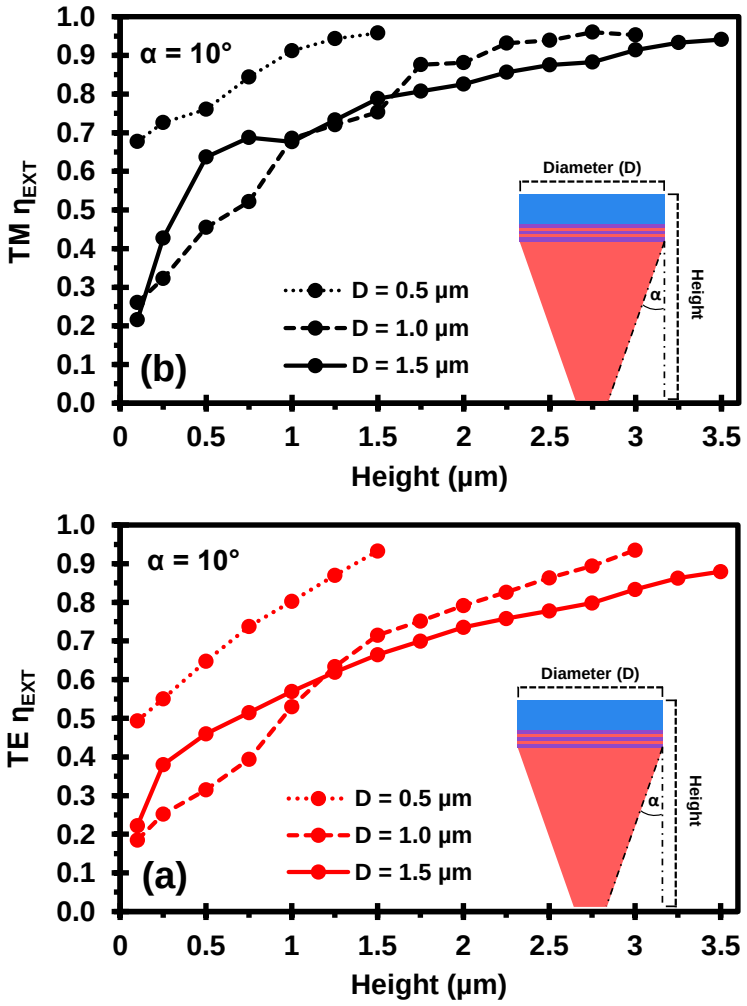

Figure 4.3.7: η_{EXT} for TM (a) and TE (b) polarizations as a function of height for structures with diameters of 0.5 μm, 1 μm, and 1.5 μm and (solid), 2.5 μm tall (dashed), and 4 μm tall (dotted) structures with diameters of 1 μm at λ = 270 nm.

efficiencies are most noticeable for structures with diameters of 1 μm and 1.5 μm, whose extraction efficiencies drop from ~60% at an AR of 1 to less than 30% at an AR of ~0.1. Low extraction efficiency is expected from low AR structures because they are very similar to the mesas which are normally used in the fabrication of LEDs and which have been shown to have poor extraction efficiencies. Figure 4.3.7 also shows a general trend of

extraction efficiency increasing with decreasing diameter. While 0.5 µm diameter structures consistently have the highest η_{EXT} at a given height, 1.5 µm diameter structures actually appear to have higher extraction efficiencies than 1 µm diameter structures at heights less than 1.5 µm. This observation holds true for both TM and TE polarizations, and is likely due the nature of the optical modes which develop within 1 µm and 1.5 µm tall structures of within this height range.

Figure 4.3.8 shows the top emission far-field polar radiation plots for 0.5 µm (red), 1 µm (black), and 1.5 µm (blue) diameter structures with heights of 1.5 µm and taper angles of 10°. The intensity of TE-polarized emission parallel to the surface normal appears to increase as the diameter of the structure decreases. This trend was also observed for other heights and is likely due to increased confinement of light in narrower structures which magnifies top emission of TE-polarized light while reducing sidewall emission. No such

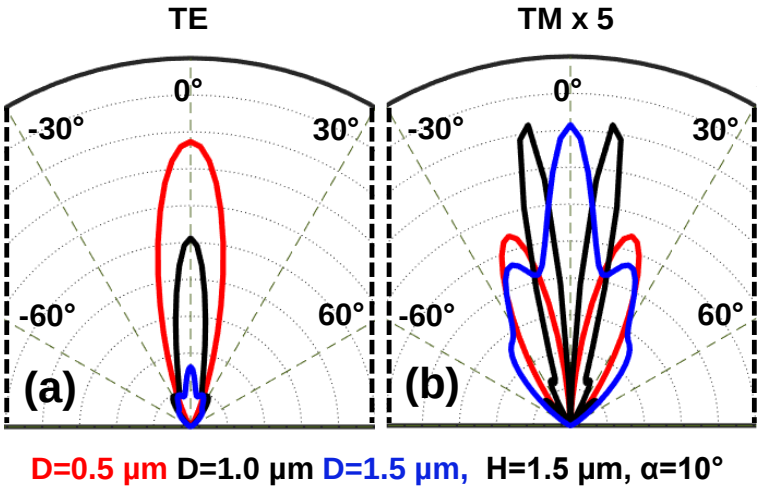

Figure 4.3.8: Far-field emission patterns for TE-polarized (a) and TM-polarized (b) light for 0.5 µm, 1 µm, and 1.5 µm diameter structures with a height at 1.5 µm and a taper angle of 10° at λ = 270 nm. TM-polarized emission (b) is multiplied by a factor of 5 to better show the emission pattern.

pattern is observed for TM-polarized emission, as each structure has approximately the same peak emission intensity, likely due to the vast majority of extraction occurring through the sidewalls. This can be attributed to alteration of the optical modes within the structures which changes the angles at which light is most effectively out-coupled through the top of the structures. Note that the TM-polarized far-field patterns in Figure 4.3.8 have been scaled up by a factor of 5 in order to make them easier to compare to one another. The far-field emission patterns for TM-polarized emission change significantly with diameter.

4.3.4 Simulation Results for Nanostructures Emitting at 270 nm

The structures explored thus far have been mostly in the "microstructure" regime, with dimensions of approximately 1 µm or greater. For DUV emission, these can be considered "super-wavelength" structures, as their dimensions are generally much larger than the wavelength of the emitted light (270 nm). It is also of interest of explore "nanostructures," with near or subwavelength dimensions closer to the wavelength of the emitted light in order to determine if the effects of height, diameter, and taper angle change for these smaller structures. Figure 4.3.9 compares the extraction efficiencies (a) and extraction efficiency enhancement factors (b) for 1 µm tall, 1 µm diameter structures (solid), and 500 nm tall, 500 nm diameter structures (dashed) as a function of taper angle. All structures have an AR of 1. TM-polarized η_{EXT} is shown in black, while TE-polarized η_{EXT} is shown in red. It is immediately evident that, despite the identical aspect ratios of these two sets of structures, the larger 1 µm structures benefit far more from higher taper angles than the 500 nm structures. For example, at 20°, the TM extraction efficiency of the 1 µm structure is enhanced by 2.3x, while the TM extraction efficiency of the 500 nm

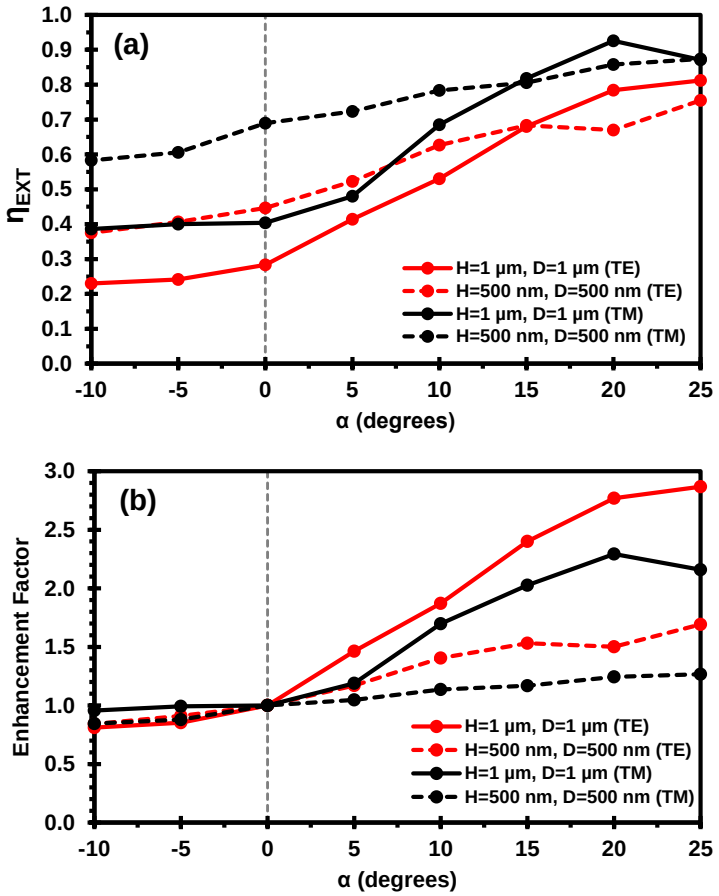

Figure 4.3.9: η_{EXT} (a) and η_{EXT} enhancement factor (b) for TE (red) and TM (black) polarizations as a function of taper angle α for 1 μm tall, 1 μm diameter structures (solid), and 500 nm tall, 500 nm diameter structures (dashed) at λ = 270 nm. Both structures have ARs of 1 (height/diameter).

structure is enhanced by only 1.25x. As can be seen from Figure 4.3.9(a), this is due mostly to the initial (α = 0°) TM η_{EXT} of the 500 nm structure being much higher (69%) than that of the 1 μm structure (40%). Smaller improvements to extraction efficiency are realized in smaller structures as taper angle is increased simply because η_{EXT} is inherently higher in smaller structures leaving less room for improvement. The key takeaway from this comparison is that extraction can be improved either through use of smaller structures with little to no taper, or larger structures with higher taper angles.

Figure 4.3.10 shows the extraction efficiencies (a) and extraction efficiency enhancement factors (b) for four different nanostructure sizes. 500/100 nm tall/diameter nanostructures are represented by diamonds and solid lines, 500/500 nm nanostructures by circles and long dashed lines, 1000/100 nm nanostructures by triangles and dotted lines, and 1000/500

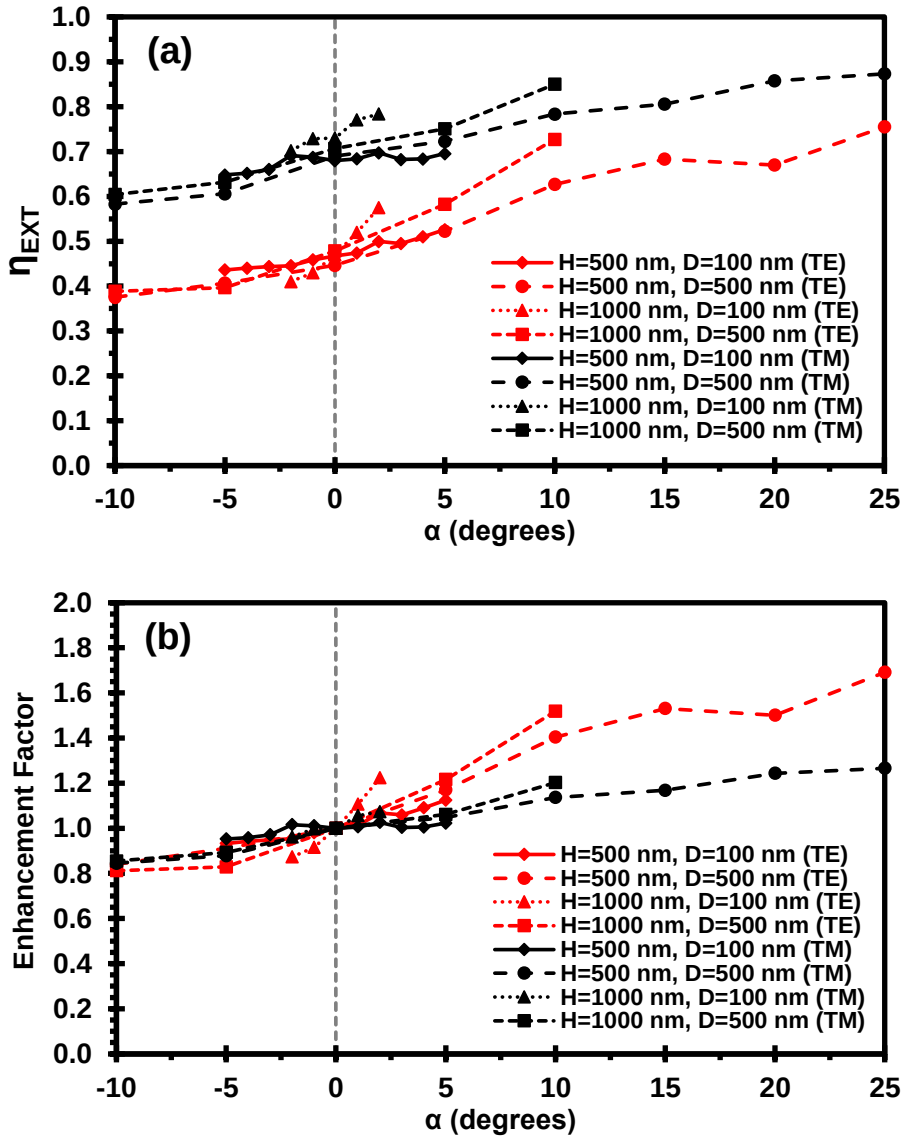

Figure 4.3.10: η_{EXT} (a) and η_{EXT} enhancement factor (b) for TE (red) and TM (black) polarizations as a function of taper angle α for 500/100 nm tall/diameter (diamond), 500/500 nm (circle), 1000/100 nm (triangle), and 1000/500 nm (square) structures at λ = 270 nm.

nm nanostructures by squares and short dashed lines. TE and TM polarizations are shown in red and black respectively. It can be seen from Figure 4.3.10(a) that TE-polarized emission benefits significantly more from higher taper angles than TM-polarized emission. This trend was not observed in the larger microstructures described previously, however the magnitude of enhancement for TE-polarized extraction efficiency is still lower in these nanostructures than it is in microstructures at equivalent taper angles. This trend is in keeping with our previous observation that larger structures almost universally benefit more from higher taper angles. It can also be seen when comparing Figure 4.3.10(a) and Figure 4.3.3(a) that the difference between TE and TM polarized extraction efficiency at $\alpha = 0°$ is larger for nanostructures than for microstructures. In Figure 4.3.3(a) η_{EXT} at $\alpha = 0°$ increases from an average of around 35% for TE polarized emission to around 45% for TM polarized emission, a difference of around 10%. This difference increases to around 25% in Figure 4.3.10(a), showing that η_{EXT} is more sensitive to the polarization of emitted light in smaller structures.

Cross-sectional electric field intensity plots at select taper angles for 100 nm diameter nanostructures are shown in Figure 4.3.11. As in Figures 4.3.4 and 4.3.5, structures with no sidewall taper exhibit very low TE polarized field intensities in the free space near the structure sidewalls, indicating that extraction of TE-polarized light from the sidewalls is negligible in these structures. Results are again similar for negative taper angles. As in Figure 4.3.4, TE-emitting structures with positive taper angles show much higher field intensities in the free space adjoining their sidewalls, indicating that extraction through the sidewalls in enhanced by even very small taper angles for TE-polarized emission. In contrast, and in keeping with the results shown in Figure 4.3.10, TM-polarized

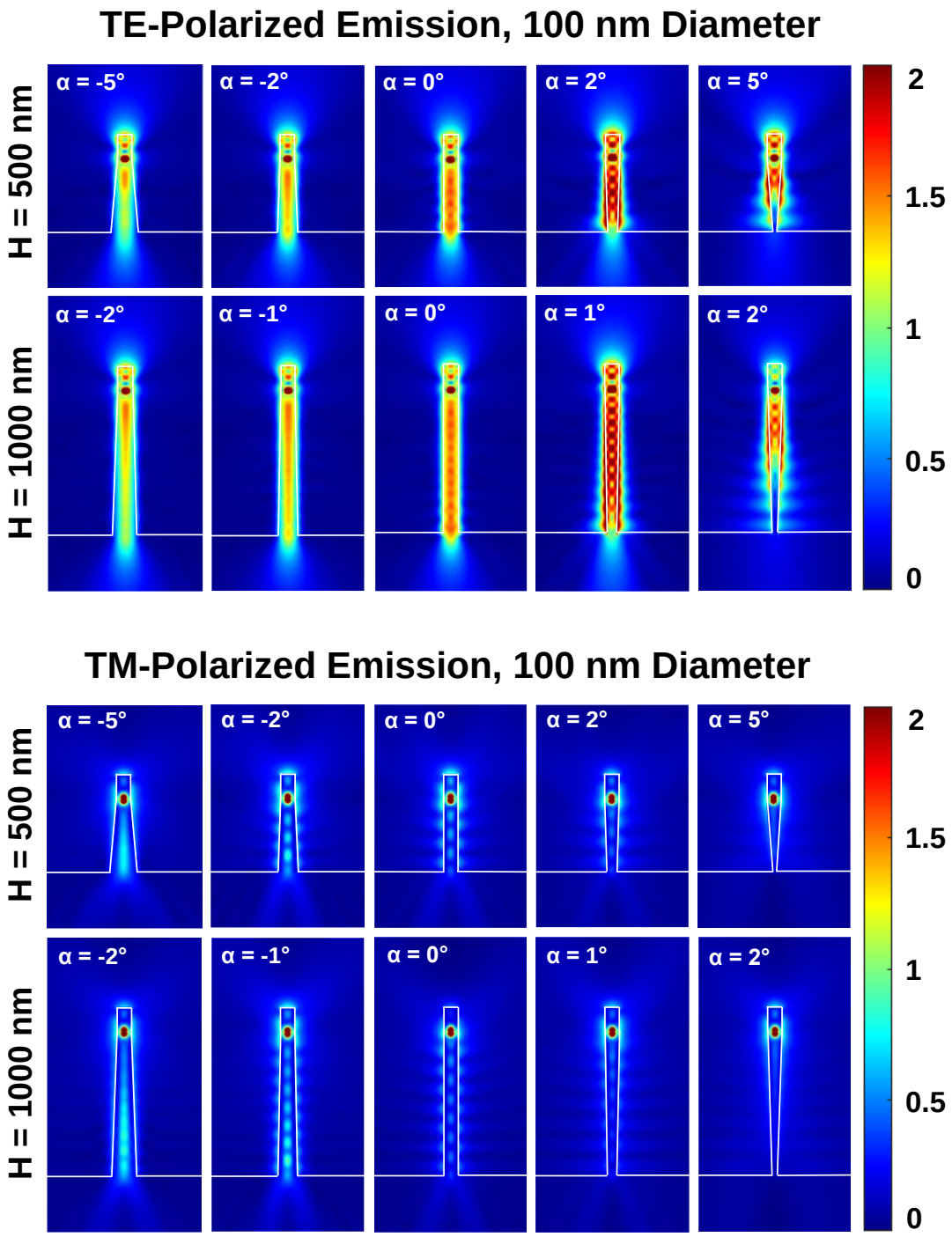

Figure 4.3.11: Cross-sectional electric field intensity plots for 500 nm and 1000 nm tall structures with diameters of 100 nm and taper angles between -5° and 5° for TE-polarized (top) and TM-polarized (bottom) emission at λ = 270 nm. Field intensity is halved in comparison to Figures 4, 5, and 12 to ensure cavity modes can be seen.

emission appears less affected by positive taper angles. As TM-polarized emission is already easily extracted from structures with such small diameters, there is little room for extraction to be further improved by the addition of small positive taper angles. As shown in Figures 4.3.4 and 4.3.5, structures with close to their maximum taper angle with very small base diameters can be seen to lose significantly less light into the substrate. This is especially noticeable in Figure 4.3.11 for TE-polarized emission. From Figure 4.3.11 it can also be seen these narrower, "subwavelength" 100 nm diameter structures are much more sensitive to the development of confined optical modes than larger structures. In the top half of Figure 4.3.11, which shows results for TE-polarized emission, all nanostructures have extremely high internal electric field intensities. Even very small increases in taper angle serve to drastically increase the field intensity in some regions. Note also that the maxima of the scale bar in Figure 4.3.11 is doubled with respect to Figures 4.3.4 and 4.3.5 in order to make the optical modes visible. While confinement of TE-polarized emission seems to be much greater in these smaller structures, TM-polarized emission appears unaffected, as it is easily extracted from the sidewalls, making it far less dependent on the size and taper angle of these nanostructures. The key conclusion of this analysis of nanostructures vs microstructures is that larger structures stand to benefit much more from an inverse taper profile, while smaller structures, which have inherently high extraction efficiency, see more limited improvements at equivalent taper angles. Additionally, the optical modes which develop within these structures likely play a key role the extraction of light from near and subwavelength structures, while larger microstructures are less susceptible to this influence.

4.3.5 Conclusion

Light extraction from both AlGaN microstructures and nanostructures was investigated at 270 nm using FDTD simulations in order to better understand the effects on η_{EXT} of parameters such structure height, diameter, and taper angle. Results showed that significant improvements to η_{EXT} can be obtained through use of an "inverse taper," in which the base of the structure is narrowed relative to the top of the structure. In the case of microstructures with diameters of 1 μm and heights > 1 μm, η_{EXT} was shown to be increased from around 45% to more than 95% (a 2.1x enhancement) for TM-polarized emission, and from around 35% to more than 85% (a 2.4x enhancement) for TE-polarized emission by a taper of only 5°. Cross-sectional electric field intensity plots visually illustrate how tapered sidewalls improve the extraction of light into free space and depict the variations in the internal optical modes which occurs as the size and taper angle of these structures are changed. In smaller nanostructures the effects of an inverse taper were found to be less significant, due to primarily to the intrinsically higher extraction efficiencies of structures with diameters < 500 nm. In comparison to microstructures, in which extraction efficiency enhancements of more than 2x could be achieved at a taper of only 5°, no more than 1.2x enhancement was realized for nanostructures at the same angle. In keeping with the findings of other publications, our results also show that η_{EXT} can also be increased by reducing the diameters of light emitting structures or by increasing their height. Light extraction has long been the single most significant bottleneck preventing the development of high EQE DUV LEDs.

The findings of this simulation study alongside the experimental results discussed in section 4.1 and 4.2 show that top-down fabricated nanowire and micropillar array LEDs

may be a viable alternative to conventional planar mesas for DUV LEDs. Of particular importance is the indication by simulation results that significant improvements in η_{EXT} which can be obtained for DUV emitting nanowires and micropillars through use of an inverse taper profile. The fact that this novel phenomenon, found only in high Al-content, DUV emitting AlGaN, can aid both in the fabrication process as well as in enhancing light extraction efficiency, makes it of great interest for further exploration. The results presented in this section were published in *IEEE Photonics Journal* in 2022 [103].

4.4 AlGaN-delta-GaN µLEDs Emitting at 262 nm

4.4.1 Introduction

While η_{EXT} is indisputably the single largest factor inhibiting the realization of DUV emitting LEDs with efficiencies comparable to their blue emitting counterparts, IQE also remains a notable issue. There primary issue limiting the IQE of DUV emitting LEDs is the quantum confined stark effect, discussed in section 1.5.2. The quantum confined stark effect, or QCSE, is a phenomenon in which the strong polarization fields in AlGaN epitaxial layers lead to significant energy band bending which pushes the electron and hole wavefunctions in the conduction and valence bands to opposite sides of the quantum well, reducing the radiative recombination rate of electrons and holes. In addition, valence band mixing occurs as the Al content of AlGaN is increased, and leads to upward movement of the crystal field split-off hole (CH) valence subband relative to the heavy hole (HH) subband. As the CH subband approaches and eventually bypasses the HH subband, the fraction of light emitted with TM-polarization increases and eventually surpasses 50%, at which point emission is considered TM-dominant. This causes η_{EXT} to decrease with decreasing Al-content/emission wavelength, as TM-polarized light has a much lower extraction efficiency from conventional planar mesa structures as discussed in section 1.5.3.

One method of mitigating the IQE impact of the QCSE and the η_{EXT} effects of valence band mixing is to modify the design of the quantum well (QW). Our group previously demonstrated the usefulness of an AlGaN-delta-GaN QW design for improving both the IQE and η_{EXT} of DUV emitting LEDs [38,68,88–92]. This approach utilizes an ultra-thin GaN “delta” layer inserted into a AlGaN square in order to improve wavefunction

overlap and rearrange the valence band structure in the active region, mitigating the valence band mixing effect which occurs in AlGaN square wells as Al-content is increased. Our early research into use of a delta-GaN QW designs utilized AlN barrier layers [38,88], and culminated in the growth of an AlN/AlGaN/delta-GaN (barrier/sub-QW/delta-layer) active region sample via molecular beam epitaxy (MBE). The IQE of this sample was measured experimentally using cryogenic-PL to be ~85% at an emission wavelength of 255 nm, which is significantly higher than prior reported IQEs for devices emitting at such a short wavelengths [90,91].

While these early results were extremely promising, the AlN barrier layers within the quantum well lead to high levels of piezoelectric strain in the active region. To address this, we performed numerical simulation studies of the effects of barrier layer Al-content on the physical and optical properties of delta-GaN active regions using a self-consistent six-band $k \cdot p$ model [68]. This study investigated the effects of parameters such as delta-GaN layer thickness, sub-QW layer thickness and composition, and barrier layer composition in order to create a better optimized delta-GaN active region. The results of this study revealed that high Al-content in the barrier region increased the electrostatic field strength in the active region, worsening the QCSE and red-shifting the emission wavelength. This effect can be seen in Figure 4.4.1, which shows the bandstructures of an optimized AlGaN/AlGaN/delta-GaN QW (a) and an AlN/AlGaN/delta-GaN QW (b). The reduced band bending and increased wavefunction overlap can be easily seen when comparing the two active region designs. Active regions with smaller Al-content differences between the barrier and sub-QW regions showed greater spontaneous emission

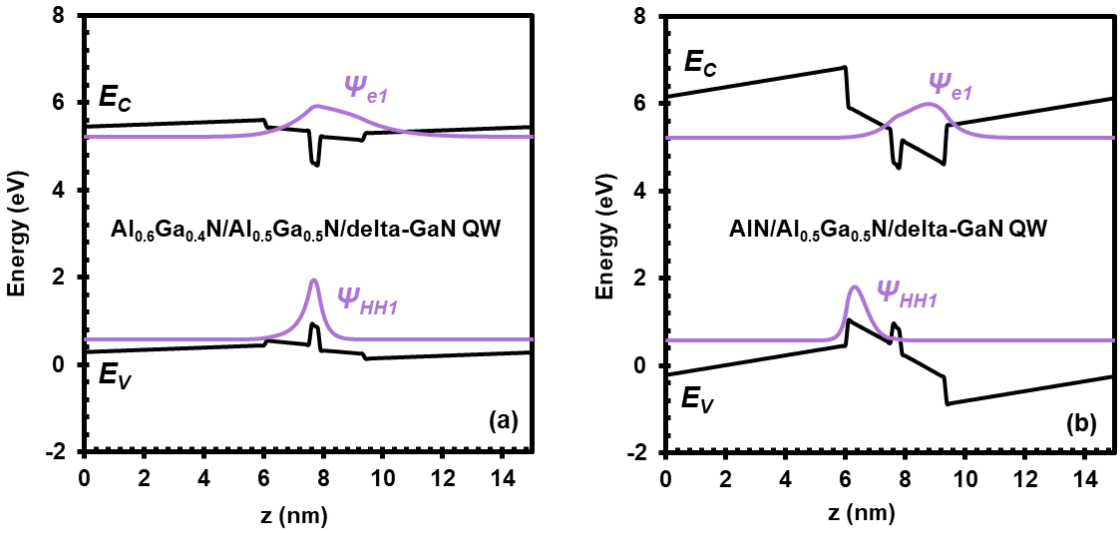

Figure 4.4.1: Bandstructures with overlayed electron and hole wavefunctions of a $Al_{0.6}Ga_{0.4}N/Al_{0.5}Ga_{0.5}N$/delta-GaN QW (a) and a AlN/$Al_{0.5}Ga_{0.5}N$/delta-GaN QW (b).

rates due to the reduction of strain effects and polarization field intensities. Engineering of the sub-QW Al content, barrier Al content, and delta-GaN layer thickness was found capable of maintaining an IQE of ~90% over the entire DUV emission regime, from 230 nm to 280 nm. When compared with conventional AlGaN square well designs, spontaneous radiative recombination rates were enhanced by up to 40x. FDTD simulations showed that η_{EXT} could be enhance by 3-7x when compared to conventional AlGaN square wells emitting at the same wavelength due to reduction in TM-polarized emission [68].

Our simulation results for "AlGaN-delta-GaN" active regions which forego the typical AlN barrier layer in favor of a more optimized AlGaN barrier layer design are extremely promising. However, this structure has not yet been demonstrated experimentally. In fact, even the AlN-delta-GaN active region grown by MBE described in Refs. [90,91], was not a fully functional, electrically driven device. As such, full experimental demonstration of this active region is desirable in order to more convincingly

assert the effectiveness of AlGaN-delta-GaN active regions for DUV emission. In this work, we fabricate electrically driven μLEDs with dimensions between 10 μm and 30 μm based on an $Al_{0.9}Ga_{0.1}N/Al_{0.75}Ga_{0.25}N$/delta-GaN MQW active region. Results show a turn on voltage of ~ 5-6 V, with series resistance dominated post-threshold characteristics. Emission peaks for 10 μm and 30 μm μLEDs were located at 262 nm and 264.5 nm respectively, extremely close the 265 nm emission wavelength predicted by our *k·p* model. Emission linewidths were also extremely narrow, at 7.1 nm and 13.6 nm for 10 μm and 30 μm μLEDs respectively. Power measurements showed much higher light output power densities for the smaller 10 μm devices, increasing from ~50 mW/cm^2 at 100 A/cm^2 to nearly 400 mW/cm^2 at 800 A/cm^2. Efficiency droop onset occurred at 83 A/cm^2 for 30 μm devices and at 200 A/cm^2 for 10 μm devices. Combined, these results show that delta-GaN active region could be a viable alternative to conventional design for improving both the IQE and η_{EXT} of DUV emitting LEDs.

4.4.2 μLED Fabrication

The epitaxy utilized in this work was based on our group's prior works as described in section 4.4.1. Six-band *k·p* simulations were used to optimize an active region to emit at ~265 nm, which was then grown using MOCVD by a commercial vendor. The epistack consisted of a 2.2 μm AlN buffer layer, followed by 600 nm $Al_{0.8}Ga_{0.2}N$, 1 μm n-$Al_{0.7}Ga_{0.3}N$, a 4x MQW, 100 nm p-$Al_{0.7}Ga_{0.3}N$, and 20 nm p^+-GaN to reduce contact resistance. The active region consisted of 5 2.5 nm $Al_{0.9}Ga_{0.1}N$ barrier layers, 8 1.5 nm $Al_{0.75}Ga_{0.25}N$ sub-QW layers, and 4 0.5 nm GaN delta layers. A simplified, not-to-scale cross section of this epistack is shown in Figure 4.4.2. The sample was prepared by first

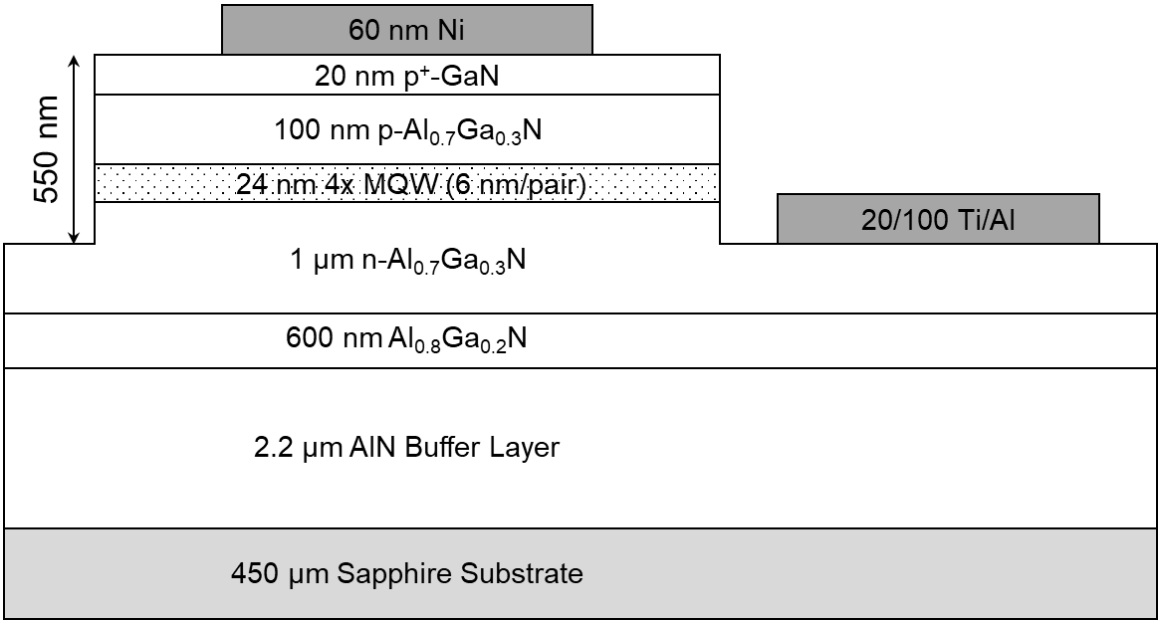

Figure 4.4.2: Not-to-scale cross sectional representation of a completed µLED device.

dicing a 50 mm wafer into quarters. The dicing resist was then stripped in NMP for 24 hours and ultrasonicated to remove sapphire particles left on the resist surface after dicing. 500 nm of TEOS was then deposited via PECVD to act as a dry etch mask for the mesa etch. Following dose/focus lithography optimization, hexamethyl disilazane (HMDS) was applied to the TEOS surface to ensure sufficient adhesion of photoresist. Liftoff resist (LOR 5A) was then spun onto the sample at 2700 rpm and baked at 170°C for 5 min, followed by positive photoresist (AZ1512), spun at 3000 rpm and baked at 100°C for 2 min (see Table 3.3.1). The sample was then exposed using a Heidelberg 405 nm LDW system, post exposure baked at 110°C for 3 min, and developed in CD-26 for 2 minutes.

With the L1 (mesa) lithography completed, the sample was then dry etched in a fluorine plasma to transfer the photoresist patterns into the TEOS etch mask. This etch was performed using an CCP-RIE reactor at 130 mtorr, with 200 W RF power, and gas flows

to 60/70/6 sccms $CF_4/CHF_3/O_2$ respectively. At an etch rate of ~ 60 nm/min, 15 1 min etch cycles were used to etch through the 500 nm TEOS layer, and overetch of ~80%, in order to ensure complete removal of the TEOS in the opened areas. This seemingly excessive overetch was utilized since the fluorine plasma will etch the exposed p-GaN at only a few nanometers per minutes, and complete clearing of the TEOS from all opened regions is essential in facilitating a successful etch of the underlying GaN. 1 minute etch cycles were used instead of a continuous 15 min etch in order to more reliably control the etch rate and heated of the sample to avoid burning of the photoresist. The photoresist layer softened in NMP for 30 min and ashed for 20 min in a 900W 300 sccm O_2 plasma to ensure completed removal of the remaining photoresist from the TEOS surface.

Following the transfer of the L1 pattern into the TEOS layer, an ICP/CCP-RIE dry etch was used etch the AlGaN epistack to a depth of ~550 nm, forming the mesa structures of the μLEDs. This etch was performed at 30 mtorr, with ICP/CCP RF powers of 350/75 W, gas flow rates of 32/8/5 sccms $Cl_2/BCl_3/Ar$, and an electrode temperature of 20°C. At an etch rate of ~350 nm/min, a 95 second (1.58 min) etch was used to obtain a depth of 550 nm, placing the bottom of the etch near the center of the 1 μm thick n-$Al_{0.7}Ga_{0.3}N$ layer. This etch depth was measured via profilometer, considering erosion of the TEOS mask at ~40 nm/min. The TEOS mask was then stripped in 10:1 BOE for 12 min, a 140% overetch, to ensure complete removal of the TEOS and exposure of the p-GaN surface.

With the μLED mesas now formed, the sample was subjected to a 20 min etch in 20% AZ400K (0.4 wt% KOH) at 90°C to remove the minimal micromasking present and remove dry etch damage on the mesa sidewalls. Figure 4.4.3 shows SEM images of the

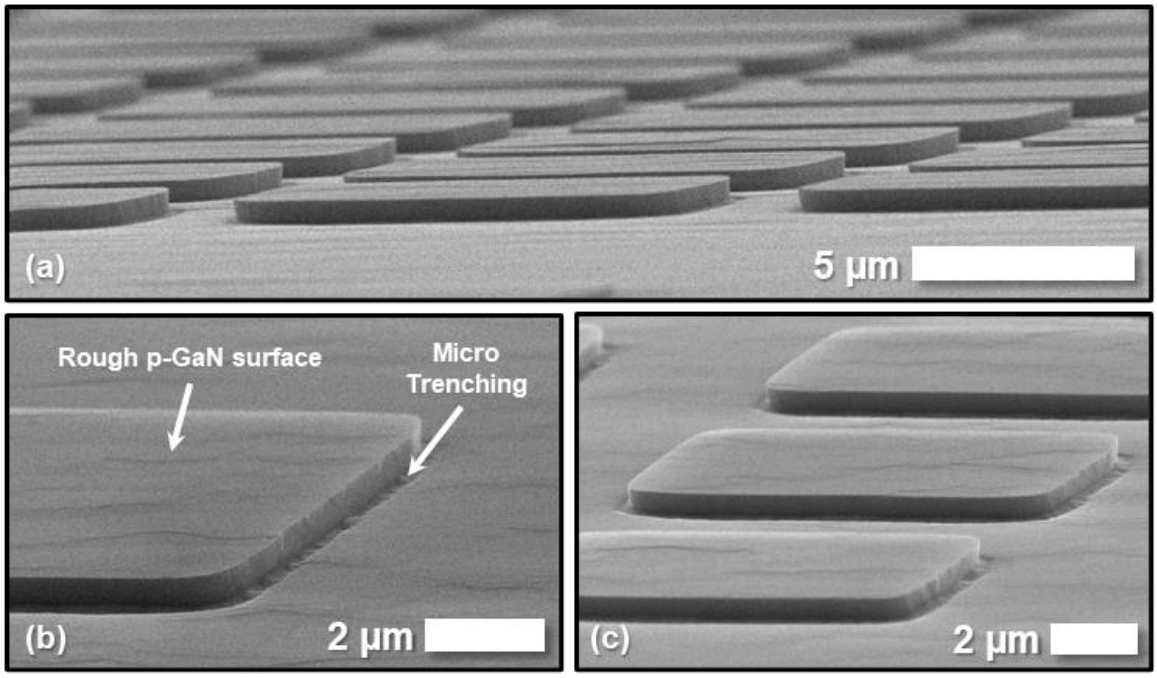

Figure 4.4.3: SEM images of 10 µm µLED mesas taken at 85° (a) and 80° (b,c) off normal. Roughness of the p-GaN surface and micro-trenching are highlighted in (b).

µLED mesas following this AZ400K etch. Of note are the unusually high roughness of the p-GaN surface and the micro-trenching highlighted in Figure 4.4.3(b). The roughness of the p-GaN surface is indicative of relatively poor-quality epitaxial growth, which is often unavoidable when growing high Al-content AlGaN at very high temperatures. Micro-trenching is a phenomenon in which high energy ions, accelerated by the plasma sheath during dry etching, deflect from the sidewalls of an etched structure, increasing the effective physical etch rate of the region directly adjacent to structure sidewalls and leading to formation of the trenchlike structures which can be seen in Figures 4.4.3 (c, d).

Following completion of the AZ400K etch, L2 (p-contact) lithography was performed. HMDS was applied, and LOR5A and AZ1512 were again coated and baked using their standard spin speeds/bake temperatures (see Table 3.3.1). The sample was then exposed using LDW, post exposure baked at 110°C for 3 min, and developed in CD-26 for

2.5 minutes to ensure sufficient undercut of the LOR layer. The sample was then etched for 30 seconds in 20% HCl to remove surface residues and native α-Ga_2O_3 before being loaded into an electron beam evaporator. Ni evaporation was started at a base pressure of $1.5x10^{-6}$ torr, and a deposition rate of ~1.5 Å/s was used to deposit ~ 80 nm of Ni. The sample left in NMP for ~20 hours and then ultrasonicated in NMP for 10 min in order to ensure complete liftoff of the Ni. The Ni p-contact layer was then RTA annealed for 2 min at 550C in O_2 in order to reduce its contact resistance. Annealing of the Ni causes an expected color change from silver to blue/purple of the Ni surface due to formation of Ni oxides, as can be seen in Figure 4.4.5(c).

The n-contact (L3) was then formed in a similar manner to the p-contact, with HMDS, LOR5A, and AZ1512 applied to the sample and exposed using LDW. A 3 min 110°C post exposure bake and 2.5 min develop were then performed, followed by a 50 W lower power O_2 descum and a 30 second etch in 20% HCl. The sample was then loaded into an electron beam evaporator, and Ti was deposited starting at a base pressure of $2x10^{-6}$ mtorr. 35 nm of Ti was deposited at a deposition rate of ~ 1 Å/s. The sample was then transferred (in less than 3 min) to a thermal evaporator, and Al deposition was started at a base pressure of $5x10^{-6}$ torr. 200 nm of Al was deposited at a deposition rate of 3 Å/s. The sample was then left in NMP for 30 hours, and ultrasonicated in NMP for 20 min to ensure complete liftoff the Ti/Al layer. This Ti/Al n-metal was then annealed for 2 min at 650°C in N_2.

With the µLEDs themselves now fully fabricated, two supplementary layers (L4 and L5) fabricated to determine the feasibility of addressing entire arrays of devices in parallel. A 200 nm TEOS layer was deposited via PECVD to act as a spacer dielectric,

allowing p-traces to cross over the underlying n-traces. Standard LOR5A/AZ1512 lithography was then performed to mask a dry etch of this TEOS layer, opening contact cuts over the p-contacts of each μLED as well as over the n-contact pads adjacent to each array of devices. This etch was performed using the same etch tool and parameters as the aforementioned dry etch of the TEOS etch mask layer for L1. Following contact open

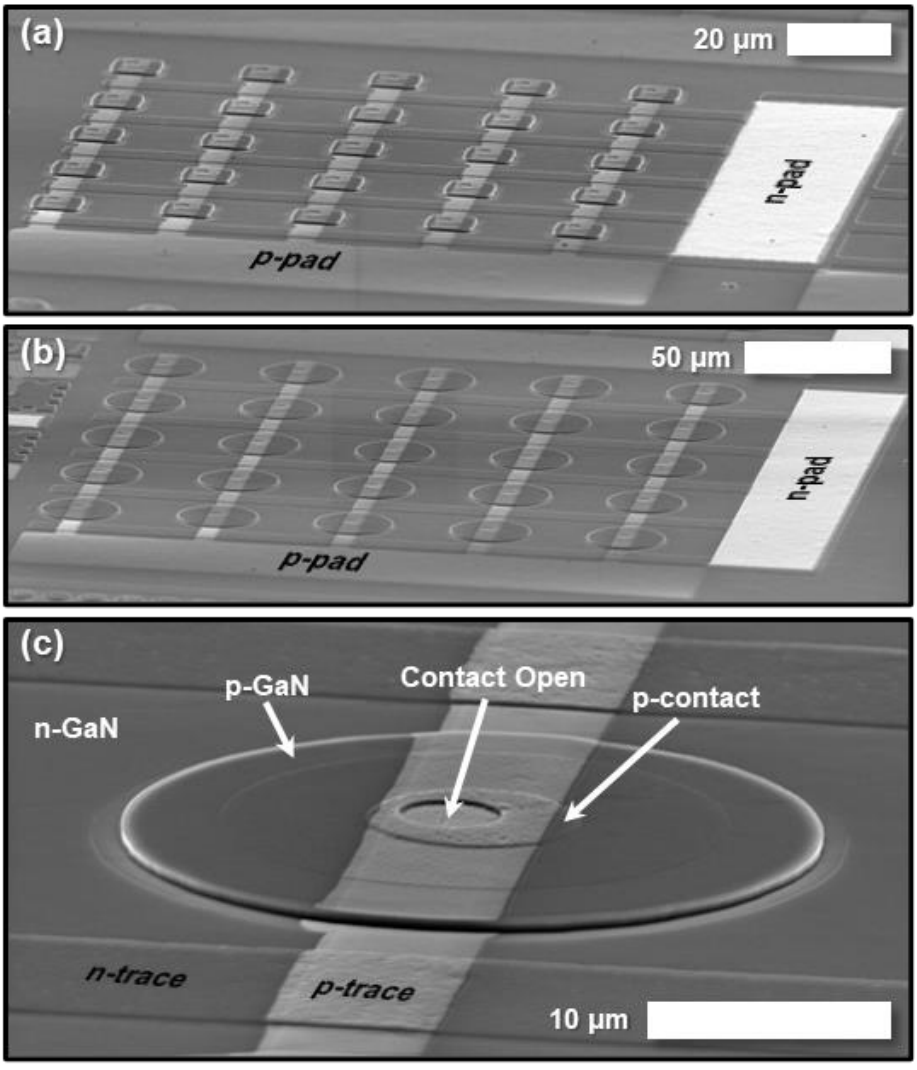

Figure 4.4.4: SEM images of completed 10 μm (a) and 30 μm (b, c) μLEDs. Images taken at 80° off normal. p- and n-pads are shown in (a, b) while p- and n-traces, nGaN/pGaN regions, and the locations of contact opens and p-contacts are shown in (c).

formation, p-traces were deposited, again using standard LOR5A/AZ1512 lithography and a 2.5 min develop. A 50 W O_2 descum was then performed, followed by a 30 second etch in 20% HCl. 100 nm of conformal Ni was then deposited via electron beam evaporation at a starting pressure of $3x10^{-6}$ torr and a deposition rate of ~2 Å/s. The sample was then left in NMP for 48 hours, which was sufficient to ensure complete liftoff of this thicker, high stress Ni layer without the need for ultrasonication. Figure 4.4.4 shows SEM images of completed devices taken at 80°, giving perspective on the relative thickness of each layer. Figure 4.4.5 shows optical images of completed devices. Minor misalignment can be seen in each image, as well as the overlap of the p- and n-traces, the location of the contact cut

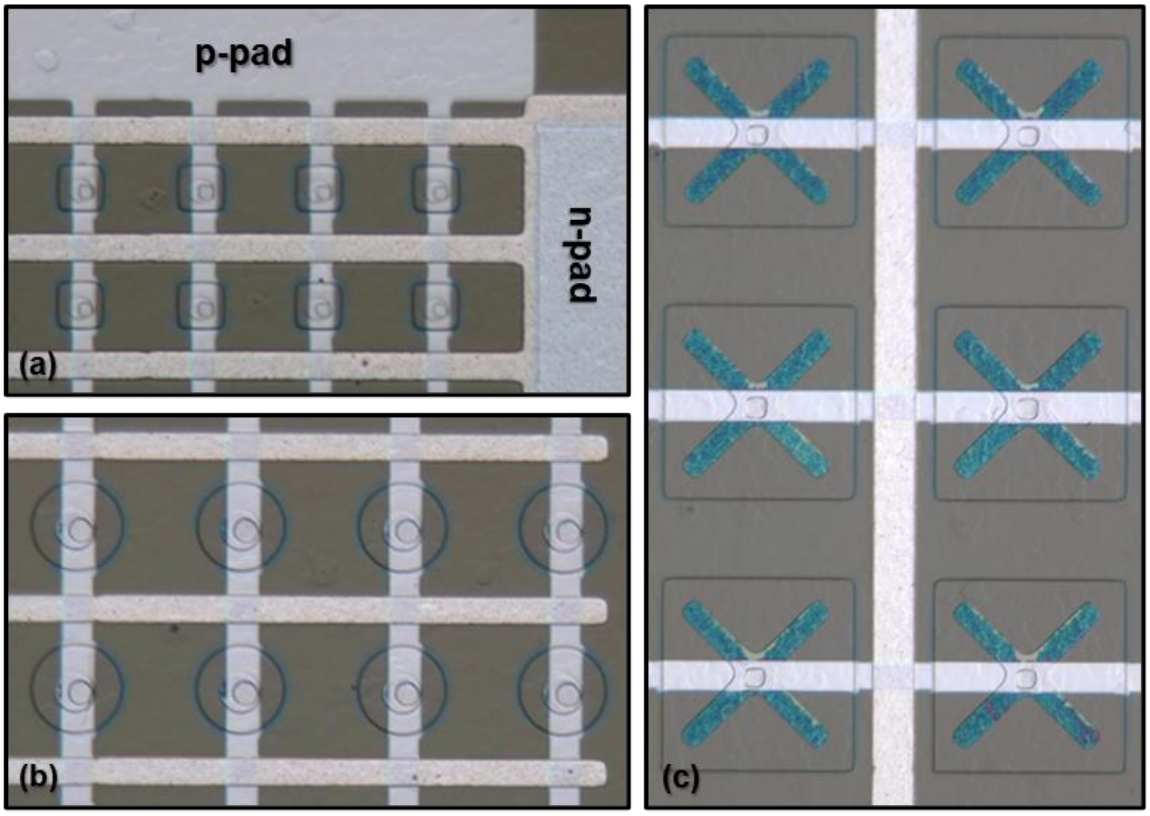

Figure 4.4.5: Optical images of 10 µm (a) 30 µm (b), and 50 µm (c) µLEDs. (a) shows the locations of the p- and n-contact pads as well as the location of the contact open over the n-pad. Discoloration of the annealed p-contact metal can be seen in (c).

over the n-pad, and the blueish discoloration of the p-contact metal (Figure 4.4.5(c)) due to formation of NiO compounds during the O_2 anneal.

4.4.3 Device Characterization

Completed devices were tested using a manual probe station and HP 4145 parameter analyzer. The sample was affixed with vacuum to the probe station stage and devices were addressed using W probe tips with diameters between 1 µm and 20 µm.

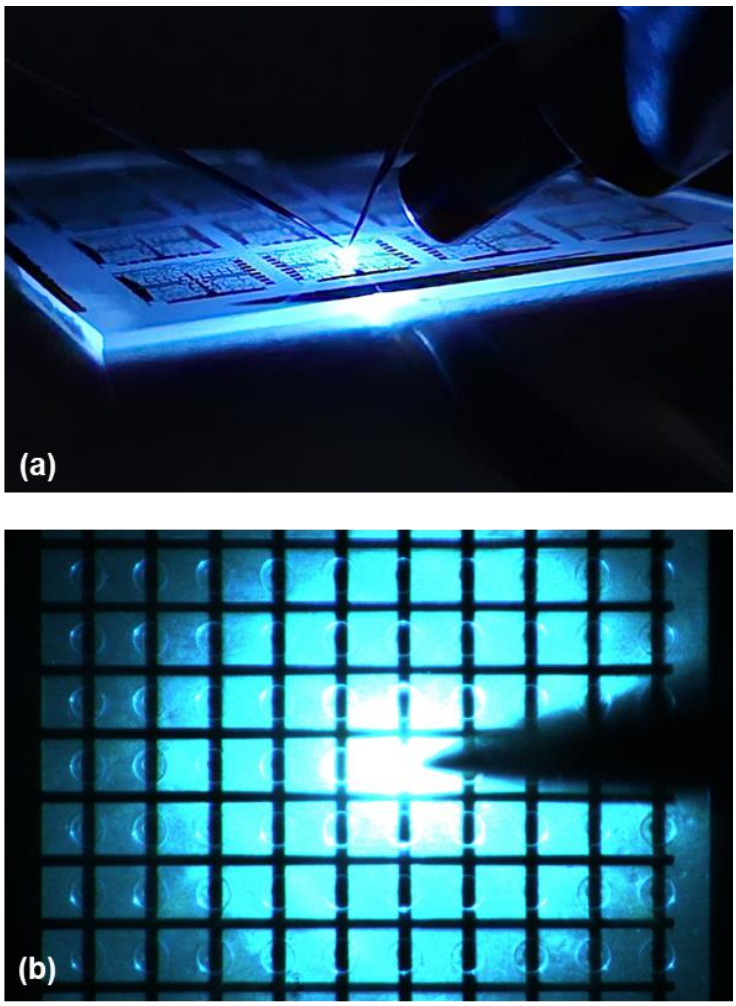

Figure 4.4.6: Illuminated 10 µm µLEDs imaged using a cell phone camera (a) and microscope camera (b). Despite narrowband emission occurring around 260 nm, cameras represent this emission as blue.

Images of the illuminated devices were captured using both a cell phone camera (Figure 4.4.6(a)) and a confocal microscope camera (Figure 4.4.6(b)). While the light emission shown in Figure 4.4.6 appears blue, it is important to note that this is due to how digital camera sensors capture and display ultraviolet light. While CMOS imaging sensors used in the majority of modern cameras are capable of recording the wavelength of detected photons, post processing of the image data displays this light as blue, since ultraviolet light is both invisible and harmful to the human eye (especially DUV light), and cannot be produced by display panels. While a small low energy tail was present in the emission of these μLEDs, allowing the illuminated devices to be viewed through 350 nm long pass laser goggles, the vast majority of light output power (LOP) was centered around 260 nm, as shown in Figure 4.4.7. Both images shown in Figure 4.4.6 were captured using a 50 ms exposure time. It is evident from Figure 4.4.6(a) that a significant amount of the emitted light is trapped within the sapphire substrate, as evidenced by the "glowing" sidewalls of the sample. This issue is more or less unavoidable in top emitting LEDs, and can be addressed using a bottom emitting configuration in which a reflective metal layer covers the entire surface of the fabricated device, forcing all light to be emitted through the substrate and improving light extraction efficiency. However, this approach was beyond the scope of our group's present capabilities as it requires more advanced packaging techniques.

While a number of large μLED arrays were fabricated in order to explore the feasibility of addressing numerous μLEDs in parallel, these devices did not perform well. When attempting to address 5x5 or 20x20 arrays of μLEDs through probing of the p- and n-pads (see Figure 4.4.5(a)), no more than a half dozen individual devices in the arrays

were able to be illuminated. This was due to several factors, likely including high resistivity of the relatively narrow p-traces and poor step coverage of the p-trace metal (100 nm Ni) over the mesa sidewall and contact open steps. As such, further attempts to characterize emission from µLED arrays were not pursued.

Figure 4.4.7 shows the electroluminescence (EL) spectra of 30 µm and 10 µm devices over a range of current densities. EL was measured by fixing an optical fiber connected to a spectrometer in close proximity (~2 mm) to the probed device at ~30° off-normal. The emissions peaks and linewidths of 30 µm and 10 µm devices were 264.3 nm/13.6 nm (at 300 A/cm^2) and 262 nm/7.1 nm (at 2000 A/cm^2) respectively. 10 µm devices were able to be driven at higher current densities than 30 µm devices due to their p-contacts covering a larger fraction of their mesa surface (18% vs 6%). The maximum current densities an LED (especially a DUV LED) can survive are almost always determined by the quality and size of the p-contact, and when failure occurs, the p-contact

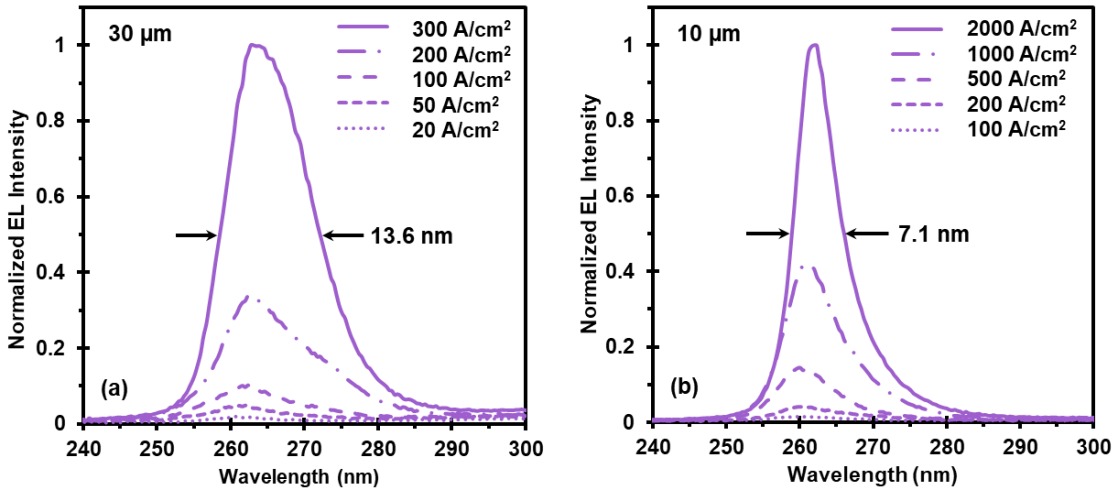

Figure 4.4.7: Normalized EL spectra for individual 30 µm (a) and 10 µm (b) µLEDs at various current densities. Emission peaks for 30 µm and 10 µm devices at their maximum measured current densities were located at 264.3 nm and 262 nm respectively. Emission linewidths at maximum measured current densities were 13.6 nm and 7.1 nm respectively.

is likewise almost always the point of failure. The moderately shorter emission wavelength of 10 µm devices at 2000 A/cm^2 when compared to 30 µm devices at 300 A/cm^2 can be attributed to the differences in current density. The much higher current densities achievable in the smaller devices due to increased coverage of their p-contacts leads to saturation of energy states (band filling) within their active regions, causing some electron hole pairs to recombine from higher energy states, leading to a minor blueshift in their emission wavelength. Interestingly, when current density is removed as a variable, as shown in Figure 4.4.8 which compares the emission of 30 µm and 10 µm devices at 200 A/cm^2, larger devices are actually found to emit at marginally shorter wavelengths. This is contrary to the behavior of visible light emitting µLEDs, in which smaller devices have been shown to have blueshifted emission [93]. Our results agree with other published works in which the size and emission wavelengths of DUV emitting µLEDs have been found to be inversely correlated to one another at a fixed current density [94,95]. One possible explanation for this may lie in the relative magnitudes of the strain induced

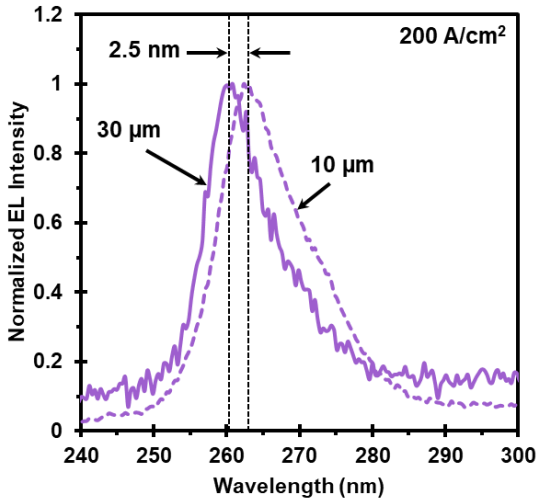

Figure 4.4.8: Normalized EL spectra for individual 30 µm and 10 µm µLEDs at 200 A/cm^2.

piezoelectric polarization fields in DUV and visible emitting epitaxies and the ways in which strain release through formation of μLED mesas affects band bending and the QCSE in the active region [93]. While the effects of current density on emission wavelength are well understood for both DUV (AlGaN) and visible (GaN/InGaN) emitting LEDs, current density independent variation in emission wavelength with device size has not been investigated as extensively. The lattice constants of AlN, GaN, and InN are 3.11 Å, 3.19 Å, and 3.54 Å respectively [96]. Of note is the much larger difference in lattice constant between GaN and AlN (-0.08 Å) than between GaN and InN (+0.35 Å). The long range (between the bulk epi and general active region) and short range (between the active region barrier and well layers) effects of strain on the active region band structure and very complex and are generally beyond the scope of this dissertation. However, it is likely that the smaller discrepancy between the AlN and GaN lattice constants (vs GaN and InN) are responsible for the reversal of emission shift in DUV emitting devices based on AlGaN (i.e. at DUV wavelengths, emission wavelength is inversely correlated to device size, whereas for visible wavelengths it is positively correlated to device size).

Current voltage characteristics are shown in Figure 4.4.9. Threshold voltages of 4.5 V and 6 V were measured for 30 μm and 10 μm devices respectively, with post threshold characteristics for all devices being largely dominated by series resistance due to the high resistivity of the p-AlGaN layer. The threshold voltage of the 10 μm device is higher due to its increased contact resistance, as has been shown in other works [97,98].

Measurements of light output power were performed using a Newport 843-R laser power meter. The 1 cm diameter detector was positioned ~ 1 cm from the probed devices,

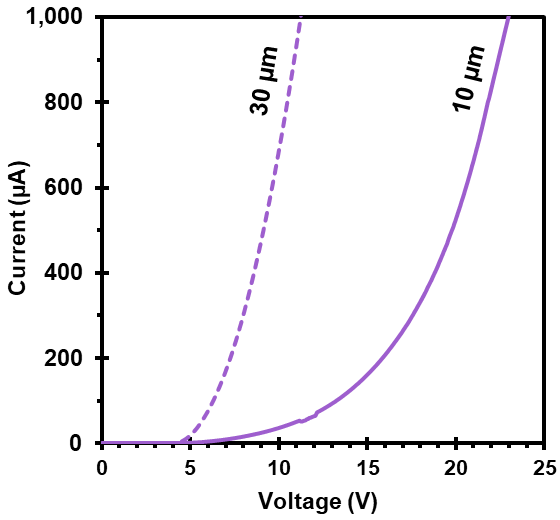

Figure 4.4.9: Current voltage characteristics for 30 μm and 10 μm μLEDs between 0 and 25 V.

and used to record the emitted light output power (LOP) as a function of current density. This test setup, while not optimal, allows for approximation of the total LOP of our μLEDs. The 1 cm detector located 1 cm from the emitting device, covered ~12.5% of the 1 cm radius hemisphere above the emitting LED. By dividing the measured LOP by 0.125 a

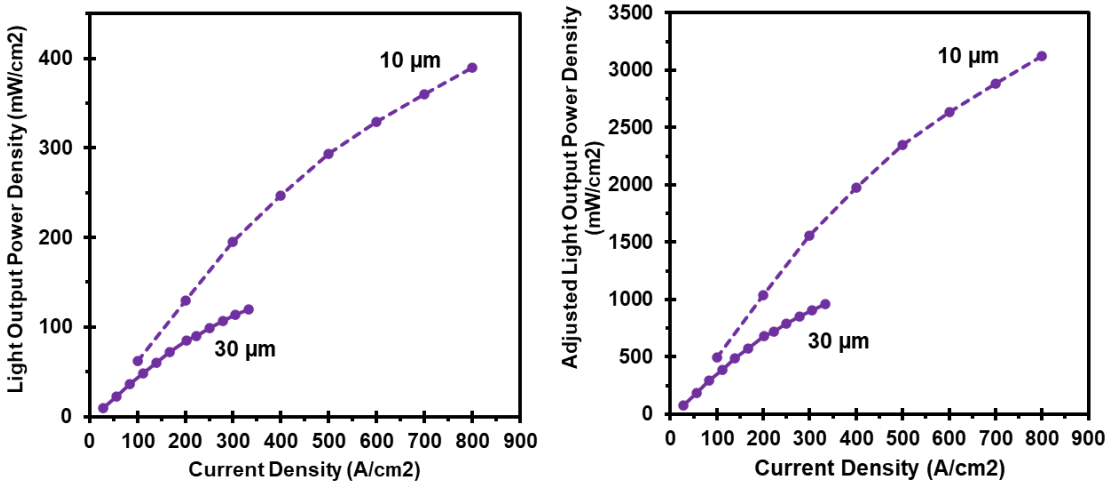

Figure 4.4.10: Measured (a) and adjusted (b) light output power as a function of current density for 10 μm (dashed) and 30 μm (solid) μLEDs.

reasonable "adjusted" upper bound for the total emitted LOP can be estimated. It is important to note that LED far field emission patterns are often quite complex, and light is almost never emitted with uniform intensity at all angles above the surface. As such, the true total LOP is likely somewhere between the measured and adjusted values shown in Figure 4.4.10. By accounting for the current and voltage supplied to the device from the parameter analyzer for each measured value of LOP, wall plug efficiency (WPE) can be estimated by dividing LOP by the product of I and V. Measured and adjusted WPE values are shown in Figure 4.4.11. While these values are not necessarily competitive with other reported results, which claim WPE and EQE values of up to 5% [98–100], the locations of efficiency droop onset are somewhat higher, at 200 A/cm^2 and 83 A/cm^2, than most reported results for similarly sized devices [94,98–101]. The relatively low WPEs of our devices can be attributed primarily to poor epitaxy and p-contact quality. As the growth of the epitaxy used to fabricate these devices was performed by a commercial vendor based

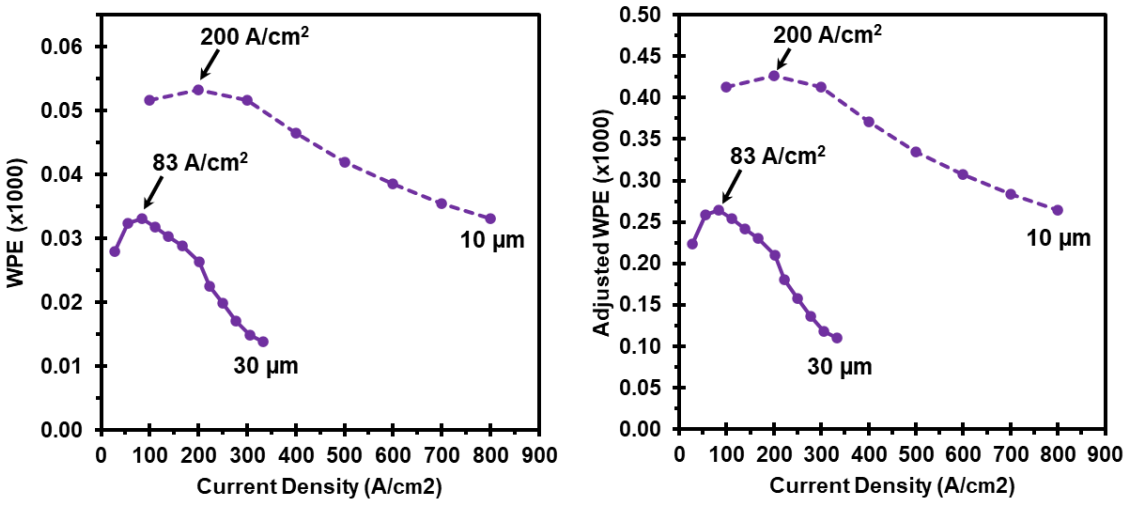

Figure 4.4.11: Measured (a) and adjusted (b) wall plug efficiency as a function of current density for 10 µm (dashed) and 30 µm (solid) µLEDs. The onset of efficiency droop was found to occur at 200 A/cm^2 for 10 µm devices and at 83 A/cm^2 for 30 µm devices. A WPE value of 1.0 is equal to 100% efficiency.

only on our provided specifications, we had little to no insight into the growth process. As evidenced by the surface roughness of the p-GaN shown in Figure 4.4.3(b), it is likely that the quality of the active region could be significantly improved through further optimization of the growth process and use of thicker (and more expensive) buffer layers. The p-contacts of our devices likely would have benefitted from being much larger and thicker, reducing contact resistance and allowing higher current densities to be driven through the devices. While this would come at the tradeoff of decreased η_{EXT} from the top of the µLED mesas, this would likely have little impact as the majority of emission occurs through the sidewalls in devices at this scale.

4.4.4 Conclusions

This study represents the first demonstration of fully functional, electrically driven DUV emitting µLEDs based on a novel AlGaN-delta-GaN active region. A six-band *k·p* model was used to optimize an $Al_{0.9}Ga_{0.1}N/Al_{0.75}Ga_{0.25}N$/delta-GaN MQW for emission at 265 nm, which was then grown by a commercial vendor. Devices were fabricated with dimensions of 10 µm and 30 µm in the RIT cleanroom. EL measurements showed emission at around 262 nm, with very narrow linewidths of between 7.1 and 13.6 nm. In contrast to InGaN/GaN visible emitting µLEDs, the larger 30 µm devices were found to emit at marginally shorter wavelengths than smaller 10 µm devices at a fixed current density, consistent with other results for DUV emitting µLEDs published in literature. While this phenomenon is not yet fully understood, it may be related to the way in which strain release through formation of µLED mesas affects band bending and the QCSE in the active region. A low turn on voltage of between 4.5 V and 6 V was determined, in line with other devices emitting at similar wavelengths. Power measurements performed using a laser power meter

showed LOP densities of between 100 and 1000 mW/cm^2 for 30 μm devices and 300 and 3000 mW/cm^2 for 10 μm devices. The higher obtainable output power densities measured for smaller devices is due primarily to higher fractional coverage of the mesa by the p-contact, which allowed for higher current densities in the smaller μLEDs. While the measured LOP densities are not necessarily comparable with the best performing devices reported in literature, there are several ways devices based on an AlGaN-delta-GaN active region could be significantly improved. These include further optimization of the growth process and use of thicker buffer layers to improve the quality of the active region, along with further optimization of the p-contact to allow for higher drive current densities. Wall plug efficiencies were calculated, revealed efficiency droop onset at 83 A/cm^2 and 200 A/cm^2 for 30 μm and 10 μm devices respectively, which moderately higher than most results reporting in literature for DUV emitting devices. These results represent an important first demonstration of AlGaN-delta-GaN based DUV emitting LEDs, and show that this active region design may be a viable alternative to existing AlGaN square well designs for high efficiency DUV emission.

4.5 Process Development for Future Micropillar/Nanowire Array LEDs

4.5.1 Introduction

Following the successful demonstration of μLEDs based on an AlGaN-delta-GaN active region, the next step is to demonstrate micropillar and/or nanowire array LEDs which leverage the high IQE of a AlGaN-delta-GaN active region alongside other key optimizations. As discussed in section 4.3, the inverse taper phenomenon which occurs in high Al-content AlGaN can be used to optimize the extraction efficiency of micro- and nano-structures. Additionally, as discussed in section 4.1, the PDMS interlayer dielectric previously using in our prior fabrication of nanowire array devices (see also section 5.2) was suboptimal for a number of reasons, necessitating a replacement which utilizes a PECVD deposited dielectric. By designing array-based devices around these three process optimizations, it should be possible to exceed the performance of the nanowire array LEDs discussed in section 4.1. In order to accomplish this, it is first necessary to develop a reliable process for planarizing the surface of conformally deposited PECVD dielectrics and studying the implementation of this process for use as an interlayer dielectric layer.

4.5.2 TEOS Planarization Process Development

As discussed in sections 3.7.2 and 4.1.2, a more robust interlayer dielectric such as SiO_2 or Si_3N_4 is ideal for fabrication of nanowire and micropillar array LEDs. When compared to the PDMS interlayer used in section 4.1.2, these materials offer improved repeatability, reliability, and structural rigidity. Tetraethyl-orthosilicate ($Si(OC_2H_5)_4$ (TEOS), a SiO_2 derivative, was chosen as it is the most reliable plasma deposited dielectric available in the RIT cleanroom. As with all PECVD dielectrics, TEOS deposits with a high

degree of conformality, which leads to significant surface topology on the surface of the overcoating dielectric layer which is not removed during the dielectric etch back process. This topology often manifests as “hills” over each nano/microstructure, with corresponding “valleys” between them. During the subsequent etch back used to expose the tip of the structures, this topology is preserved and can cause the dielectric layer to experience etch punch through at the bottom of the valleys, which will lead to shorting of the p-contact layer and the n-GaN/n-contact. Additionally, conformal dielectric deposition often also results in discontinuities in the dielectric surface, which increases the sheet resistance of the continuous p-contact and can even cause opens to form if the p-contact layer is too thin. As such, a method of planarizing the surface of conformally deposited PECVD TEOS had to be developed prior to utilizing it as an interlayer dielectric for micropillar arrays LEDs. The method we developed makes use of a sacrificial, self-planarizing photoresist layer and a modified fluorine TEOS dry etch which etches TEOS and photoresist at equal rates. By coating the planarizing photoresist over a topologically complex TEOS surface, the magnitude of surface features can be significantly reduced. The subsequent planarizing dry etch then removes the photoresist and the TEOS at equal rates, eroding the TEOS surface features as the photoresist is removed. This allows the surface feature height (h) of the TEOS surface to be reduced by orders of magnitude after only a few planarization cycles. As opposed to chemical mechanical planarization/polishing (CMP) (which is not available in the RIT cleanroom), which utilizes a combination of corrosive chemicals and mechanical abrasion to remove surface features [108,109], this technique can be used on samples of any size and shape, and can be performed in almost every research cleanroom with dielectric deposition and dry etching capability.

In order to develop this planarization method, samples were first prepared by dry etching a uniform array of micropillars on a 2-in GaN wafer. This was accomplished by first patterning an array of 2 µm squares on a 10 µm pitch using a liftoff process and a g-line stepper. Ni was deposited via electron beam evaporation to a thickness of 200 nm and lifted off in N-Methyl-2-pyrrolidone (NMP). The wafer was then dry etched to a depth of 2 µm at 75 W RF power, 350 W ICP power, 10 mtorr, and 32/8/5 sccms $Cl_2/BCl_3/Ar$.

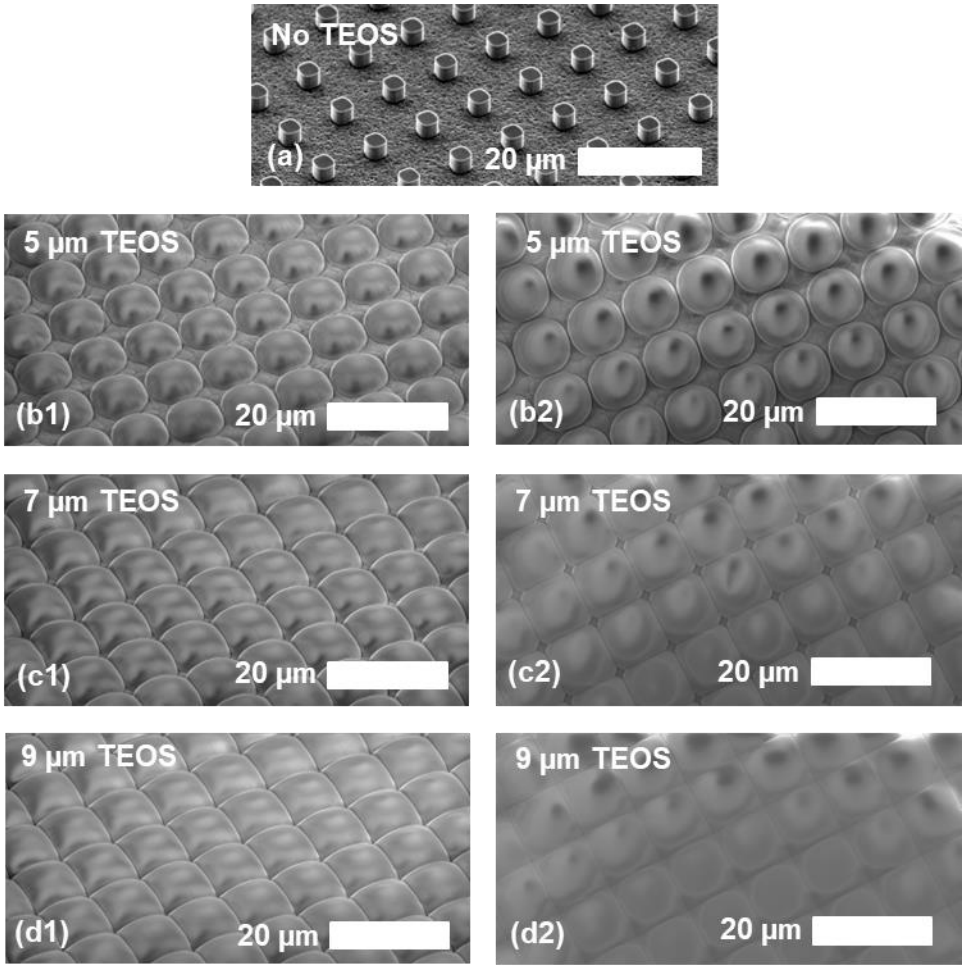

Figure 4.5.1: SEM images showing micropillars (2 µm diameter, 2 µm height, 10 µm pitch) following dry etching and KOH treatment (a), and subsequently after 5 µm (b), 7 µm (c), and 9 µm (d) of conformal TEOS deposition. Images a, b1, c1, and d1 where taken at 45° off normal, while b2, c2, and d2 were taken normal to the sample surface [104].

Following the dry etch, the wafer was etched in 40% AZ400K (a photoresist developer containing 2 wt% KOH) heated to 80°C for 20 min to remove dry etch damage and micromasking. The wafer was then coated with a protective photoresist layer and diced into 1 cm^2 samples. After the samples were removed from the dicing tape and cleaned in acetone to remove the protective photoresist layer, scanning electron microscope (SEM) images were taken of the finished micropillar arrays, as shown in Figure 4.5.1(a). TEOS was then deposited to thicknesses of 5 μm (Figure 4.5.1(a1, a2)), 7 μm (Figure 4.5.1(c1, c2)), and 9 μm (Figure 4.5.1(d1, d2)). Deposition thicknesses of 9 μm or more were found to fully "merge" the domelike S structures, seen best in Figure 4.5.1(b1, b2), reducing surface feature height. Samples with 9 μm of TEOS were characterized using SEM and atomic force microscopy (AFM) to determine surface feature height h, defined as the average of the lowest and highest points on the surface (shown in Figure 4.5.2(a)). For samples with 9 μm of TEOS, h was found to be ~ 1.6 μm, 400 nm less than the height of the underlying micropillars. To planarize the TEOS surface shown in Figure 4.5.1(d1, d2), AZ MiR 701 photoresist was first coated at 2500 rpm and baked for 3 min at 110°C. On a planar surface these coating parameters give a photoresist thickness of ~950 nm, and AFM measurements of the micropillar sample surface following resist coating show that h is reduced from 1.6 μm to around 200 nm. This indicates that photoresist layer does not planarize perfectly but still produces a large reduction in surface feature height. Figure 4.5.2(b) shows a cross-sectional representation of a perfectly planarized photoresist layer over a domed TEOS surface. A fluorine plasma etch was then used to etch back the photoresist and TEOS at equal rates (Figure 4.5.2(c)). This etch was carefully optimized from a standard TEOS dry etch to have both a high etch rate and 1:1 selectivity between

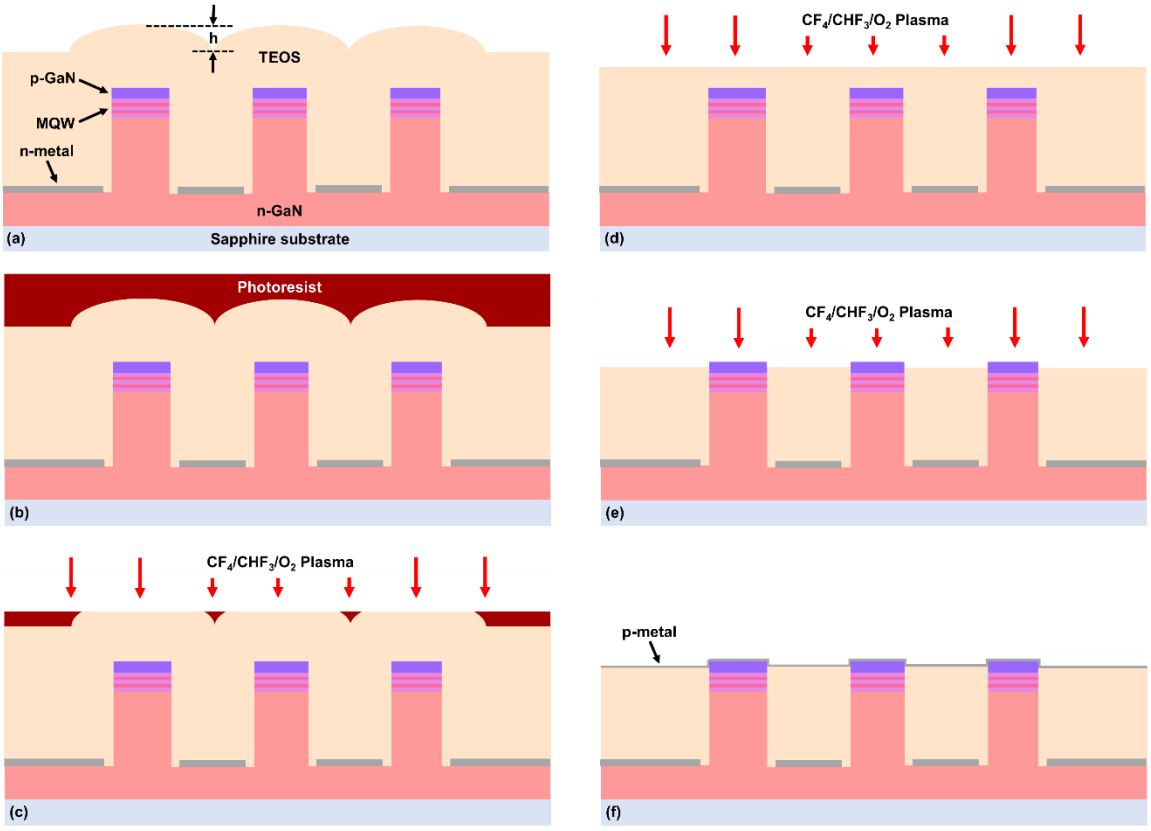

Figure 4.5.2: Cross sectional schematic showing the TEOS planarization process. (a) TEOS deposited over an array of micropillars, surface topology in the TEOS layer is evident. (b) Photoresist is coated over the TEOS surface and self-planarizes. (c) A fluorine plasma etch with 1:1 selectivity between photoresist and TEOS is used to etch back photoresist and TEOS at equal rates. (d) The now planarized TEOS surface is further etched back using any TEOS plasma etch. (e) The tips of the micropillars are exposed. (f) A conformal p-contact is deposited, connecting all micropillars in parallel, allowing for formation of a micropillar LED [104].

photoresist and TEOS. The etch was performed at 130 mtorr and 200 W RF power, with gas flow rates of 70/60/14 sccms $CHF_3/CF_4/O_2$.

At an etch rate of 100 ± 5 nm/min, this etch removed about 1 μm of photoresist and TEOS in approximately 10 min. It was found that extended continuous dry etching longer than 2 minutes led to roughening of the photoresist surface. This surface roughness

would then be transferred into the TEOS surface once all photoresist was removed. The development of this surface roughness is likely due to heating of the sample by the plasma over time. As the sample substrate is sapphire as opposed to Si, heating of the sample surface is always of concern during dry etching as sapphire is much less thermally conductive that Si and prevents heat from being easily removed through the Si carrier wafer underneath the sample. This issue was eliminated by breaking the planarization etch into shorter sub-etches, each with a duration of 1 min. Sub-etches were spaced by a 3-minute cooling step in which the same gas flows were maintained in the absence of plasma. In addition to fully preventing surface roughening of exposed photoresist, the use of multiple sub-etch steps also allows for more controllable etch rates, as sample heating can also affect the rates at which photoresist and TEOS etch, leading to a nonlinearity in a plot of etch depth vs etch time.

After all photoresist has been removed, leaving a (theoretically) planar surface as shown in Figure 4.5.2(d), any TEOS dry etch can then be used to further etch back the TEOS layer until the tips of micropillars are exposed, as shown in Figure 4.5.2(e). At this point, the planarization process has achieved its purpose of enabling the use of a conformally deposited TEOS layer as an interlayer dielectric, and a p-contact layer can be safely deposited to connect multiple micropillars in parallel. Without initial planarization to remove the surface topology of the as deposited TEOS, deep trenches with sharp discontinuities would exist in the interlayer dielectric, making formation of a continuous p-contact layer difficult and risking potential shorting of the n and p contacts in a worst-case scenario.

Creation of a non-selective dry etch was critical in the development of a process which could planarize a dielectric surface with significant topology. Fortunately, this is fairly straightforward to do by simply altering the O_2 flow rate of the etch. Oxygen plasma is used to ash wafers and is thus well suited for removing photoresist. Starting with a TEOS etch with a selectivity > 1, O_2 flow can be increased until a selectivity of 1 (or very close to 1) is achieved. Figure 4.5.3(a) shows a plot of selectivity vs O_2 for a standard TEOS dry

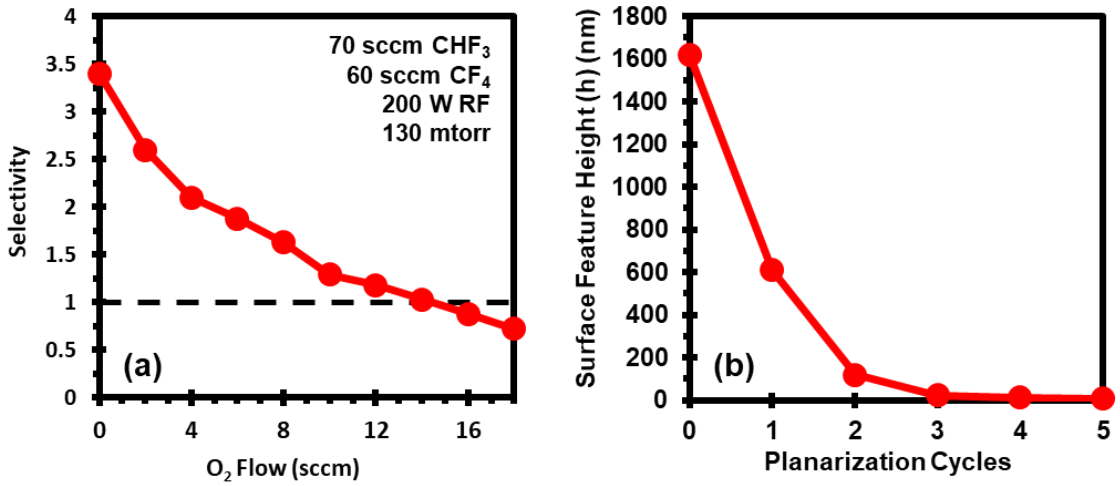

Figure 4.5.3: (a) Etch selectivity between photoresist and TEOS as a function of the O_2 flow rate in sccm. (b) Surface feature height h (see Figure 4.5.2(a)) as a function of the number of planarization cycles [104].

etch. This optimization process should be easily replicable in most facilities which have access to a etch tool plumbed with either CHF_3, CF_4, SF_6, or another fluorine gas, and O_2. The etch parameters necessary to achieve this non-selective etch will change depending on the etch tool, for example, the parameters shown in Figure 4.5.3(a) (130 mtorr, 200 W RF, 70/60/14 sccm $CHF_3/CF_4/O_2$) provided an etch selectivity of 1 ± 0.05 on our Trion Phantom III RIE, but on our Trion Minilock RIE (a similar but slightly older tool) only

11 sccms O_2 were required to achieve the same selectivity with all other parameters the same. As long as a photoresist masked TEOS dry etch with a selectivity > 1 can be achieved on a tool, this process should also be viable. As previously discussed, extended etches can cause unwanted roughening of the photoresist surface. Likewise, alteration of other etch parameters can also cause surface roughening of the resist. For example, increasing the RF power beyond a certain threshold will do this, as will an unbalanced ratio of fluorine gases. A roughened resist surface will manifest as clouding of the sample surface to the naked eye, and will be immediately evident in a microscope. In order to achieve an ideal planarization process, care should be taken to optimize the dry etch such that roughening does not occur.

We performed etch optimization using 2-inch Si wafers coated with TEOS. Photoresist was spin-coated on half the wafers, and then a pair of wafers (1 coated, 1 uncoated) were etched on a carrier wafer simultaneously. This process was repeated many times, changing the etch parameters each time, in order to determine etch rate and selectivity and to prevent roughening. TEOS and photoresist thickness were measured using a interferometer. Figure 4.5.4 shows SEM images of the TEOS surfaces with varying degrees of planarization. It is immediately evident that complete planarization of the surface shown in Figure 4.5.4(a) is not achieved in a single planarization cycle (Figure 4.5.4(b)). This is likely due to a combination of imperfect self-planarization of the overcoating photoresist layer (i.e. the photoresist surface is not perfectly planar and has a surface feature height of h ~ 200 nm) and preferential etching of photoresist in the vicinity of exposed TEOS, which causes spatial variation in the selectivity of the etch. Figure 4.5.3(b) shows surface feature height as a function of the number of planarization cycles

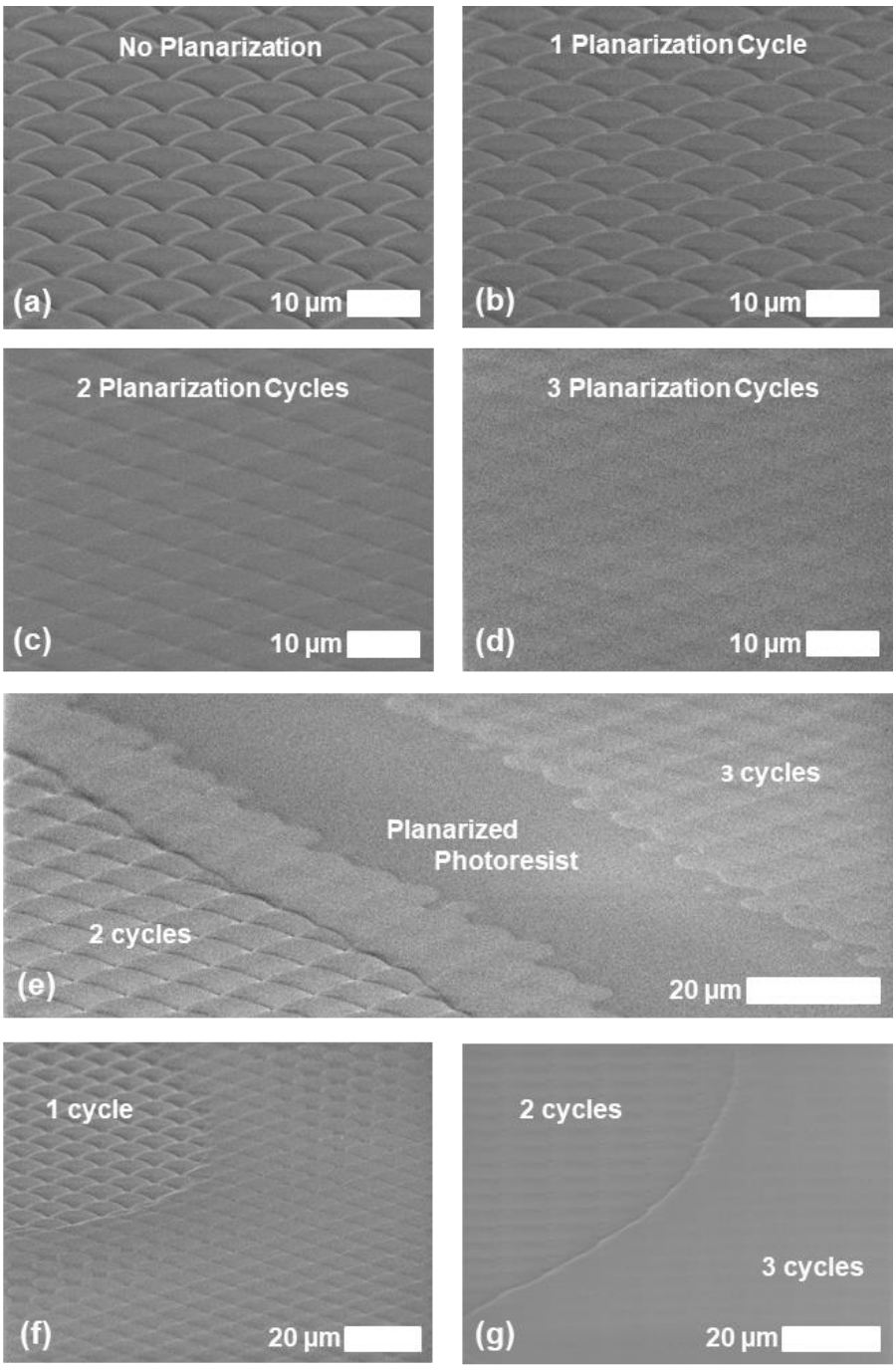

Figure 4.5.4: SEM images showing the TEOS surface after (a) no planarization, (b) 1 planarization cycle, (c) 2 planarization cycles, (d) and 3 planarization cycles. (e) Shows a region in which 2 and 3 cycles of planarization are visible, as well as residual photoresist between the two regions. Likewise (f) and (g) do the same for direct comparison of 1 and 2 cycles and 2 and 3 cycles respectively. All images were taken at 70° off normal [104].

performed. After a single cycle, h is reduced from 1.6 μm to around 600 nm. Additional cycles then reduce this to ~ 75 nm after 2 cycles (Figure 4.5.4(c)), and then to ~25 nm after 3 cycles (Figure 4.5.4(d)). At 5 planarization cycles (the maximum we performed), h was reduced to only 7 nm, however there is likely no realistic reason to perform more than 2 or 3 cycles due to diminishing returns. Figs. 4.5.4(e-g) were taken in defective regions on their respective samples, where photoresist failed to adhere to the TEOS surface. Fortunately, this allows for side-by-side comparison of regions which have received different number of planarization cycles. Figure 4.5.4(e) is perhaps the most interesting, showing regions planarized twice and thrice separated by a region in which photoresist is still present. Photoresist remains in this image because a thicker "edge bead" usually forms around the periphery of regions to which resist does not adhere, this leads to residual resist remaining even after it has all been removed in the thrice planarized region. Likewise, Figures 5.4.4(f) and 5.4.4(g) show the direct abutment of single and twice planarized regions and twice and thrice planarized regions respectively. Taken as a whole, Figure 5.4.4 gives an excellent qualitative depiction of the planarization process, showing the significant surface topology present in Figure 4.5.4(a) following TEOS dep can be more or less entirely removed after only three planarization cycles (Figure 4.5.4(d-e, g)).

4.5.3 Micropillar Array Fabrication Process Development

Following development of a suitable process for planarizing TEOS, micropillar arrays were fabricated from the same AlGaN-delta-GaN epitaxy used for the devices described in section 4.4. A cross-sectional representation of this epi-structure is shown in Figure 4.5.5. Following a solvent clean of the wafer, TEOS was deposited via PECVD to

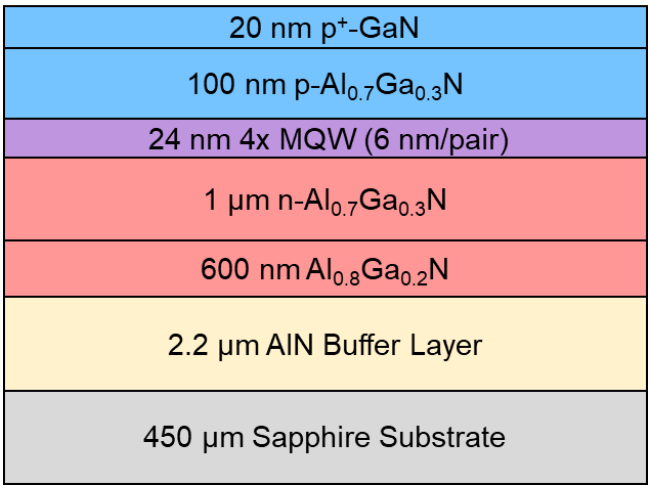

Figure 4.5.5: Cross-sectional representation of the AlGaN-delta-GaN epitaxy used during process development.

a thickness of 350 nm (Figure 4.5.5(a)). HMDS was applied to the TEOS surface and photoresist (LOR5A and AZ1512) was then coated onto the wafer surface and exposed using LDW. Following development of the resist, Ni is deposited via electron beam evaporation to a thickness of 70 nm to act as a dry etch mask (Figure 4.5.6(b)). The underlying TEOS is then etched using a standard TEOS etch with 200 W CCP RF power at 130 mtorr and gas flows of 60/70/6 sccms $CF_4/CHF_3/O_2$. At an etch rate of ~60 nm/min, nine 1-minute etch cycles were performed (an overetch of ~50%) to clear the TEOS. An ICP/CCP Cl based dry etch was then used to etch the underlying AlGaN-delta-GaN epistack. Etch parameters of 30 mtorr, 75/350 W CCP/ICP RF power, and 32/8/5 sccms Cl_2/BCl_3/Ar were used to achieve an etch rate of ~335 nm min. A total of 118 seconds of etching was used to hit the etch depth target of 660 nm, as measured by profilometer (Figure 4.5.6(c)). Following confirmation of the etch depth assuming negligible erosion of

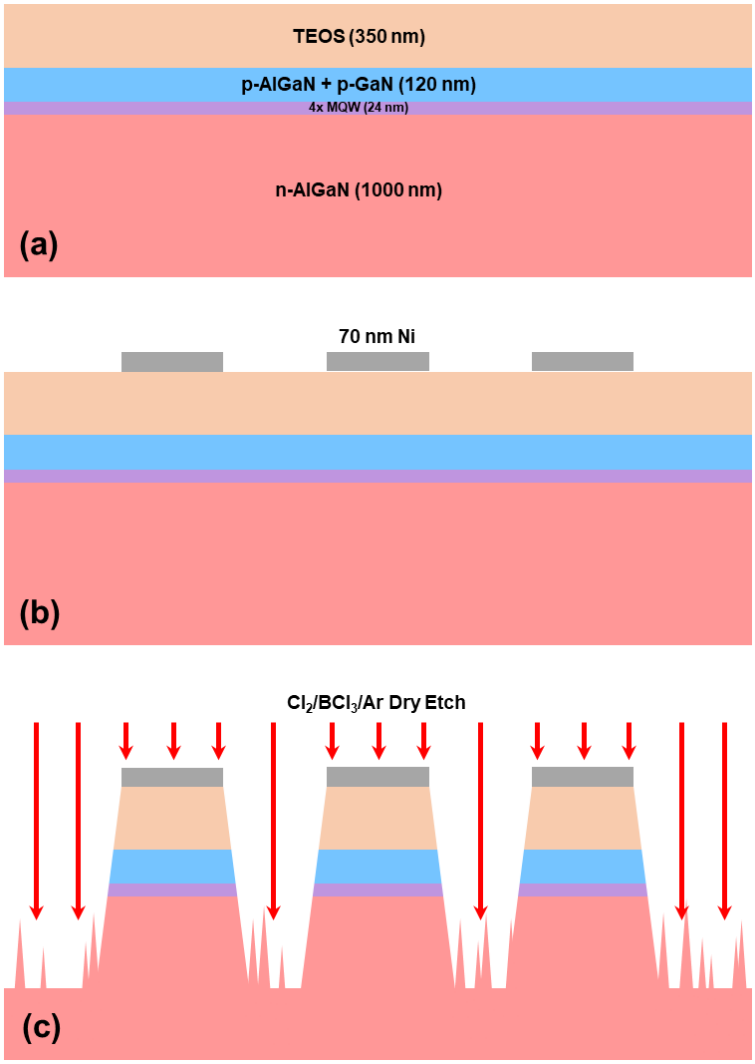

Figure 4.5.6(a-c): Deposition of 350 nm TEOS (a), patterning of 70 nm Ni (b), dry etching of the TEOS and underlying AlGaN epitaxy (c).

the Ni etch mask, the Ni etch mask was removed by etching the sample for 10 min in 25% HCl at 20°C (Figure 4.5.6(d)). The underlying TEOS layer was then removed using a 5 min etch in 10:1 BOE at 20°C (Figure 4.5.6(e)). A combined TEOS + Ni dry etch mask was used for two reasons. During extended Cl etching, Ni_xCl_y compounds will form on the surface of the Ni mask [102]. When thick enough, these compounds can prevent etching of the underlying Ni in HCl, making it nearly impossible to remove from the sample. The

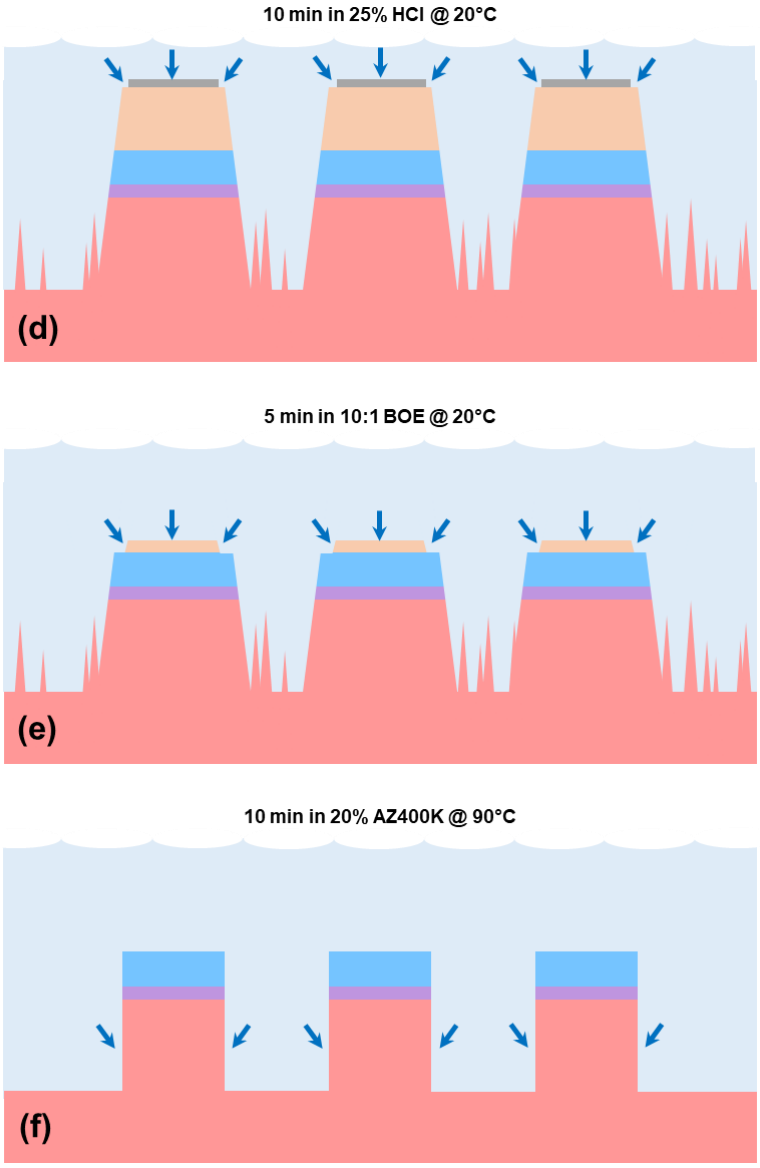

Figure 4.5.6(d-f): Wet etching of the Ni mask in 25% HCl (d), wet etching of the underlying TEOS in 10:1 BOE (e), etching of the AlGaN for 10 min in 20% AZ400K to remove etch grass and straighten sidewalls (f).

underlying TEOS layer allows the Ni etch mask to be removed regardless of Cl etch duration and the thickness of Ni_xCl_y on the Ni surface. Additionally, a TEOS only etch mask would require a clear field photoresist exposure to mask the TEOS etch. The LDW exposure tool we use has issues writing clear field patterns on transparent samples such as

AlGaN/GaN on sapphire, and as such, we are able to obtain much higher resolutions using dark field liftoff exposures. Following removal of the TEOS, the sample is etched in 20% AZ400K (0.4 wt% KOH) at 90°C to remove the micromasking present on the exposed

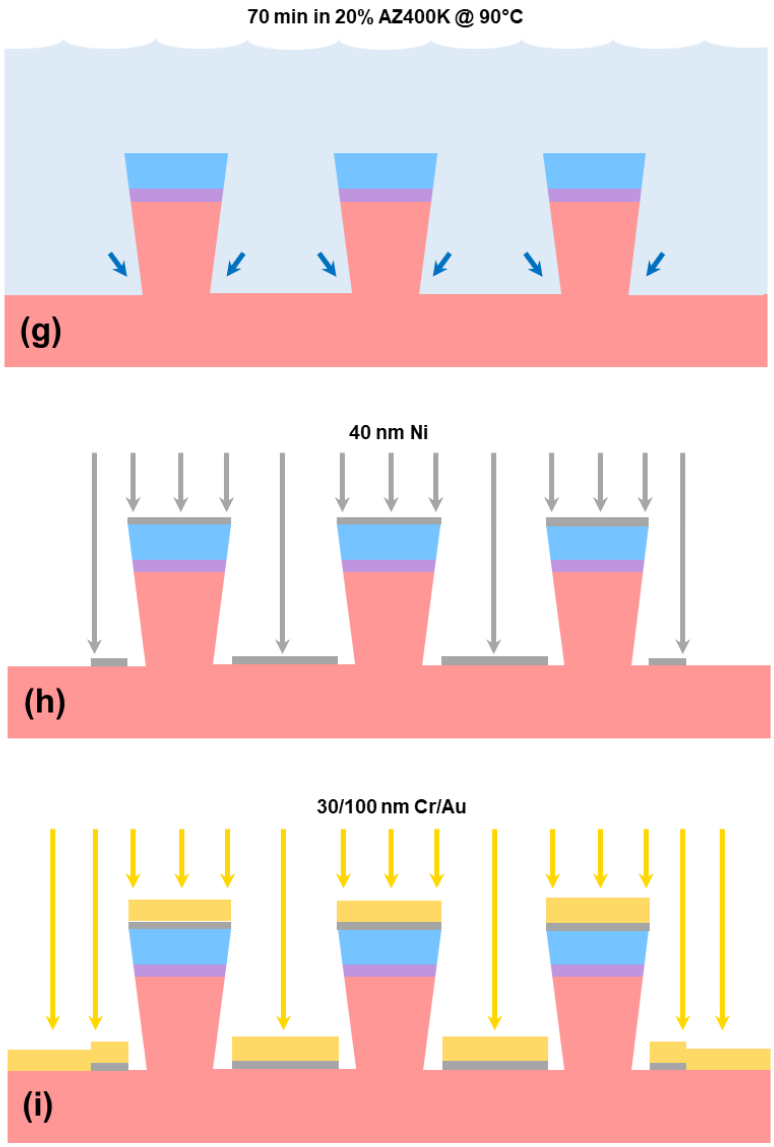

Figure 4.5.6(g-i): Extended wet etching of the AlGaN for 70 min in 20% AZ400K to produce an inverse taper sidewall profile (g), deposition of 40 nm Ni on top of the micropillars followed by annealing in O_2 at 550°C to form an ohmic p-contact (h), deposition of 30/100 nm Cr/Au to form an unannealed ohmic n-contact to the n-AlGaN (i).

n-AlGaN surface and modify the geometry of the micropillar sidewalls. After 10 min of etching in this solution all micromasking is removed and vertical sidewalls are obtained, as shown in Figure 4.5.6(f). A further 60 minutes of etching (70 min total) is performed to produce the inverse taper profile described previously in sections 4.1 and 4.2, as shown in Figure 4.5.6(g).

Once the micropillars are formed, LOR5A and AZ1512 are coated and exposed, and 40 nm of Ni is selectively deposited over the arrays via directional electron beam evaporation to serve as the p-contact (Figure 4.5.6(h)). The inverse taper of the micropillars prevents sidewall deposition entirely. The Ni is then annealed for 2 minutes in O_2 at 550°C to reduce its contact resistance and form an ohmic p-contact to the tops of the micropillars. LOR5A and AZ1512 are again coated and exposed, and 30/100 nm of Cr/Au is deposited to act as the n-contact in the field regions arounds the arrays (Figure 4.5.6(i)). This Cr/Au layer is also deposited over the arrays themselves to form a thicker metal stack on the tops of the micropillars. While this will prohibit emission of light from the tops of the micropillars, it allows much more room for error during the TEOS etchback process which would normally have to terminate within the very thin 120 nm p-GaN/p-AlGaN region to avoid shorting the MQW. Cr/Au provides an ohmic contact without the need for annealing, unlike Ti/Al, which prevents degradation of the previously annealed p-contact during N_2 n-contact annealing.

Following formation of the p- and n-contacts, TEOS is deposited conformally to a thickness of 2 μm via PECVD, as shown in Figure 4.5.6(j). The TEOS (or other dielectric) thickness required for an interlayer dielectric is determined by the height of the underlying micro/nanostructures, and to a lesser degree the size and pitch of these structures. In

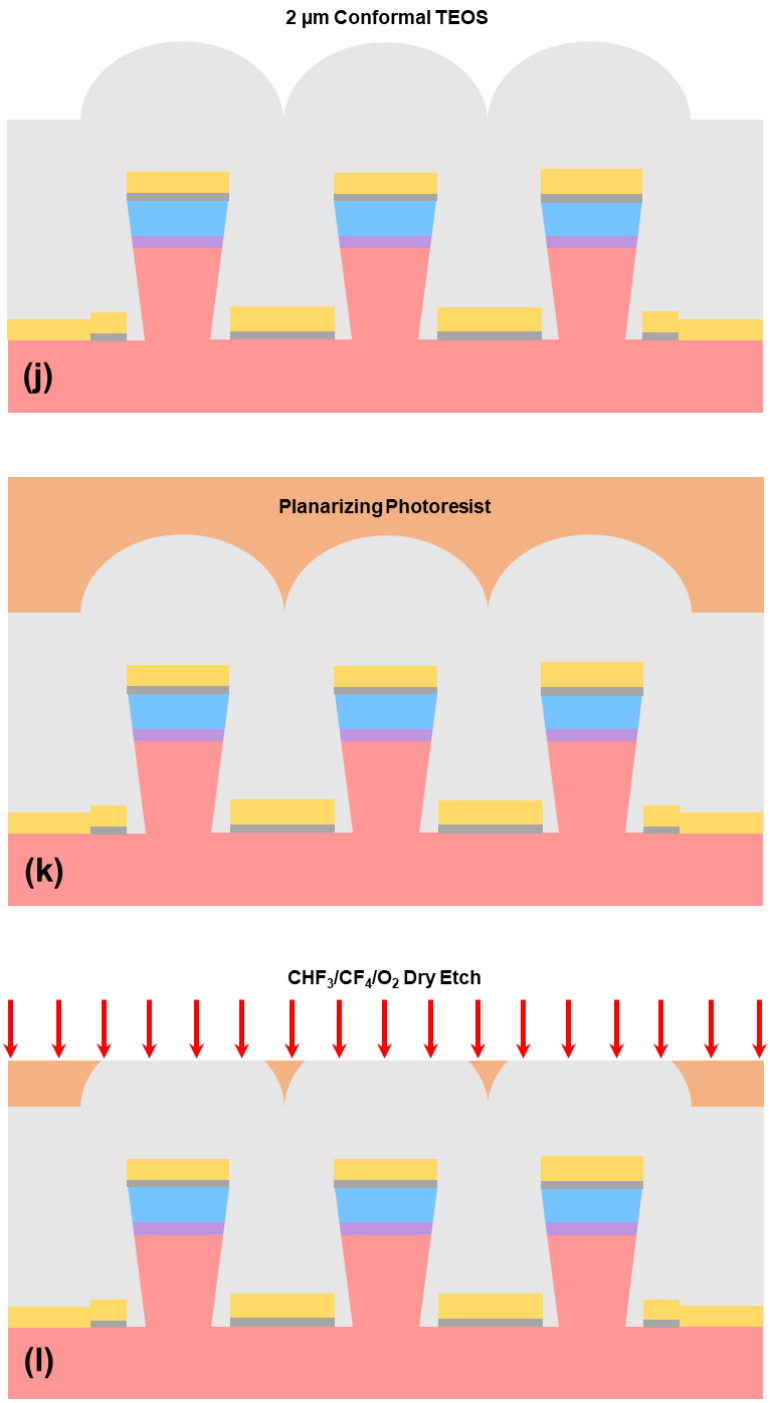

Figure 4.5.6(j-l): PECVD deposition of 2 µm of conformal TEOS (j), coating of a semi-self-planarizing photoresist layer onto the TEOS surface (k), planarization of the TEOS surface using a F dry etch (l).

general, the deposited thickness must be greater than the height of the surface structures in order to ensure that dielectric will remain in the field regions once the tips of the structures are exposed via etchback. The TEOS planarization process development described in section 4.5.2 was performed on a uniform array of structures, however, when arrays of different size structures with varying pitch are present on the same sample, this planarization process becomes more complex. The topology of the TEOS surface above arrays of nano/microstructures depends primarily on the spacing between these structures. If the space between structures is less than 2x the deposited dielectric thickness, the dielectric will merge between adjacent structures. If the space between structures is greater than 2x the dielectric thickness, a gap will remain following dielectric deposition. The presence of both these types of structures (those with merged and unmerged dielectric) on the same sample can complicate the planarization and etchback process, as will be described later in this section.

Following deposition of 2 μm conformal TEOS, photoresist (AZ1512 in this case) is coated over the sample at a spin speed of 3000 rpm. The surface of this resist layer self-planarizes as shown in Figure 4.5.6(k). A $CHF_3/CF_4/O_2$ dry etch tuned (as described in section 4.5.2) to etch the photoresist and underlying TEOS at the same rate is then used to remove the photoresist layer along with the peaks of the most prominent TEOS features as shown in Figure 4.5.6(l). In an ideal scenario, the photoresist would perfectly self-planarize over the entire sample as shown in Figure 4.5.6(l), however in reality this is not the case. Instead, the resist will undergo “short-range” planarization, meaning that it will planarize over the surfaces of individual, tightly packed (small pitch) arrays, but will not undergo “long-range” planarization between arrays and sparsely packed (large pitch)

arrays. This leads to the resist coating to its default thickness in the field regions, and thinner over arrays. As such, it is not possible to planarize the entire surface of the sample in a single photoresist coat and etch step, so several planarization "cycles" must be used,

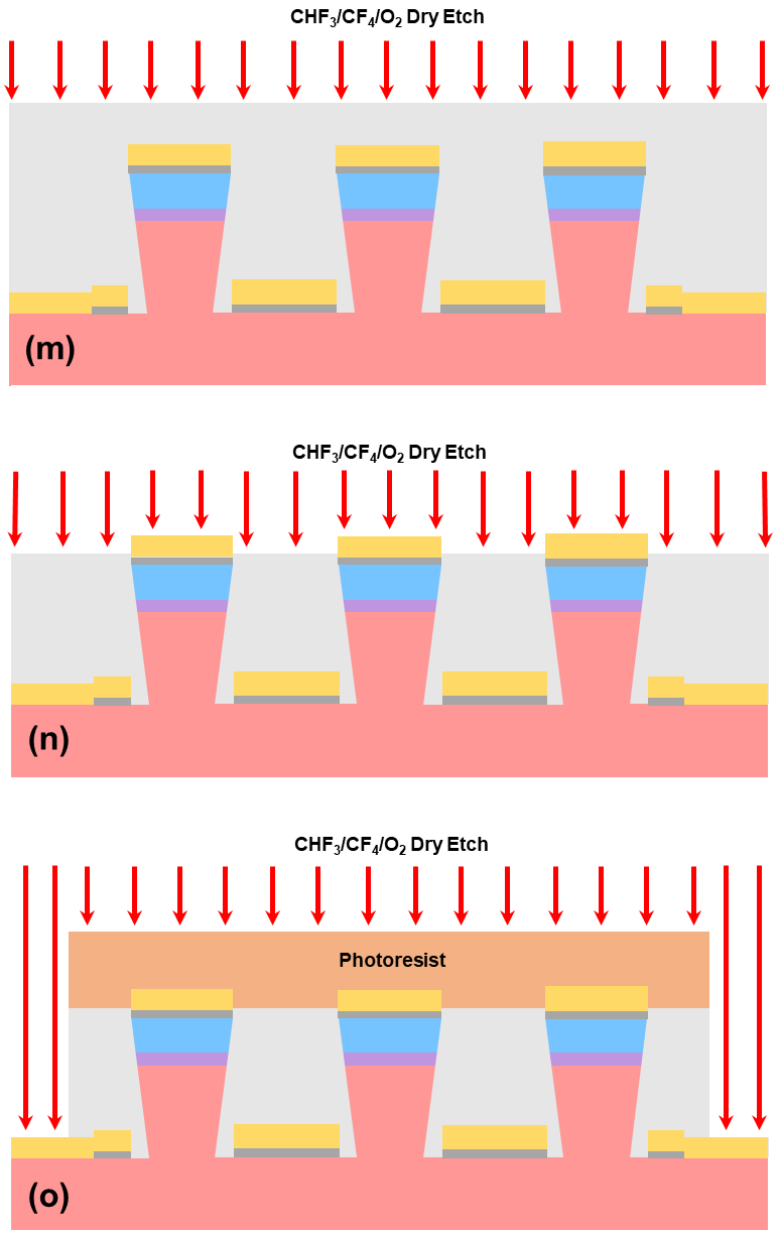

Figure 4.5.6(m-o): Etchback of the planarized TEOS surface (m), exposure of the micropillars (n), etching of the field TEOS to expose the n-contact (o).

with each cycle consisting of photoresist coating and enough dry etching to remove the entirety of the resist layer across the entire sample. In this case, 4 planarization cycles were completed in order to achieve sufficient planarization of all array variants present on the sample, whose individual elements ranged from 600 nm to 5 µm in diameter (D) with pitches of either 2D or 3D. Arrays were formed of either 20x20 or 50x50 elements. After the TEOS surface is sufficiently planarized, it can be etched back using a F plasma to expose the tips of the buried micropillars, as shown in Figures 4.5.6(m-n). In this case a standard TEOS etch with 200 W CCP RF power at 130 mtorr and gas flows of 60/70/6 sccms $CF_4/CHF_3/O_2$ was used to etch back the TEOS at a rate of ~60 nm/min.

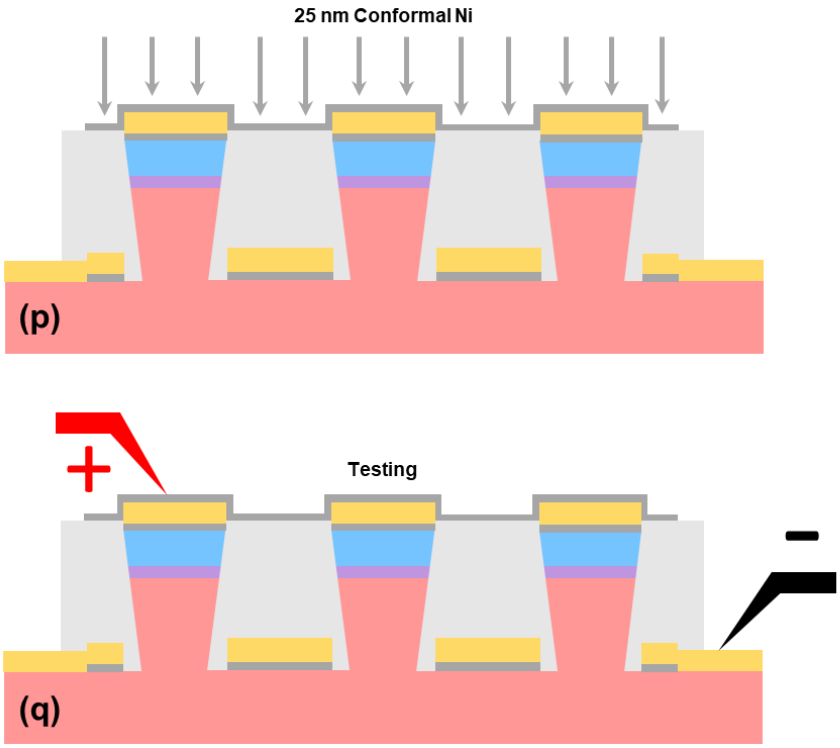

Figure 4.5.6(p-q): Conformal deposition of Ni to form to connect each array of micropillars in parallel (p), testing of a completed device (q).

Following completion of the etchback, photoresist (AZ1512) is coated and exposed to mask a dry etch of the field TEOS to expose the n-contacts (Figure 4.5.6(o)). LOR5A and AZ1512 are then coated, exposed, and developed, and 25 nm of conformal Ni is deposited to connect all the structures in an array in parallel, as shown in Figure 4.5.6(p). At this point individual devices are ready for testing, which is performed by applying a positive bias to the Ni p-contact or a negative bias to the Cr/Au n-contact as shown in Figure 4.5.6(q).

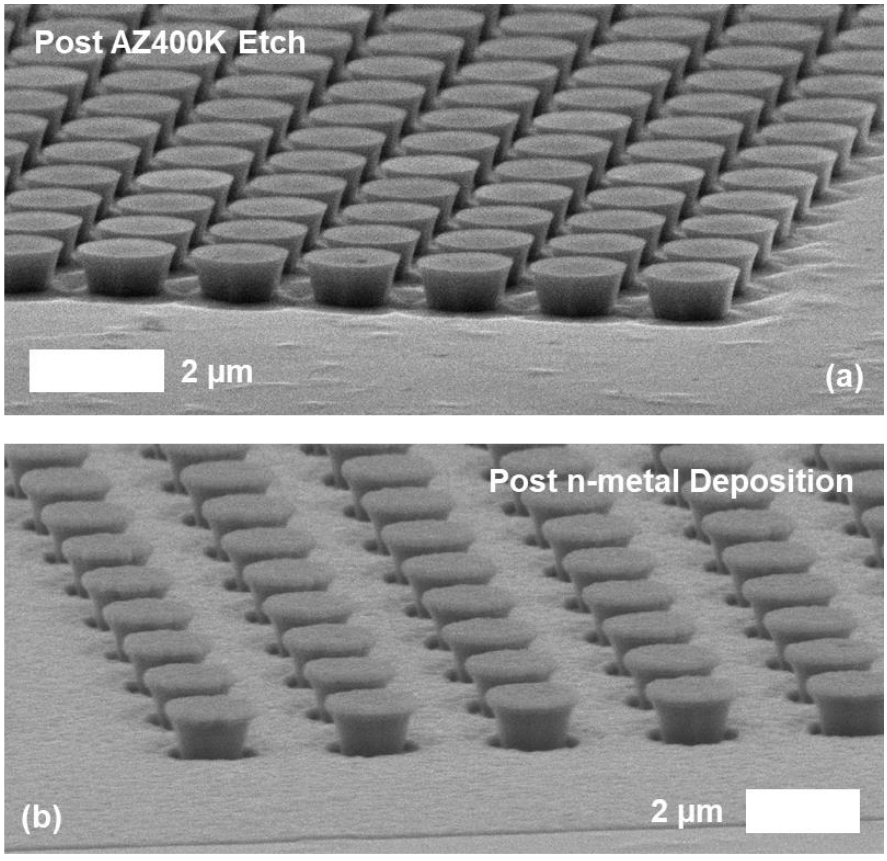

Figure 4.5.7: SEM images of 1.5 µm micropillars on a 2 µm pitch following AZ400K etching (a), and 1.25 µm micropillars on a 2.5 µm pitch following deposition of the 40 nm Ni p-contact and 30/100 nm Cr/Au n-contact (b).

Figure 4.5.7 shows SEM images of arrays of micropillars before and after deposition of the p- and n-contact metals. The inverse taper created by the AZ400K etch is easily visible in both (a) and (b), while the metal shadowing is evident in (b). The diameters/pitches of the micropillars shown in Figure 4.5.7(a) and (b) are 1.5/2 μm and 1.25/2.5 μm respectively. Likewise, Figure 4.5.8 shows a full 20x20 array of 1.25 μm micropillars on a 2.5 μm pitch. In this image, the entire visible region is covered in Cr/Au, with the darker box surrounding the array delineating the region in which 40 nm of

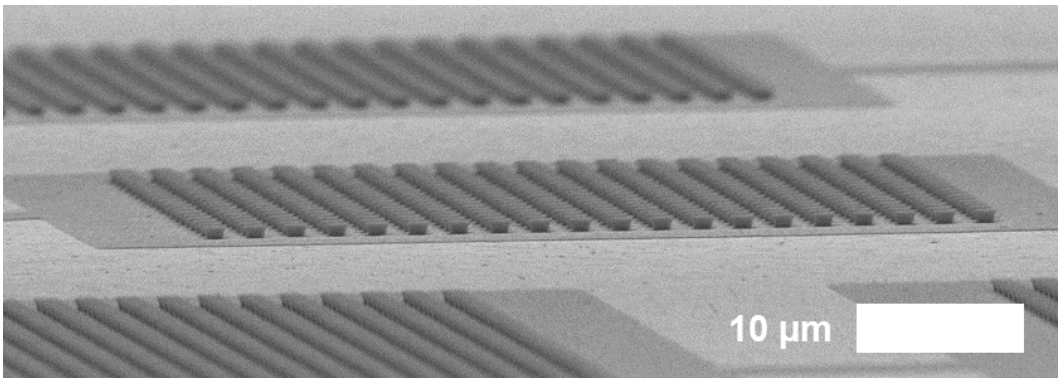

Figure 4.5.8: SEM images of a 20x20 array of 1.25 μm micropillars on a 2.5 μm pitch following n-metal deposition.

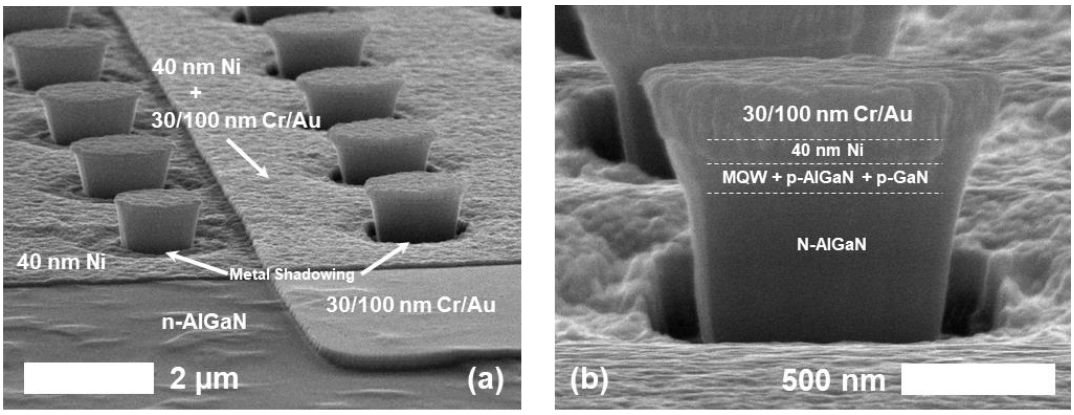

Figure 4.5.9: SEM images showing the intersection between regions of exposed n-AlGaN, annealed Ni, and Cr/Au on annealed Ni (a), and a near cross sectional view of an 800 nm micropillar covered with 40 nm Ni and 30/100 nm Cr/Au (b).

annealed Ni is present under the Cr/Au layer. Figure 4.5.9(a) shows an area in which regions of n-AlGaN, annealed Ni, and Cr/Au on annealed Ni intersect, highlighting several interesting phenomena. First, the etched n-AlGaN surface has inherited the roughness of the p-GaN surface noted in section 4.4.2, indicating that epitaxy is of relatively poor quality. Second, the surface of the annealed Ni layer is quite rough when compared to the unannealed Cr/Au layer. This is generally expected due to densification of the as-deposited Ni and formation of NiO compounds during annealing. Figure 4.5.9(b) shows a higher magnification image of a single 800 nm micropillar at ~85° off normal. The interfaces between the Cr/Au, Ni, p-GaN/p-AlGaN/MQW, and n-AlGaN regions are indicated by dashed lines, and the metal shadowing caused by the inverse taper profile is clearly visible. The distortion which can be seen in Figure 4.5.9(b) is caused by charging.

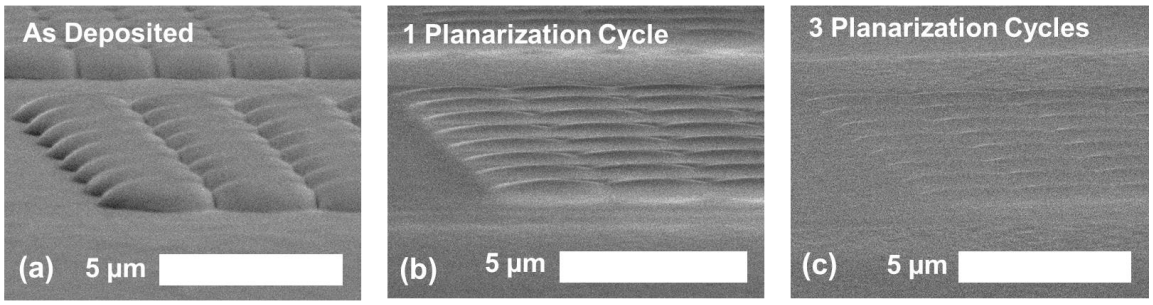

Figure 4.5.10: SEM images showing the TEOS surface over the same micropillar array as deposited (a), and after 1 (b) and 3 (c) planarization cycles.

As previously described, a number of planarization cycles are almost always needed to achieve sufficient planarization over an array of micropillars or other structures. This is clearly illustrated by Figure 4.5.10, which shows the same micropillar array following TEOS deposition (a), and after one (b) and three (c) planarization cycles. The significant surface topology, with roughly the same height as that of the underlying

micropillars (~660 nm), is reduced significantly by a single planarization cycle, and is almost completely removed after three planarization cycles. In Figure 4.5.10(c), surface feature height has been reduced to roughly 50 nm, and ~1000 nm of TEOS is left above the tops of the buried micropillars. This shows the effectiveness of this planarization process even for isolated arrays, despite the need to perform it several times to achieve suitable levels of planarization. The etchback process which follows planarization is shown in Figure 4.5.11. As the TEOS is etched back from a thickness of roughly 1000 nm, the underlying micropillars first appears as dark spots on the TEOS surface as shown in Figure 4.5.11(a). This is due to the underlying pillars and their metal caps acting as charge sinks, drawing the negative charge which accumulates on the insulating TEOS surface during bombardment by the electron beam down into the substrate. As the etchback progresses and micropillars come closer to clearing, the Au on their surfaces enters the penetration depth of the electron beam and the formerly dark spots above the pillars become brighter regions to the increased secondary electron emission by the Au, as can be seen in Figure 4.5.11(b). At 1000 nm of etchback, many of the micropillar arrays are very close to clearing. After 1500 nm of etchback, as shown in Figure 4.5.11(c), most micropillars are cleared, and many are "over cleared," meaning that the MQW region is exposed and will be shorted following deposition of a conformal connecting metal on top of the TEOS.

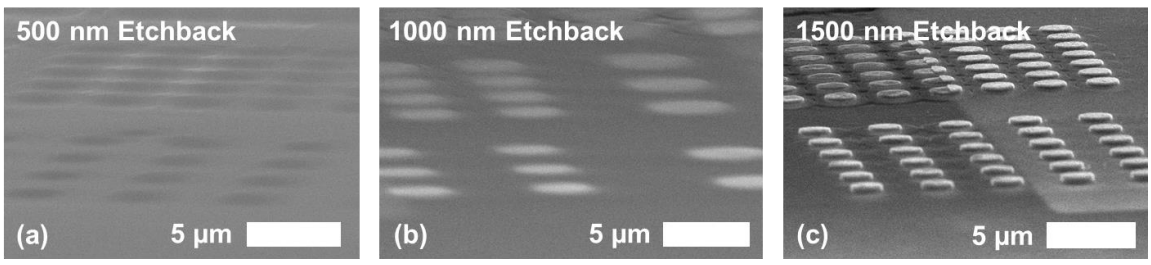

Figure 4.5.11: SEM images showing the TEOS surface over micropillar arrays following 500 nm etchback (a), 1000 nm etchback (b), and 1500 nm etchback (c).

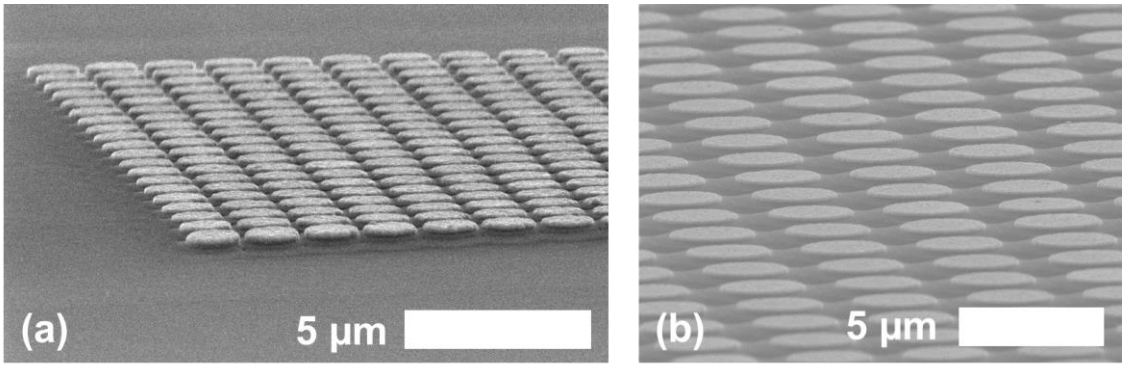

Figure 4.5.12: SEM images showing the Cr/Au covered surfaces of micropillars following successful etchback of the TEOS.

Most arrays required between 1100 and 1300 nm of etchback to properly expose the underlying micropillars, as can be seen in Figure 4.5.12, while denser arrays took more than 1500 nm of etchback to fully clear. As previously described, this is due to the planarizing resist coating thicker over denser arrays, results in less etching of the underlying TEOS during the planarization process. As a consequence, it was found that denser arrays required more etchback to fully clear when compared to sparse arrays. Figure 4.5.13 shows SEM images of dense arrays in which the micropillars at the corners of the arrays cleared long before those in the center. Figure 4.5.13(a) shows an SEM image of a partially cleared array. The center of the array appears much darker due to remaining, uncleared TEOS. This effect is also shown in Figures 4.5.13(b) and (c) at higher magnification. The primary reason for early clearing of the array corners is the way in which photoresist planarizes over denser arrays. When resist is coated, it coats to its default thickness in the field regions, and coats thinner over the elevated arrays, as expected. However, the resist coats thinnest at the edges of the arrays at the transition between the array and the field region. As such, where 1 µm of resist might exist in the field region and

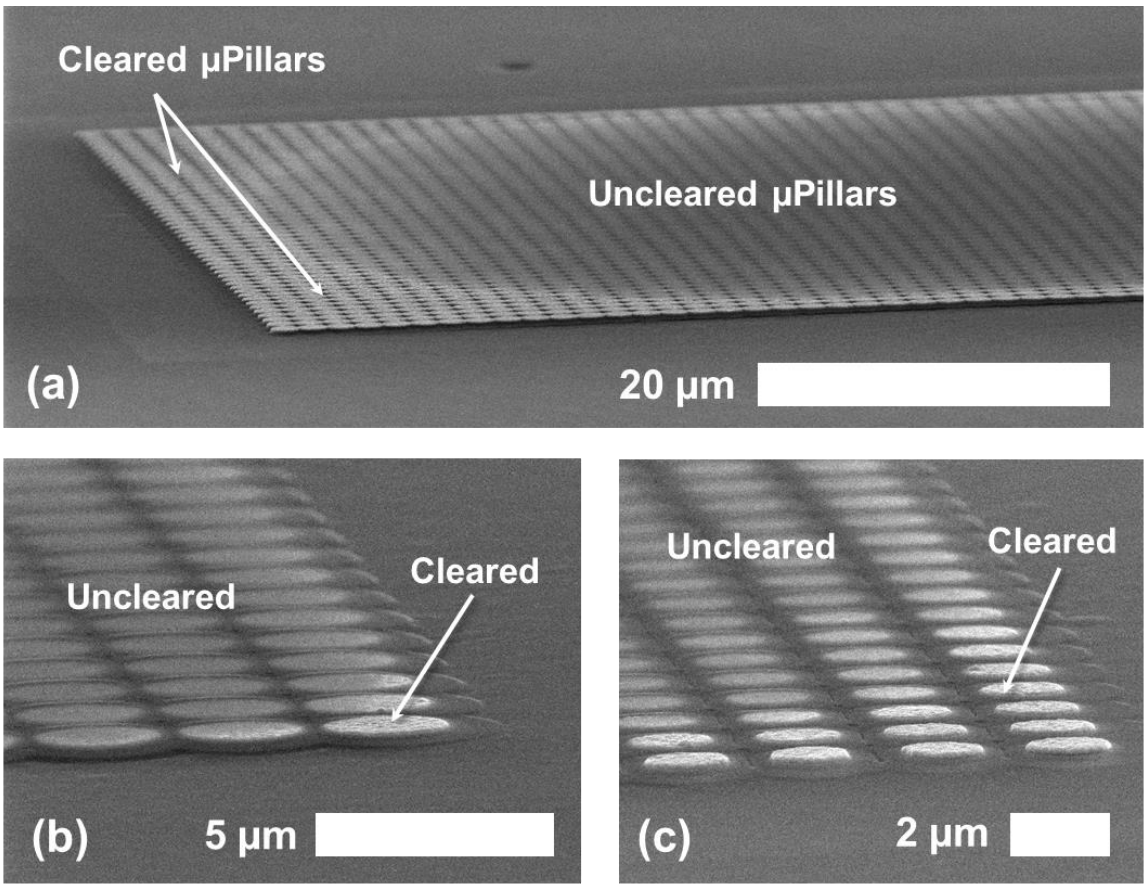

Figure 4.5.13: SEM images highlighting the issues which can occurs during planarization of TEOS over isolated arrays of micropillars. (a) shows a large, dense array in which the corner regions have cleared to expose the Cr/Au on the micropillars, while the center of the array remains covered in TEOS. Likewise (b) and (c) show close up images of the corner regions of similar arrays.

750 nm over of the center of an array, only 500 nm might exist at the edges of the array, with the corners having even less resist. During the planarization process, the resist is completely removed earlier at the corners and edges of an array than in the center, resulting in the TEOS in these regions experiencing more etching during planarization than the TEOS toward the center of the arrays. The thinner TEOS in these regions thus clears faster during the etchback process, leading to the issue illustrated in Figure 4.5.13. In order to fully clear the micropillars in the center of these arrays, additional etchback must be

performed which can potentially lead to “over clearing” at the edges and corners of the array. An array with over cleared elements risks shorting of these over cleared elements once the conformal connecting metal is deposited. There are several ways to address this issue, the simplest being to simply fabricate devices of reduced size as shown in Figure 4.5.14. This is done by simply reducing the size of the connecting metal pad atop the cleared array as can be seen in Figure 4.5.14(b). This ensures that only properly cleared elements are addressed by the connecting metal, and avoids complications which may arise from over cleared side and corner elements. Reduced size arrays are shown at greater magnification in Figure 4.5.15. A more proper solution to this issue would be to design the

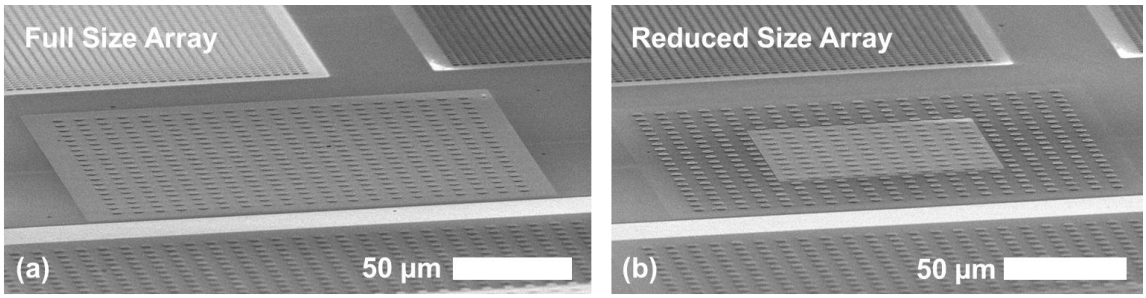

Figure 4.5.14: SEM images of completed full size (a) and reduced size (b) devices following deposition of 25 nm of conformal Ni to connect many micropillars in parallel.

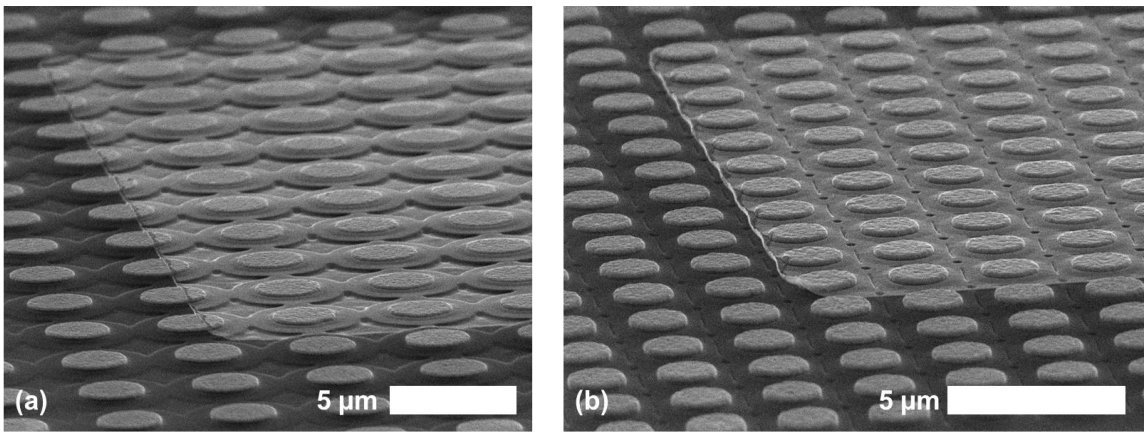

Figure 4.5.15: SEM images of reduced size arrays following conformal Ni deposition. The diameter/pitches of the arrays shown in (a) and (b) are 2.5/4.5 µm and 2/3.5 µm respectively.

layout to eliminate field regions entirely, covering the entire sample with micro/nanostructures of similar size and pitch, with the exception of small open regions when n-contacts can be accessed. While this would more or less eliminate the issue of early clearing at the corners of arrays, it reduces the number of designs which can be included on a sample, restricting them to similar element diameters and pitches. Unfortunately, there is likely no perfect solution to this problem aside from using CMP to planarize the dielectric surface.

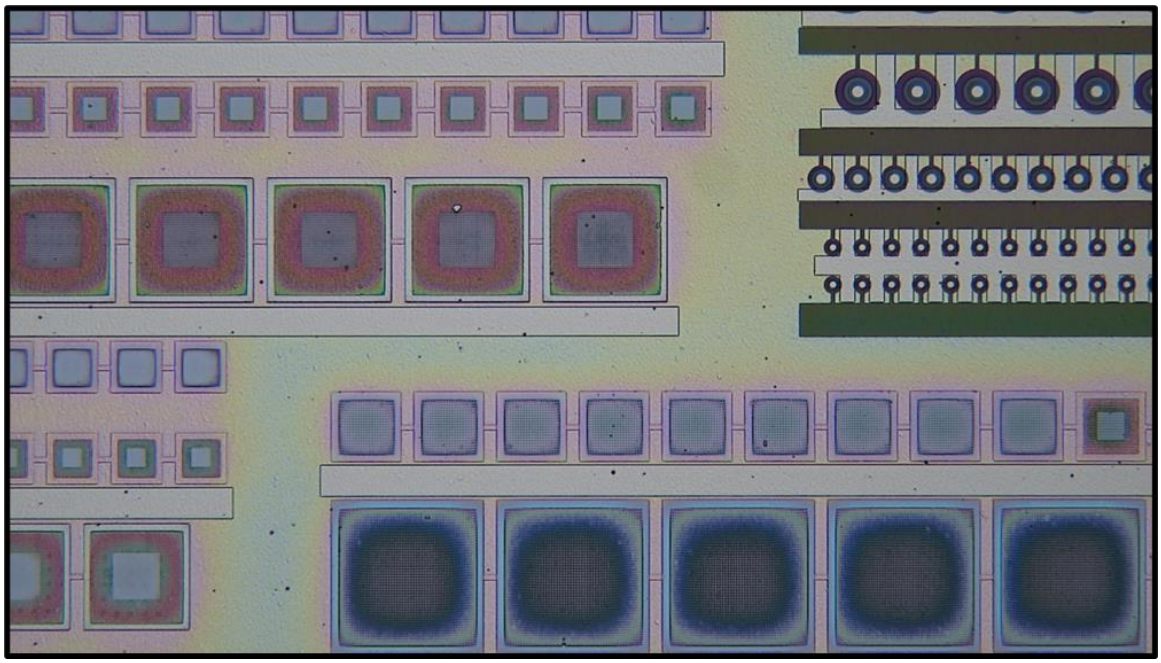

Figure 4.5.16: Optical images of completed devices. The variable color of different arrays is caused by thin film interference in the variable thickness TEOS interlayer of the arrays. Conventional mesa LEDs can be seen in the top right.

Figure 4.5.16 shows a low magnification optical image of many arrays of both full and reduced size. The early clearing of almost all array corners and edges is visible from the variable colors across each array to thin film interfere in the variable thickness TEOS.

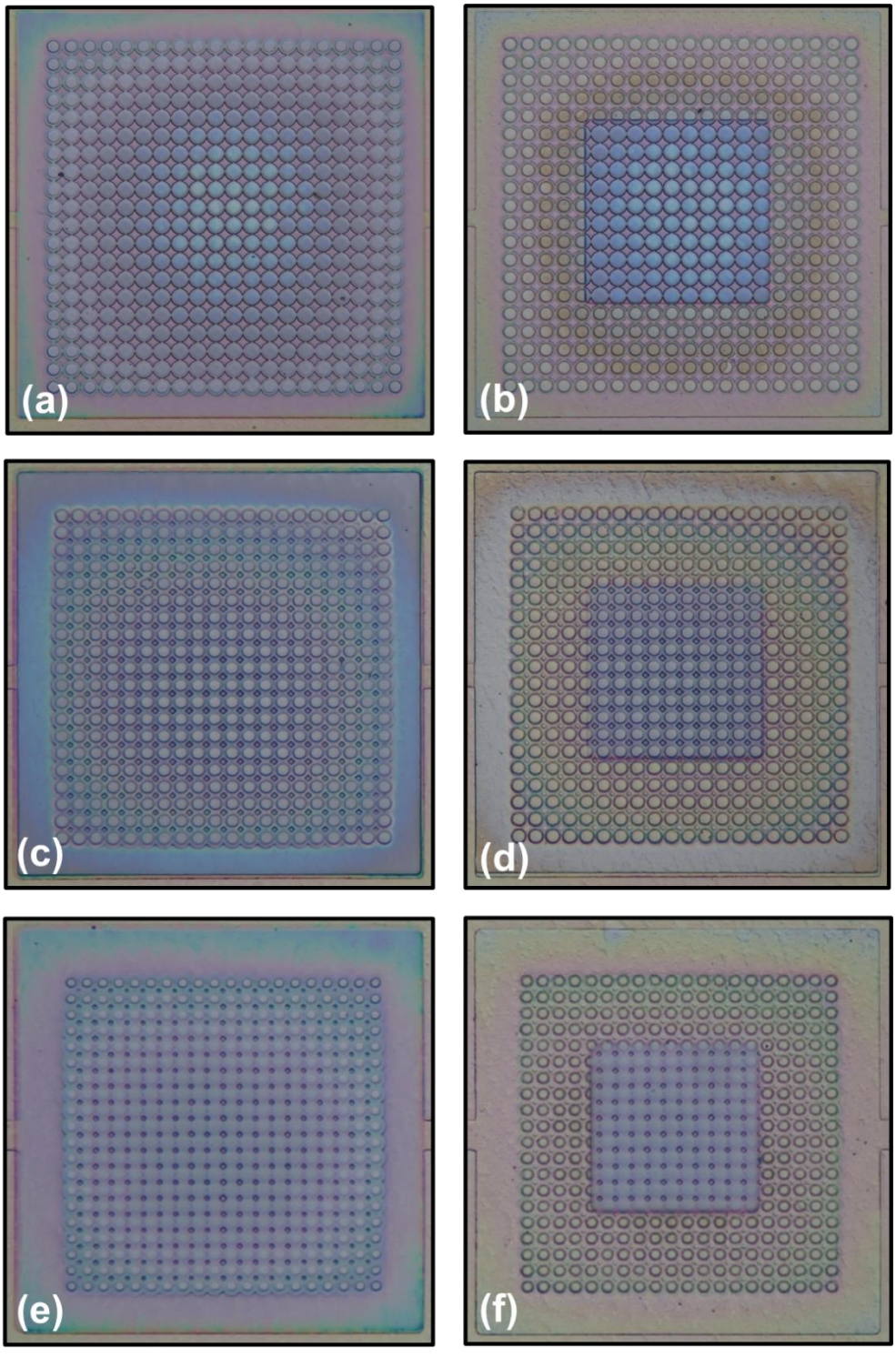

Figure 4.5.17: Optical images of completed devices of full and reduced size. (a) and (b) show 3 μm micropillars on a 5 μm pitch, (c) and (d) show 2 μm micropillars on a 3 μm pitch, and (e) and (f) show 1 μm micropillars on a 2 μm pitch.

A number of conventional mesa LEDs can also be seen in the top right of Figure 4.5.16. High magnification images of full and reduced size devices are shown in Figure 4.5.17 following deposition of a conformal connecting metal (25 nm Ni). These images further highlight the relationship between TEOS thickness and element position with the array. It can also be seen how reducing the size of the connecting metal layer can avoid the complications cause by including potentially over cleared elements at the array corners and edges.

4.6 Future Work

4.6.1 High Aspect Ratio Micropillar and Nanowire LEDs Leveraging TEOS Planarization

Following the extensive process development described in section 4.5, the most immediate near to term extension of this research will be to fabricate devices leveraging these well-developed processes. In order to do so, a new custom grown epistack is desirable, and can be based on either a AlGaN-delta-GaN or conventional AlGaN square well active region. It will be important for this epistack to include a much thicker n-AlGaN region than the custom AlGaN-delta-GaN epitaxy used in sections 4.4 and 4.5, ideally at least 3 μm thick. This will allow fabrication of higher aspect ratio structures as deeper etches could be performed while still remaining within the n-AlGaN layer. The ability to fabricate higher aspect ratio nanowires and micropillars will be important for confirming the results of the simulation study discussed in section 4.3.

These planned devices will utilize planarized TEOS as an interlayer dielectric, taking into account the learnings described in section 4.5.3. Most notably, they will forgo isolated arrays and field regions in favor of covering almost the entire sample surface with nanowires and/or micropillars of similar diameter (likely between 800 nm and 2 μm) and pitch (likely 2x to 3x the diameter of the array elements). Maintaining a consistent fill factor between regions which host different sized element may also aid in the uniformity of photoresist planarization and etchback. These changes will mitigate the issue described in section 4.5.3 in which the edges and corners of isolated arrays clear long before the centers of arrays, as instead each device will be defined by the size of the connecting metal

pad within a monolithic field of identical elements. Openings in this field will be made to allow uninhibited access to the n-contact.

The process development described in section 4.5.3 used a 30/100 nm Cr/Au layer as an n-contact, with this Cr/Au also deposited atop the 40 nm Ni p-contact on the micropillars. This was done to allow more room for error during the etchback process. However, this may not be necessary if the aforementioned changes (using monolithic fields of elements rather than isolated arrays) are effective and simplify the etch back process. Use of only a thin Ni layer on the nanowires/micropillars would increase light extraction substantially, especially when utilizing an AlGaN-delta-GaN active region which reduces the fraction of light emitted with TM-polarization.

4.6.2 Packaging and EQE Characterization of DUV LEDs

Direct characterization of light extraction efficiency and EQE requires use of an integrating sphere which captures and diffuses all light emitted by a device before it is fed into a spectrometer. Devices must be packaged before they can be tested within an integrating sphere, as wafer level probing of the device contacts is not compatible with most integrated sphere test setups. This packaging requires wire bonding and die bonding of individual die to a PCB, and necessitates additional design considerations such as placement of bond pads on each die and connection of individual devices to these bond pads using low resistance metal traces. Our group has been working to develop an integrating sphere test setup for measuring EQE alongside packaging capabilities but unfortunately these efforts are not yet mature. Attempts were made to wire bond the AlGaN-delta-GaN μLEDs described in section 4.4, however the Al bond pads fabricated on that sample were not compatible with the wire bonder available at RIT, and it was

recommended that we instead utilize thicker, Au bond pads in the future. As such, all planned device fabrication will include Ti/Au bond pads of 30/300 nm thickness in order to allow for packaging and EQE testing.

4.6.3 Exploring the Effects of Device Size on Emission Wavelength Shift in AlGaN and InGaN Active Region Devices

As briefly described in section 4.4.3, the current density independent wavelength shift which occurs as the size of μLEDs or micropillars/nanowires is changed has been found to behave differently in AlGaN based DUV emitting LEDs than in InGaN based visible light emitting LEDs. In all visible (red, green, blue) InGaN/GaN LEDs, peak emission wavelength is positively correlated with μLED size, with smaller devices emitting at shorter wavelengths than larger ones at a fixed current density. This is generally attributed to increased strain relaxation in the active region for smaller devices, reducing piezoelectric polarization electric fields and altering the magnitude of energy band bending such that electron and hole ground states are moved marginally farther from their flat band ground states, decreasing emission wavelength. However, in AlGaN DUV emitting LEDs, the opposite trend has been repeatedly observed as described in section 4.4.3, with peak emission wavelength being inversely correlated to device size. The AlGaN-delta-GaN μLEDs described in section 4.4.3 showed a 2.5 nm redshift between 10 μm and 30 μm devices at 200 A/cm^2, with the 10 μm devices emitting at *longer* wavelengths that the 30 μm devices (see Figure 4.4.8).

This phenomenon is not well studied, and most references to it in literature are only in passing. While the relation between peak emission wavelength and device size has been well documented for visible emitting LEDs, only a handful of publications mention it for

DUV emitting LEDs, and none investigate the phenomenon directly or explore the reasons for the contrast between visible and DUV emitting devices. Our group plans to investigate this phenomenon in detail by fabricating many different samples from different epitaxies emitting in the DUV range (260 and 280 nm), the UV-B range (320 nm), the UV-A range (375 nm), and at blue (450 nm) and green (540 nm) wavelengths. By comparing the direction and magnitude of emission wavelength shift as a function of device size (from 5 μm to 200 μm) for these different epitaxies, we hope to better understand this phenomenon which is currently poorly understood in literature.

4.6.4 Microtransfer Printing of DUV Nanowire LEDs

Microtransfer printing has seen increasing interest recently for fabrication of μLED displays and integration of LEDs and lasers onto CMOS and silicon photonics substates. RITs recent acquisition of a Microtransfer printer (located in the RIT cleanroom) has allowed our research group to begin several projects based around the transfer of mesa LEDs and lasers onto CMOS substrates. While LED and laser transfer has been well studied and is currently used commercially, transfer of nanowire LEDs, especially DUV emitting nanowire LEDs, has not yet been attempted. By combining the nanowire liftoff process detailed in section 4.2 with RIT's new Microtransfer printing capability, it may be possible to demonstrate the transfer of arrays of nanowires onto a CMOS host substrate for the first time.

This process may begin as shown in Figure 4.6.1(a), with deposition and patterning of an SiO_2 etch mask, followed by Cl dry etching to form nanowires (Figure 4.6.1(b). Figure 4.6.1 does not show KOH etching after the dry etch to form an inverse taper, however this step *would* likely be included. Following the nanowire dry etch, and

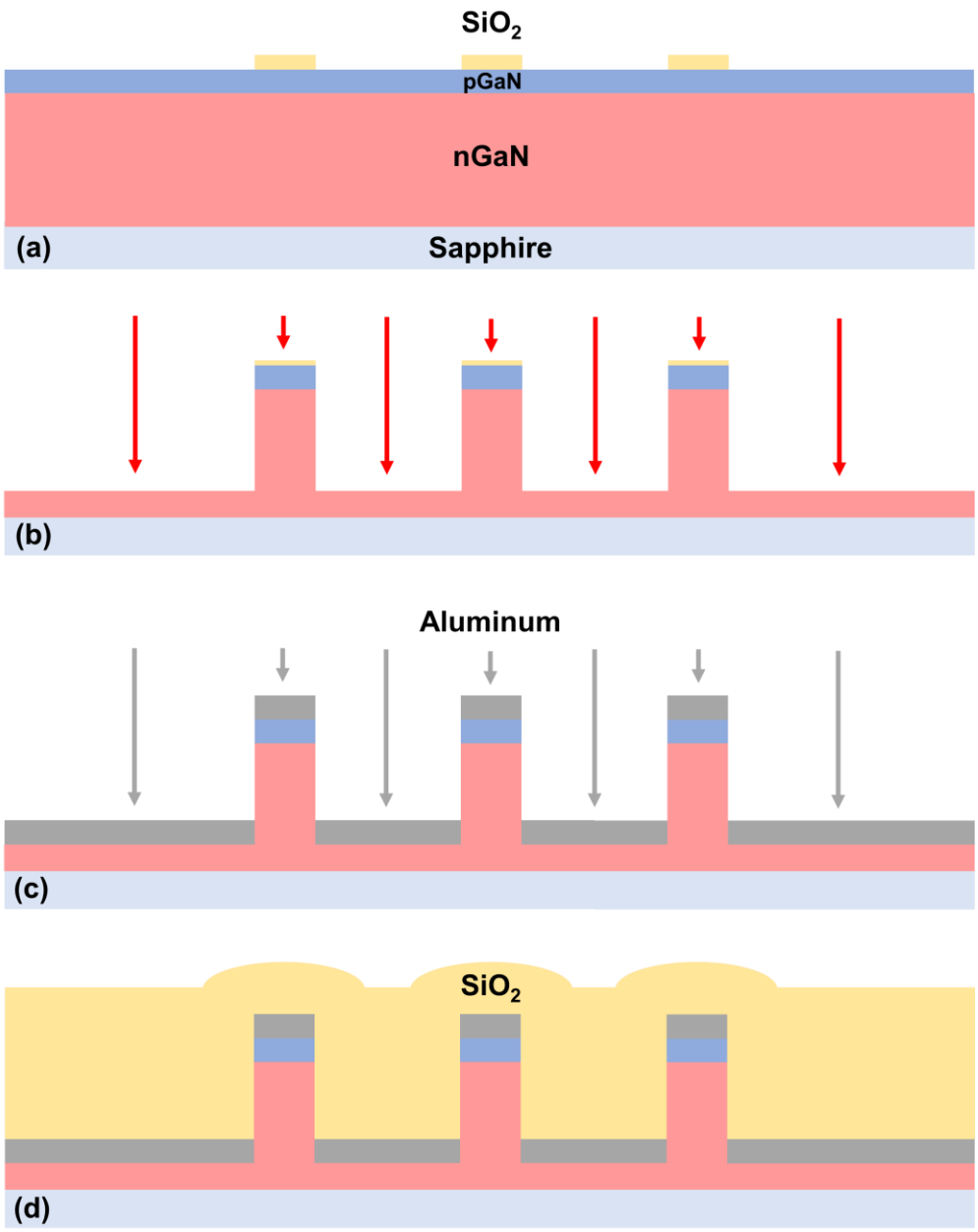

Figure 4.6.1(a-d): Deposition and patterning of SiO_2 to form an etch mask (a), Cl etching of the AlGaN to form nanowires (b), directional Al deposition (c), conformal SiO_2 deposition (d).

thick layer of Al (possible 500 nm) would be deposited via directional thermal evaporation (Figure 4.6.1(c)). SiO_2 (or TEOS or Si_3N_4) would then be deposited via PECVD and planarized as described in section 4.5.2 (Figures 4.6.1(d) and (e)). Apertures would then

be etched in this planarized dielectric to expose the underling Al layer (Figure 4.6.1(f)) and an Al wet etch would be performed to remove the Al from beneath the dielectric (Figure 4.6.1(g)). With the bases of the nanowires now exposed a KOH etch, either heated

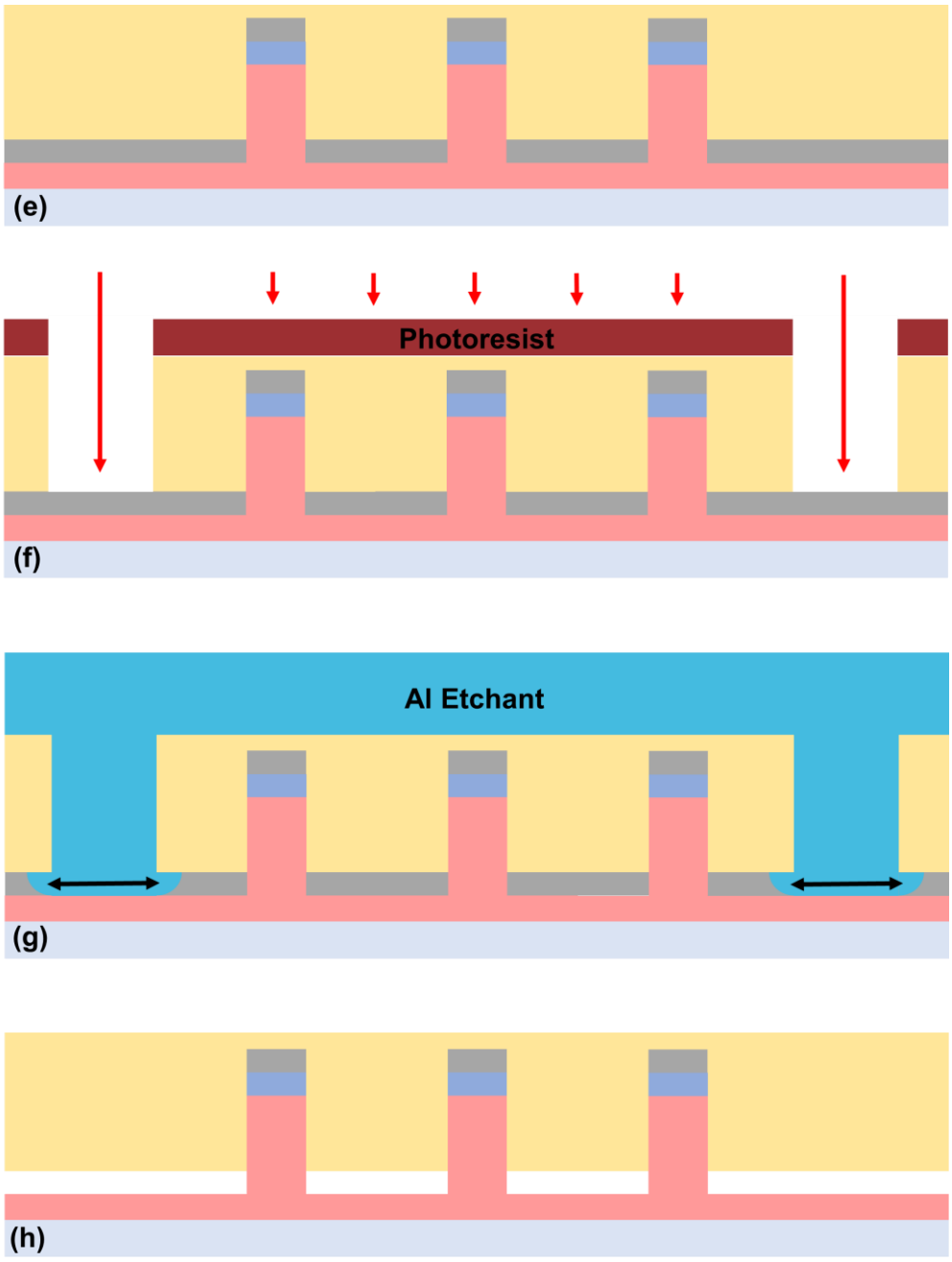

Figure 4.6.1(e-h): SiO_2 planarization (e), opening of apertures in the SiO_2 layer (f), removal of the Al layer under the SiO_2 using an Al wet etch (g-h).

or room temperature, would be used to narrow the bases of the nanowires as described in section 4.2.3, either fully separating them from the substrate or narrowing them enough that they can be broken by a low applied shear force (Figure 4.6.1(i)). The planarized SiO_2

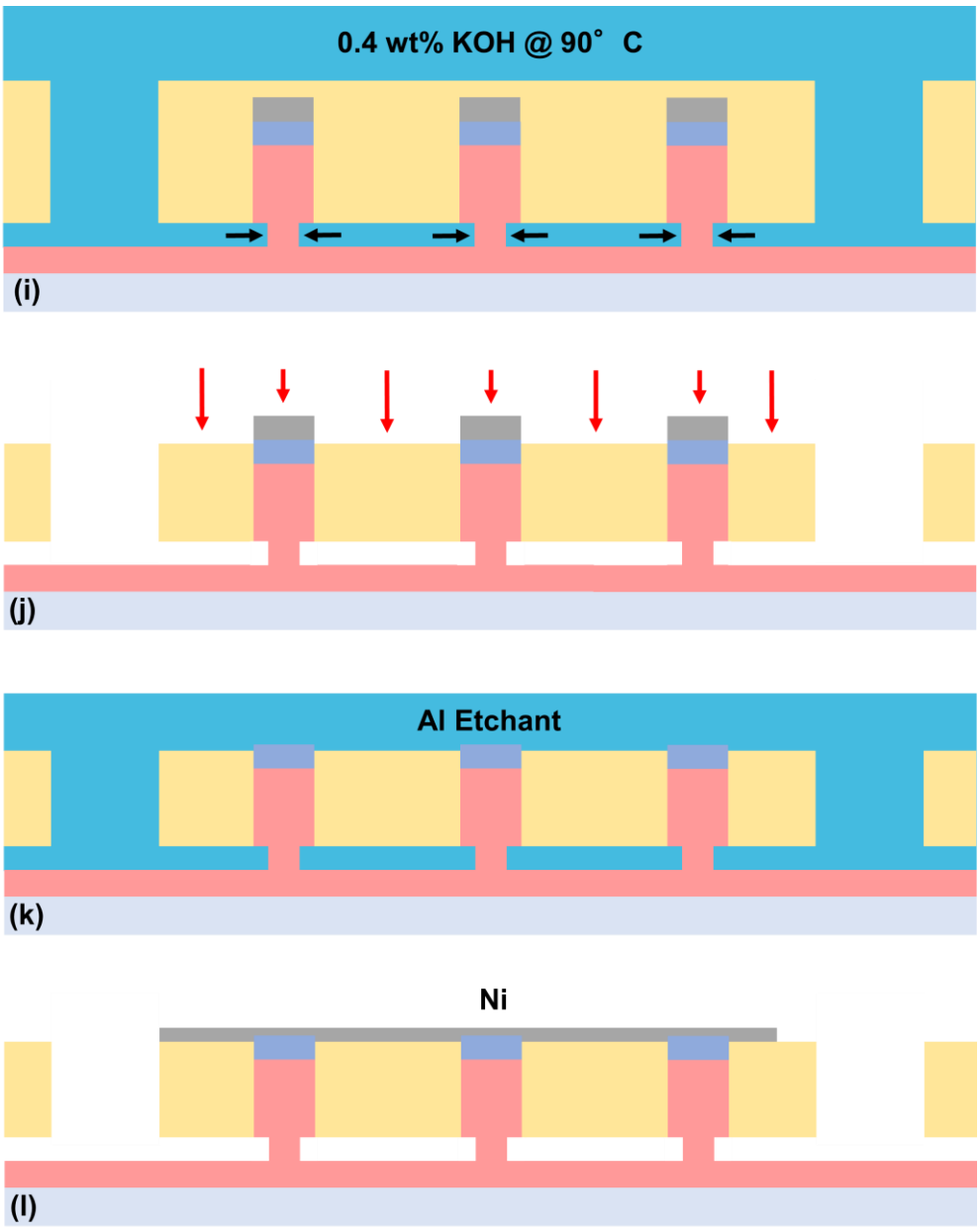

Figure 4.6.1(i-l): Narrowing or separation of the nanowire bases by a heated or room temperature KOH etch (i), etchback of the planarized SiO_2 to expose the Al atop the nanowires (j), removal of the Al with a wet etch (k), deposition of a conformal connecting metal layer (Ni) onto the tops of the nanowires (l).

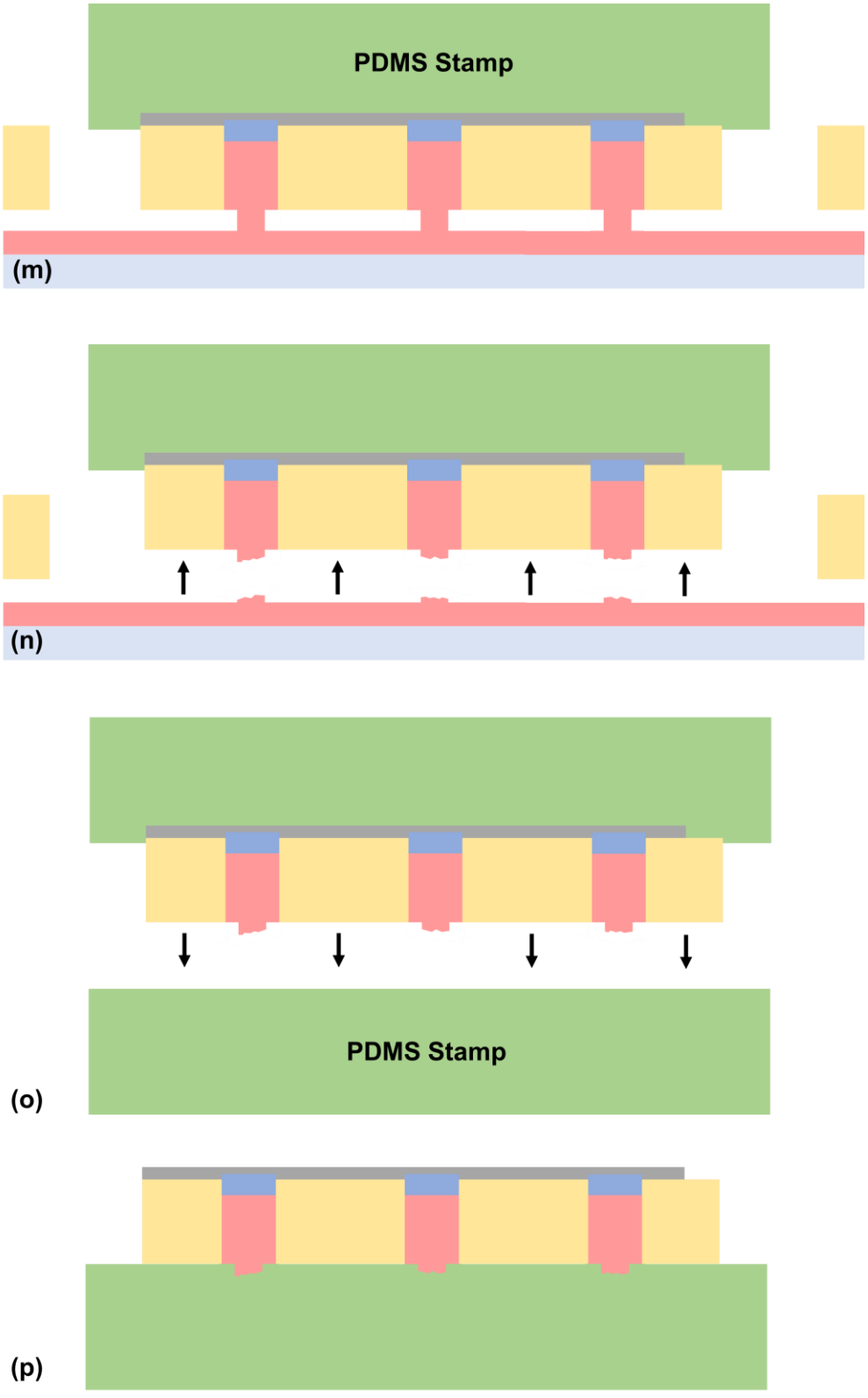

Figure 4.6.1(m-p): Contacting of the PDMS stamp to a device (m), lifting of the device from the substate (n), lowering (o) and placing (p) of the device onto a second PDMS stamp.

would then be etched back to expose the Al tipped nanowires (Figure 4.6.1(j)), and an Al wet etch would then be used to remove the Al, exposing the p-GaN at the top of the nanowires (Figure 4.6.1(k)). A conformal, thin layer of Ni would then be deposited to connect a number of nanowires in parallel, forming a discreet device (Figure 4.6.1(l). A small PDMS stamp on the microtransfer printer head would then be brought into contact with a single device, and would apply tensile and/or shear force to remove the device from the substate (Figure 4.6.1(m)). The device would then be inverted and brought into contact with a second PDMS stamp (Figure 4.6.1(o)), such that the etch bases of the nanowires were in contact with the second stamp (Figure 4.6.1(p)). The device would then be lowered onto an SiO_2 coated CMOS host substate (Figure 4.6.1(q)) and released by the PDMS stamp (Figure 4.6.1(r)). Contact opens would then be etched, permitting access to the Ni p-contact (Figure 4.6.1(s)), and Ni or ITO interconnects would be fabricated to connect the device to the CMOS substrate (Figure 4.6.1(t)).

The described fabrication steps are all tentative and it is likely that many revisions will need to be made along the way in order to obtain working devices. If successful, this would be the first reported demonstration of DUV emitting (or even visible emitting) nanowire array LEDs onto a host substrate.

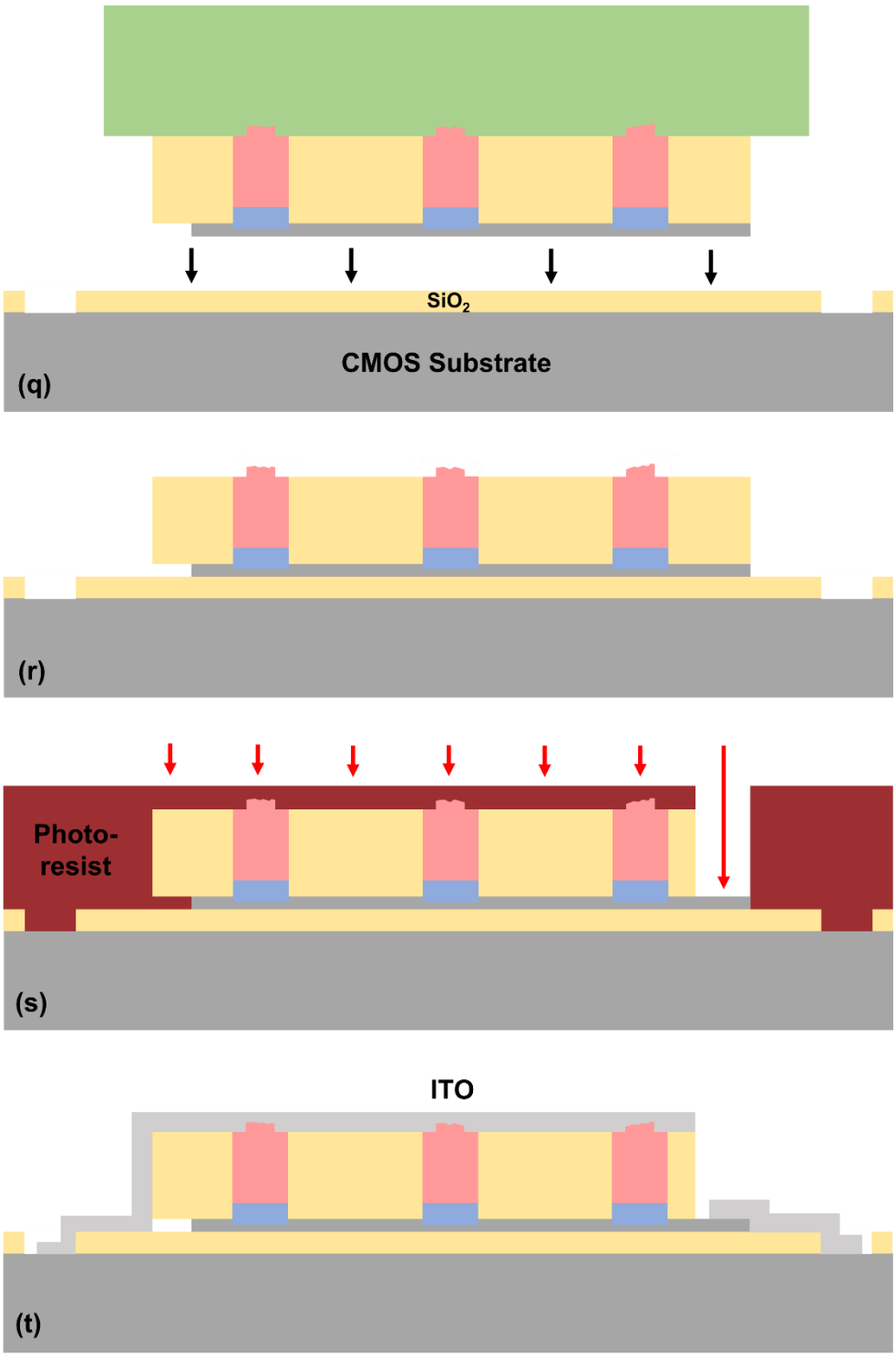

Figure 4.6.1(q-t): Lower of the inverted device onto the CMOS host substrate (q, r), etching of contact opens through the planarized SiO_2 to allow access to the Ni p-contact (s), and deposition of an interconnect layer (either Ni or ITO) to connect the device with the CMOS host substrate (t).

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CHAPTER 5: Visible Wavelength GaN Optoelectronic Devices

5.1 InGaN/delta-InN Quantum Wells for High Efficiency Red Emission

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5.1.1 Introduction

InGaN QW LEDs and lasers have seen a significant increase in utilization over the past decade thanks to substantial increases in efficiency. InGaN LEDs are used extensively in industrial, commercial, and residential lighting applications as well as in emerging display technologies for μLED alternate reality (AR) and virtual reality (VR) headset displays, while InGaN laser diodes are used in digital micro-mirror device (DMD) laser projectors and are desirable for wafer level integration with silicon photonics [2–4]. While blue LEDs have been very well optimized over the past decade, often boasting external quantum efficiencies (η_{EQE}) greater than 85%, InGaN LEDs and lasers emitting at longer wavelengths still struggle to match the efficiencies of their blue counterparts, making it difficult to fabricate high-efficiency, high-brightness red emitters for lighting, display, and laser applications [5–10]. Consequently, μLED displays often rely on AlInGaP for red-emitting pixels, which complicates the fabrication process and increases manufacturing cost [11]. Red lasers using InGaN QWs as the gain medium have not yet been achieved, and as a consequence InGaN quantum dot lasers are instead used in applications which require compact, high-efficiency RGB laser diodes, such as DMD laser projectors [12,13]. The low η_{EQE} of red-emitting InGaN QWs can be attributed to the difficulty of incorporating high In-content layers into the active region, as well as the large internal

electrostatic fields which exist with GaN/InGaN QWs, which can be on the order of 1-5 MV/cm [14–16]. These internal electric fields serve to confine the electron and hole wavefunctions to the edges of the QW, reducing the electron-hole wavefunction overlap (Γ_{e_hh}) which in turn reduces the spontaneous emission radiative recombination rate (R_{sp}). Several techniques have been proposed and examined as means to alleviate the electron-hole wavefunction separation within GaN/InGaN QWs emitting at shorter wavelengths to address the quantum-confined Stark effect (QCSE), including use of non-polar InGaN [17], staggered InGaN QWs [18,19], strain-compensated InGaN QWs [20], and type-II InGaN QWs [21,22], as well as AlGaN-delta-GaN QWs [23,24] and InGaN-delta-InN structures [25]. However, there have been very few studies performed on promising solutions for red emitters based on the InGaN materials system, which are of great importance for μLED displays, laser diodes, and other solid state lighting applications.

While staggered InGaN QWs have been shown to offer improved Γ_{e_hh} when compared to GaN/InGaN QWs, this enhancement becomes less pronounced in the red emission regime around 630 nm [18,19]. Structures that incorporate an ultrathin delta-InN layer at the center of an InGaN QW have been shown to be more effective at maintaining high Γ_{e_hh} and high R_{sp} at green and red wavelengths [25]. In these structures, the peak emission wavelength can be roughly tuned by varying the thickness of the delta-InN layer [25]. The use an InN delta-layer within an InGaN QW has also been shown to enhance Γ_{e_hh} at longer wavelengths within the red emission regime [25], in contrast to other approaches, which suffer from decreasing Γ_{e_hh} as the emission wavelength is increased [18–24]. Recent advances in epitaxial growth of InN make this a feasible approach for high volume manufacturing of epi-stacks incorporating InN delta-layers [26,27]. While

delta-InN structures have been shown to produce more efficient red emission, all existing studies have focused on InGaN-delta-InN QWs with GaN quantum barriers (QBs) grown on GaN substrates. The InN and high In-content InGaN epi-layers required for InGaN-delta-InN QWs have a much larger lattice constant than GaN, leading to formation of high-strength piezoelectric polarization electric fields within the QW which reduce Γ_{e_hh}. To solve this issue, the use of InGaN substrates has been proposed as a means to reduce lattice mismatch induced piezoelectric electric field intensity in the QW [28–31]. Growth of thick InGaN layers on sapphire and GaN substrates has been well-demonstrated [32-40], with these thick InGaN layers serving as growth templates for InGaN LED epi-stacks. However, InGaN QBs must be used in these structures, and suffer from low carrier injection efficiency due to reduced QB height. To resolve these issues and produce the most efficient red-emitting InGaN QW, we propose the use of an InGaN-delta-InN QW with an InGaN growth substrate, which can be used to reduce the piezoelectric electric field intensity while maintaining high carrier injection efficiency.

Here, we investigate an InGaN-delta-InN QW on an InGaN substrate (hereafter denoted as an $In_xGa_{1-x}N/In_yGa_{1-y}N$/delta-InN QW where x represents the In-content in the barrier/substrate and y the In-content in the sub-QW region) which addresses the QCSE and improves R_{sp} with greatly enhanced wavelength tunability in the red regime. In contrast to structures investigated in prior works [25,28–31], our structure combines an InGaN-delta-InN QW active region with an InGaN substrate for the first time. The InGaN substrate, which is fully relaxed and possesses no internal strain itself, has with the same In-content as the QB regions, serves to reduce the lattice mismatch between epitaxial layers and decrease the strength of the resulting piezoelectric polarization electric field in the

active region. Experimentally, use of an InGaN substrate serves to reduce the threading dislocation density in the epitaxial films, leading to decreased non-radiative recombination [32–38]. In this work, we show a monotonic increase in Γ_{e_hh} with increasing λ_{peak} within the red emission regime, from 26% at 555 nm to 57% at 858 nm, which we attribute to stronger localization of the electron-hole wavefunction to the center of the QW with increasing InN delta-layer thickness. The peak emission wavelength (λ_{peak}) of the $In_xGa_{1-x}N/In_yGa_{1-y}N$/delta-InN QW is tunable from ~555 nm - 900 nm by varying the delta-layer thickness between 1 and 8 Å. We compare the optical properties of our $In_xGa_{1-x}N/In_yGa_{1-y}N$/delta-InN QW structure to an InGaN/InGaN QW (hereafter denoted as an $In_xGa_{1-x}N/In_yGa_{1-y}N$ QW where x represents the In-content in the barrier/substrate and y the In-content in the QW region), both with InGaN QBs, at the same λ_{peak}. Results show an R_{sp} enhancement of ~5 - 7x for $In_{0.15}Ga_{0.85}N/In_{0.3}Ga_{0.7}N$/delta-InN QWs with a 3-Å delta-InN layer when compared to a $In_{0.15}Ga_{0.85}N/In_{0.38}Ga_{0.62}N$ QW, with both emitting with λ_{peak} = 630 nm. These results are extremely promising and show that $In_xGa_{1-x}N/In_yGa_{1-y}N$/delta-InN QWs may be a superior alternative to GaN/InGaN QWs for high efficiency red emission.

5.1.2 Simulation Methodology

Band structure and wavefunction calculations were carried out using a self-consistent six-band $k \cdot p$ formalism developed by Chuang *et al.* [41–44]. A detailed description of the numerical model used in the script can be found in [20], and material parameters were obtained from [45,46]. The calculations for an $In_xGa_{1-x}N/In_yGa_{1-y}N$/delta-InN QW utilize a 60 Å $In_xGa_{1-x}N$ QB, 15 Å $In_yGa_{1-y}N$ sub-QW, and InN of variable thickness for the delta-QW, while a 60 Å $In_xGa_{1-x}N$ QB and 30 Å

$In_yGa_{1-y}N$ QW were used for the $In_xGa_{1-x}N/In_yGa_{1-y}N$ QW. Numerical calculations account for all allowed transitions between available confined states in the conduction bands (CB) and valence bands (VB). Valence band mixing, strain effects, carrier screening, spin-orbit interactions, and spontaneous and piezoelectric polarization are considered. The model also accounts for the internal electrostatic fields which result from spontaneous and piezoelectric polarization, which arise due to lattice mismatch, with the details of the electric field calculation available in [20]. A carrier density (n) of $5x10^{18}$ cm^{-3} is used for most comparisons.

5.1.3 Simulation Results

Figures 5.1(a) and 5.1(b) show the alignment of the energy band structure and electron and hole wavefunctions for an $In_{0.15}Ga_{0.85}N/In_{0.38}Ga_{0.62}N$ QW and an $In_{0.15}Ga_{0.85}N/In_{0.3}Ga_{0.7}N$/delta-InN QW with a 3 Å thick delta-layer, respectively. The energy bands shown in Figure 5.1.1 are the first conduction subband ground state and the heavy hole (HH) ground state at zone center (k = 0). The energy band bending which is obvious in both of these band structures is a product of the piezoelectric and spontaneous

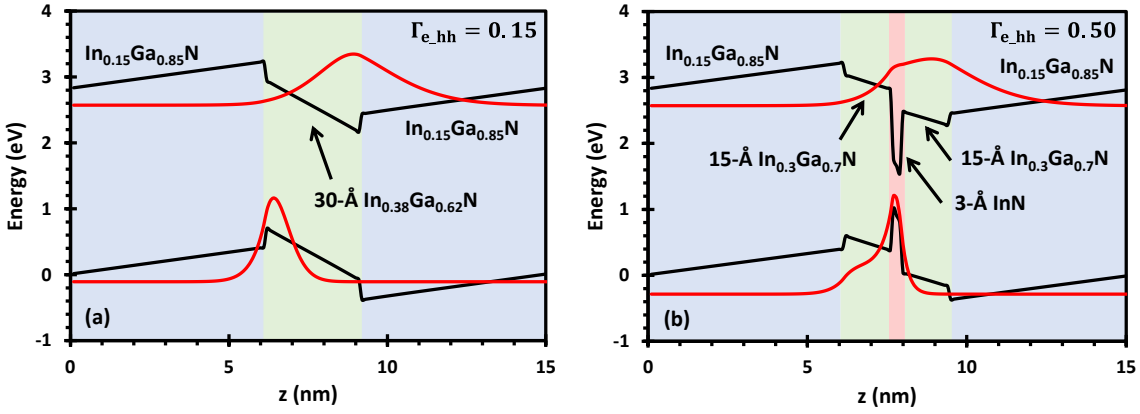

Figure 5.1.1: Bandstructures and ground state wavefunctions in an $In_{0.15}Ga_{0.85}N/In_{0.38}Ga_{0.62}N$ QW (a) and an $In_{0.15}Ga_{0.85}N/In_{0.3}Ga_{0.7}N$/delta-InN QW with a 3 nm delta-layer (b), showing enhanced Γ_{e_hh} for the delta-InN structure.

polarization electric fields that exist within wurtzite GaN and InGaN. The strong electric fields which cause this band bending also serve to shift electrons and holes to opposite sides of the QW, leading to reduced Γ_{e_hh} and R_{sp} due to the QCSE. This effect is most pronounced in Figure 5.1.1(a), in which the electron and hole wavefunctions are strongly localized to the CB minimum and VB maximum on opposite sides of the QW. As a consequence, the Γ_{e_hh} for this $In_{0.15}Ga_{0.85}N/In_{0.38}Ga_{0.62}N$ QW structure, which emits at 630 nm, is a mere 15%. Insertion of a 3 Å InN delta-layer into the center of an $In_{0.15}Ga_{0.85}N/In_{0.3}Ga_{0.7}N$ QW, as shown in Figure 5.1.1(b), serves to localize the electron and hole wavefunctions to the center of the QW, increasing the Γ_{e_hh} to 50%, an improvement of nearly 3.5x. Calculations for conventional and delta-InN structures with GaN QBs and substrates, also emitting at 630 nm, show an Γ_{e_hh} of 10% for a conventional $GaN/In_xGa_{1-x}N$ QW and an Γ_{e_hh} of 18% for a $GaN/In_xGa_{1-x}N$/delta-InN QW.

These enhancements demonstrate the effectiveness of using an InGaN substrate and InGaN QB layers, which lead to reduced interfacial lattice mismatch-based piezoelectric strain between epitaxial layers, which in turn reduces the electric field strength within the active region and improves Γ_{e_hh}. The use of $In_{0.15}Ga_{0.85}N$ QBs on an $In_{0.15}Ga_{0.85}N$ substrate allows for zero lattice mismatch between the barriers and the substrate. The lattice parameters of GaN, $In_{0.15}Ga_{0.85}N$, $In_{0.3}Ga_{0.7}N$, and $In_{0.38}Ga_{0.62}N$, are 3.189 Å, 3.242 Å, 3.296 Å, and 3.323 Å, respectively. In the case of GaN barriers, the lattice mismatch between the QBs and an $In_{0.3}Ga_{0.7}N$ sub-QW would be $\Delta a = 0.106$ Å, corresponding to an in-plane strain of $\varepsilon_{xx/yy} = 3.232\%$. For a $In_{0.38}Ga_{0.62}N$ QW with GaN QBs, the mismatch would be 0.135 Å, for a strain of $\varepsilon_{xx/yy} = 4.058\%$. By using an $In_{0.15}Ga_{0.85}N$ substrate and $In_{0.15}Ga_{0.85}N$ QBs, the lattice mismatch and corresponding in plane-strain for an $In_{0.3}Ga_{0.7}N$

sub-QW and an $In_{0.38}Ga_{0.62}N$ QW are reduced to 0.053 Å/1.616% and 0.082 Å/2.456%, respectively. This significant reduction in strain through use of an InGaN substrate and InGaN QBs is what allows for mitigation of the QCSE and improvement of Γ_{e_hh} by more than 3.5x.

Figure 5.1.2 shows the spontaneous recombination rate spectra for an $In_{0.15}Ga_{0.85}N/In_{0.3}Ga_{0.7}N$/delta-InN structure with a 3 Å InN delta-layer for n = 1 - 10x10^{18} cm^{-3}. A semi-uniform increase in the recombination rate is observed with increasing n along with a slight blueshift of λ_{peak}. This blueshift can be attributed to increased carrier population in the QW, which forces some carriers to recombine with energies above that of the primary transition from states slightly above/below the CB and HH ground states. Although the spontaneous recombination rate spectra of the $In_{0.15}Ga_{0.85}N/In_{0.38}Ga_{0.62}N$ QW

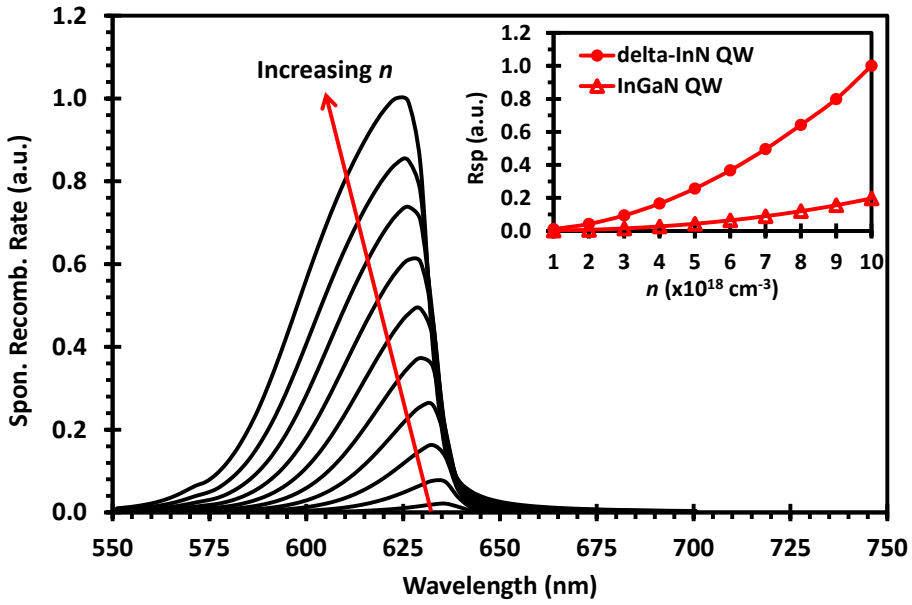

Figure 5.1.2: Spontaneous recombination rate spectra for an $In_{0.15}Ga_{0.85}N/In_{0.3}Ga_{0.7}N$/delta-InN QW with a 3 Å delta-layer for n = 1 - 10x10^{18} cm^{-3}. Inset shows R_{sp} as a function of n for both the $In_{0.15}Ga_{0.85}N/In_{0.3}Ga_{0.7}N$/delta-InN QW with a 3 Å delta-layer and an $In_{0.15}Ga_{0.85}N/In_{0.38}Ga_{0.62}N$ which both have λ_{peak} = 630 nm at n = 5x10^{18} cm^{-3}.

is not shown, it is important to point out that this structure exhibits a greater amount of blueshift than the $In_{0.15}Ga_{0.85}N/In_{0.3}Ga_{0.7}N$/delta-InN QW shown in Figure 5.1.2. The peak emission wavelength of the $In_{0.15}Ga_{0.85}N/In_{0.38}Ga_{0.62}N$ QW blueshifted by 19 nm when increasing n from $1x10^{18}$ to $10x10^{18}$ cm^{-3}, while the peak emission wavelength of the $In_{0.15}Ga_{0.85}N/In_{0.3}Ga_{0.7}N$/delta-InN QW only blueshifted by 13 nm. The inset of Figure 5.1.2 plots the R_{sp} of an $In_{0.15}Ga_{0.85}N/In_{0.38}Ga_{0.62}N$ QW and an $In_{0.15}Ga_{0.85}N/In_{0.3}Ga_{0.7}N$/delta-InN QW with a 3 Å delta-layer as a function of n. A maximum R_{sp} enhancement of 6.8x is realized at n = $1x10^{18}$ cm^{-3}, with enhancement decreasing monotonically with increasing n to a value of 5.07x at n = $1x10^{19}$ cm^{-3}. This represents a substantial increase in radiative emission within the active region of the LED, which will lead to enhanced brightness and power efficiency.

Figure 5.1.3(a) shows the spontaneous recombination rate spectra for delta-InN layers between 1 and 8 Å thick. Increasing the delta-InN thickness by only a single angstrom (less than one InN monolayer), produces a significant increase in λ_{peak}. As the delta-layer thickness increases, confinement of energy states within the delta-layer

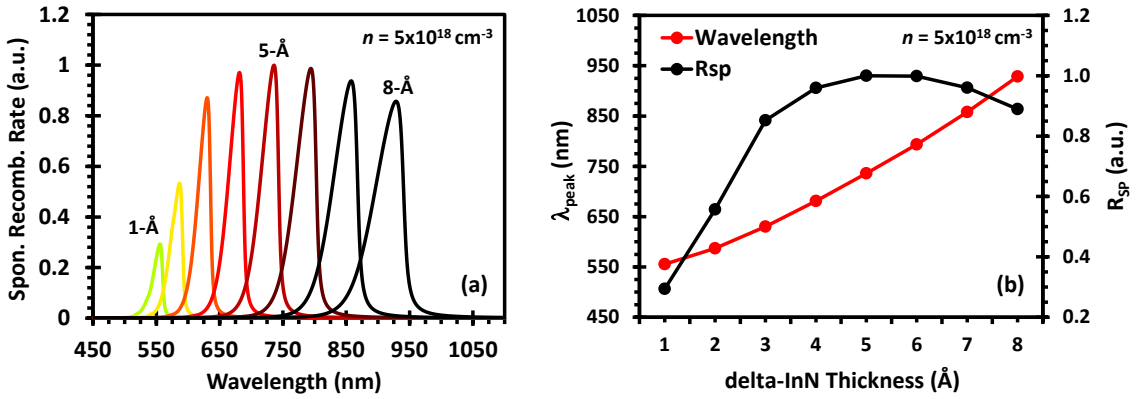

Figure 5.1.3: (a) Spontaneous recombination rate spectra for $In_{0.15}Ga_{0.85}N/In_{0.3}Ga_{0.7}N$/delta-InN structures of varying delta-InN thickness for n = $5x10^{18}$ cm^{-3}. (b) λ_{peak} and R_{sp} as a function of delta-InN thickness.

decreases, allowing the CB and HH ground states move closer to their theoretical minima/maxima, reducing the energy of the primary inter-band transition and increasing the emission wavelength as shown in Figure 5.1.3(b). The Γ_{e_hh} increases with increasing delta-layer thickness up to a thickness of 6 Å, whereupon it begins to decrease as the delta-layer begins to behave more as an InN square well, with wavefunctions beginning to separate to opposite sides of InN delta-layer. This trend in Γ_{e_hh} is mirrored by a similar trend in R_{sp}, or the integral of each of the emission curves show in Figure 5.1.3(a). R_{sp} also increases with increasing delta-layer thickness up to a thickness of 6 Å and decreases beyond it, illustrating the dependence of R_{sp} on Γ_{e_hh}, as shown in Figure 5.1.3(b).

While we have calculated the spectra for delta-layer thicknesses between 1 and 8 Å in increments of 1 Å, it is important to note that a single InN monolayer (ML) is approximately 3 Å thick [46]–[49]. While precision growth of single (3 Å) and double (6 Å) monolayers of InN has been demonstrated through use of both metal organic chemical vapor deposition (MOCVD) and molecular beam epitaxy (MBE) [47–50], the growth of InN fractional monolayers (FMLs), for example a 4 Å (4/3 ML) layer, is more difficult, as a variety of complex growth conditions effect the long- and short-range order of the incomplete top monolayer [48–50]. While Figure 5.1.3 shows InN layers of fractional thickness (1, 2, 4, 5 Å, etc.), it is important to note that our theoretical model does not make any accommodations for the additional morphologic complexity of FMLs, and treats these layers of fractional thickness as isotropic and continuous. Even assuming growth of InN FMLs to be reliably attainable, the emission peaks within the red emission regime are spaced by between 30 and 50 nm. For applications in which specific red

wavelengths are desired, simply adjusting the InN delta-layer thickness would likely be insufficient to achieve precise emission wavelength targets.

Figure 5.1.4(a) plots λ_{peak} as a function of the In-content in both the QB and sub-QW regions for an $In_xGa_{1-x}N/In_yGa_{1-y}N$/delta-InN QW with a 3 Å delta-layer at $n = 5x10^{18}$ cm^{-3}. It is evident that λ_{peak} can be tuned continuously over a very large range through manipulation of the In-content in the $In_xGa_{1-x}N$ QB, $In_yGa_{1-y}N$ sub-QW, or both, for a fixed delta-layer thickness. This approach could allow for easy tuning of red LED λ_{peak} without the need to grow InN FMLs. A single 3 Å InN monolayer could be used, and the In-content in the QB and sub-QW regions could be tuned through alteration of the gas flow/atom flux rates during the MOCVD/MBE epitaxial growth process in order to achieve extremely precise emission wavelength targets.

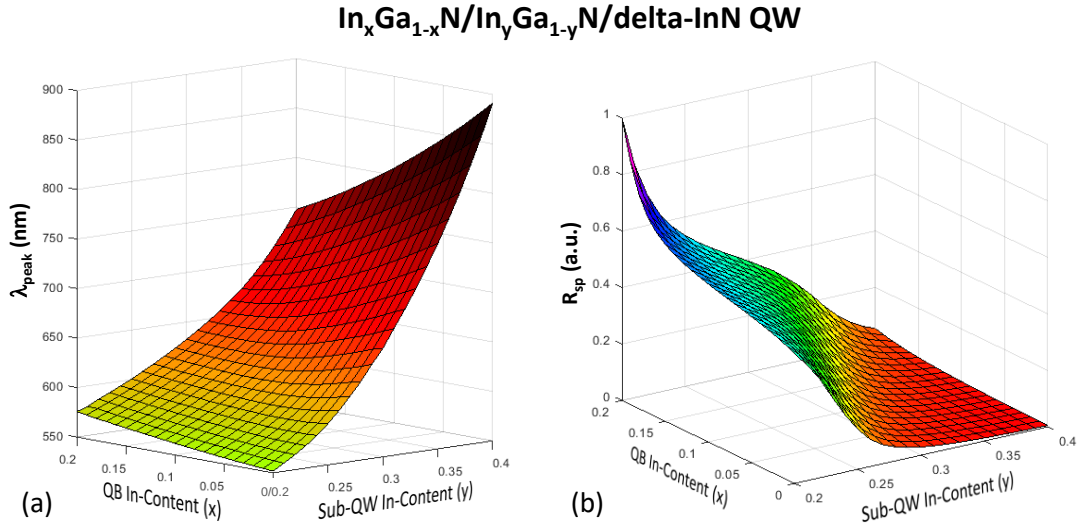

Figure 5.1.4: (a) λ_{peak} dependence on the In-content of the QB and sub-QW regions for an $In_xGa_{1-x}N/In_yGa_{1-y}N$/delta-InN QW with a 3 Å delta-layer, showing that red emission wavelength is continuously tunable through small variations of the In-content in these regions. Chart colors are accurate. (b) R_{sp} dependence on the In-content in the QB and sub-QW regions.

As shown in Figure 5.1.4(a), engineering of the In-content in the $In_xGa_{1-x}N$ QB and $In_yGa_{1-y}N$ sub-QW can be used to vary λ_{peak} from green (550 nm) to the near-IR (890 nm). Figure 5.1.4(b) plots R_{sp} for the same structure as a function of In-content in the QB and sub-QW regions. Combined, the data presented in these two figures shows that use of $In_xGa_{1-x}N/In_yGa_{1-y}N$/delta-InN QWs could allow for design of high-efficiency red LEDs. Figure 5.1.4(b) also clearly illustrates the advantage of using InGaN in the substrate and QB, with R_{sp} increasing monotonically with In-content in the QB for all values of In-content in the sub-QW.

The large R_{sp} enhancements demonstrated through insertion of an InN delta-layer into the center of the InGaN QW translate directly to improvements in radiative recombination efficiency (η_{RAD}). Figure 5.1.5(a) plots the η_{RAD} calculated using a simple ABC-model with Shockley-Read-Hall (SRH) and auger coefficients of $1x10^6$ s^{-1} and $3.5x10^{-34}$ cm^6s^{-1} respectively [51]. The SRH and Auger coefficient values reported in [51] are taken from a variety of experimental and theoretical work, and are reasonable approximations for the materials used in our simulations. It is worthy of note that Auger coefficient value used here and reported in [51] is the theoretical value for InGaN, while the experimentally determined value may be as high as $1.4x10^{-30}$ cm^6s^{-1}. As expected, our $In_xGa_{1-x}N/In_yGa_{1-y}N$/delta-InN QW shows higher η_{RAD} than an $In_xGa_{1-x}N/In_yGa_{1-y}N$ QW emitting at 630 nm across a wide range of carrier densities. This enhancement can be attributed to the enhanced electron-hole wavefunction overlap facilitated by the InN delta-layer as previously described and shown in Figure 5.1.1. Carrier injection efficiencies (η_{INJ}) were calculated for both structures as a function of *n* using the model described in [43]. The parameters used in this calculation were taken from [43]. Figure 5.1.5(b) shows

the η_{INJ} of each structure decreasing with increasing n due to increased carrier leakage from the QW at higher carrier densities (dashed lines). The η_{INJ} is higher for the $In_{0.15}Ga_{0.85}N/In_{0.38}Ga_{0.62}N$ QW at higher n due to its greater QB height of 0.29 eV, with the $In_{0.15}Ga_{0.85}N/In_{0.3}Ga_{0.7}N$/delta-InN having a barrier height of only 0.18 eV.

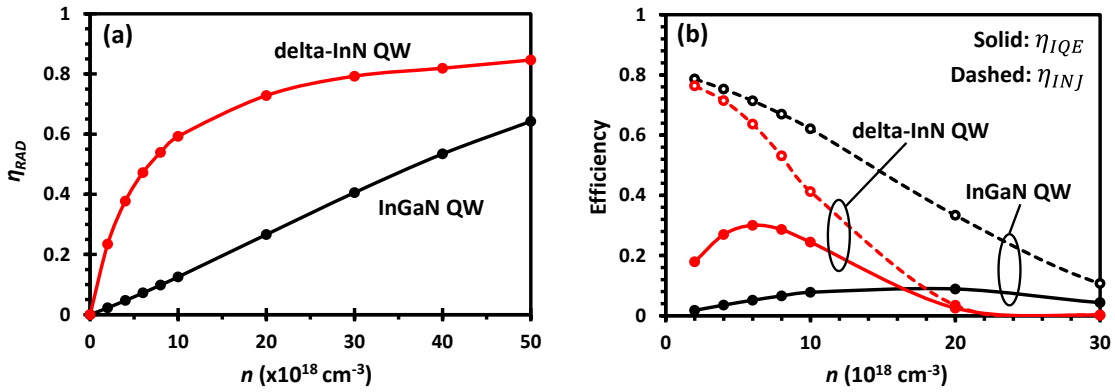

Figure 5.1.5: (a) η_{RAD}, and (b) η_{INJ} (dashed line) and η_{IQE} (solid line) for an $In_{0.15}Ga_{0.85}N/In_{0.38}Ga_{0.62}N$ QW (black) and an $In_{0.15}Ga_{0.85}N/In_{0.3}Ga_{0.7}N$/delta-InN QW with a 3 Å delta-layer QW (red) as n. Both structures have λ_{peak} ~ 630 nm at n = 5x10^{18} cm^{-3}.

As previously described, both structures were designed to emit at λ_{peak} = 630 nm at n = 5x10^{18} cm^{-3}, with the $In_{0.15}Ga_{0.85}N/In_{0.38}Ga_{0.62}N$ structure achieving this with an In-content 0.38 in the QW and the $In_{0.15}Ga_{0.85}N/In_{0.3}Ga_{0.7}N$/delta-InN structure with an In-content of 0.30 in the sub-QW. The greater band offset between the QB and QW regions in the $In_{0.15}Ga_{0.85}N/In_{0.38}Ga_{0.62}N$ structure makes it more resistant to carrier leakage when compared to the $In_{0.15}Ga_{0.85}N/In_{0.3}Ga_{0.7}N$/delta-InN structure. The solid lines in Figure 5.1.5(b) plots the internal quantum efficiency (η_{IQE}), which is the product of η_{RAD} and η_{INJ}. Although the injection efficiency of the $In_xGa_{1-x}N/In_yGa_{1-y}N$/delta-InN structure is always lower than that of the $In_xGa_{1-x}N/In_yGa_{1-y}N$ QW, its η_{IQE} is significantly higher within the normal operating regime of LEDs (n = 1 - 10x10^{18} cm^{-3}) due to the massively enhanced

η_{RAD} within this carrier density regime as shown in Figure 5.1.5(a). The η_{IQE} of the $In_{0.15}Ga_{0.85}N/In_{0.3}Ga_{0.7}N$/delta-InN QW at n = 2x10^{18} cm^{-3} is 10x greater than that of the $In_{0.15}Ga_{0.85}N/In_{0.38}Ga_{0.62}N$ QW, with this enhancement decreasing linearly to 3.1x at n = 1x10^{19} cm^{-3}. At carrier densities in excess of n = 2x10^{19} cm^{-3} the η_{IQE} of the $^{InxGa1xN}/In_yGa_{1-y}N$/delta-InN structure falls below that of the $In_xGa_{1-x}N/In_yGa_{1-y}N$ QW. An electron blocking layer (EBL) could be possibly be used to reduce the carrier leakage of the delta-InN structure and improve its η_{INJ} at higher n.

It is also of great interest to investigate the potential of this $In_xGa_{1-x}N/In_yGa_{1-y}N$/delta-InN QW for laser applications. Figure 5.1.6 shows the material gain for an $In_{0.15}Ga_{0.85}N/In_{0.38}Ga_{0.62}N$ QW and an $In_{0.15}Ga_{0.85}N/In_{0.3}Ga_{0.7}N$/delta-InN QW with a 3 Å delta-layer on $In_{0.15}Ga_{0.85}N$ substrates as a function of n. It has previously been shown that use of ternary InGaN substrates can dramatically improve the material gain and reduce the

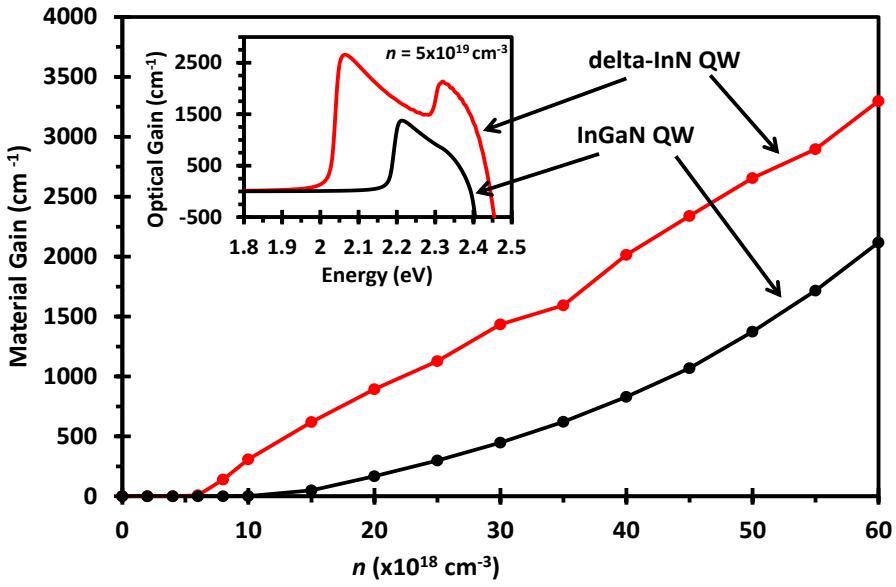

Figure 5.1.6: Material gain as a function of n for an $In_{0.15}Ga_{0.85}N/In_{0.38}Ga_{0.62}N$ QW (black) and an $In_{0.15}Ga_{0.85}N/In_{0.3}Ga_{0.7}N$/delta-InN QW (red). Inset shows the optical gain spectra at n = 5x10^{18} cm^{-3}.

threshold carrier density of InGaN QW lasers emitting in the green and yellow emission regimes [28]. Here, our material gain calculations are based on Fermi's Golden Rule and a Lorentzian line-shape function [20,28,42].

Inhomogeneous broadening was not considered as no experimental data has been reported on inhomogeneous broadening for InGaN grown on ternary substrates [28]. The results shown in Figure 5.1.6 indicate that the material gain and threshold carrier density of InGaN QW lasers emitting in the red emission regime can be enhanced through insertion of an InN delta-layer into the QW. Figure 5.1.6 shows that exceptional improvements in material gain can be realized through use of a delta-layer structure for lower n, with this enhancement becoming less pronounced as n increases. Assuming the threshold material gain to be approximately 1500 cm^{-1} [20,52], we see that the threshold carrier density (n_{th}) is achieved around $n_{th} = 3x10^{19}$ cm^{-3} for the $In_{0.15}Ga_{0.85}N/In_{0.3}Ga_{0.7}N$/delta-InN QW (red), with the $In_{0.15}Ga_{0.85}N/In_{0.38}Ga_{0.62}N$ QW (black) having a material gain of less than 500 cm^{-1} at the same n. n_{th} is only achieved in the $In_{0.15}Ga_{0.85}N/In_{0.38}Ga_{0.62}N$ QW at a carrier density $n = 5x10^{19}$ cm^{-3}. The inset of Figure 5.1.6 shows the optical gain spectra of the $In_{0.15}Ga_{0.85}N/In_{0.3}Ga_{0.7}N$/delta-InN QW with a 3 Å delta-layer (red) and the $In_{0.15}Ga_{0.85}N/In_{0.38}Ga_{0.62}N$ QW (black) at $n = 5x10^{19}$ cm^{-3}. The twin peaks present in the spectrum of the delta-layer structure are due to activation of a secondary interband transition which becomes available within the delta-layer once carrier density exceeds $n = 2x10^{19}$ cm^{-3}. The effects of the secondary, higher energy peak at 2.32 eV can be eliminated through engineering of the laser cavity length. While both structures emit with λ_{peak} = 630 nm (1.97 eV) at $n = 5x10^{18}$ cm^{-3}, their optical gain spectra peak at shorter wavelengths of 602 nm (2.06 eV) and 561 nm (2.21 eV) for the

$In_{0.15}Ga_{0.85}N/In_{0.3}Ga_{0.7}N$/delta-InN and $In_{0.15}Ga_{0.85}N/In_{0.38}Ga_{0.62}N$ QWs respectively. Just as λ_{peak} can be precisely tuned through manipulation of the In-content in the QB and sub-QW as shown in Figure 5.1.4(a), the position of the primary peak in the optical gain spectra of an $In_xGa_{1-x}N/In_yGa_{1-y}N$/delta-InN QW can likewise be tuned for laser applications.

5.1.4 Conclusions

In summary, we have demonstrated for the first time that insertion of an InN delta-layer into an InGaN QW, along with use of an InGaN growth substrate, can produce unparalleled localization the electron and hole wavefunctions towards the center of the QW for red emission. This novel InGaN/InGaN/delta-InN QW produces significant improvements in Γ_{e_hh} and R_{sp} within the red emission regime, enabling high-efficiency red LEDs and laser diodes. Use of an InGaN growth substrate reduces the lattice mismatch experienced by epitaxial layers, reducing the magnitude of the spontaneous and piezoelectric electric fields, and mitigating the QCSE in the active region. Analysis of structures emitting at a benchmark red emission wavelength of 630 nm shows an Γ_{e_hh} of 50% for a $In_{0.15}Ga_{0.85}N/In_{0.3}Ga_{0.7}N$/delta-InN structure on an InGaN substrate, compared to 10% for a $In_{0.15}Ga_{0.85}N/In_{0.38}Ga_{0.62}N$ QW on an InGaN substrate and 18% for a $In_{0.15}Ga_{0.85}N/In_{0.28}Ga_{0.72}N$/delta-InN QW on a GaN substrate. This enhanced Γ_{e_hh} increases R_{sp} by between ~5 - 7x within the carrier density range n = 1-10x10^{18} cm^{-3}, which in turn serves to enhance η_{IQE} by between 3 – 10x when compared to a $In_xGa_{1-x}N/In_yGa_{1-y}N$ QW emitting at the same wavelength. λ_{peak} can also be carefully tuned through manipulation of InN delta-layer thickness and In-content in the QB and sub-QW regions to achieve precise emission wavelength targets. Additionally, notable enhancements in

material gain and n_{th} can also be achieved through use of an InN delta-layer making this structure of secondary interest for use in laser diodes. The $In_xGa_{1-x}N/In_yGa_{1-y}N$/delta-InN QW structure grown on an InGaN substrate investigated in this work shows great promise for achieving high-efficiency InGaN LEDs and laser diodes emitting in the red spectral regime. This advancement could revolutionize the development of emitters for μLED displays and laser diodes by allowing for development of blue, green, *and* red pixel elements based on the same materials system.

5.2 Micropillar Array LEDs Emitting at 520 nm

Presented orally at EMC 2021

5.2.1 Introduction

Micropillar light-emitting diodes (LEDs) have long been investigated as alternatives to conventional mesa LEDs, as they allow for increased light extraction efficiency (LEE) and a reduction of the internal electric field strength in AlInGaN alloys. Micropillars also show potential for use as single pixels in micro-LED (μLED) displays and photonic crystal surface-emitting laser diodes (PCSELs). While epitaxially grown micropillars allow for higher material quality in the active region and reduction of the quantum confined Stark effect, they often suffer from uniformity and yield issues, and are difficult to fabricate into ordered, addressable arrays. Micropillars can alternatively be formed through dry etching of epitaxially grown light emitting layers, taking advantage of processes and tools developed by the semiconductor industry. The general process for fabricating a micropillar array LED involves dry-etching of an n-i-p epitaxial stack to form high aspect ratio structures, followed by deposition of the n-contact metal, application of an interlayer dielectric, and deposition of the p-contact material. As most LEDs emitting in the visible range are based on the AlInGaN material system, an aggressive Cl_2 plasma must be used to perform the dry-etch. The poor selectivity of Cl_2 plasmas against conventional dry-etch hardmask materials such as photoresist and SiO_2 necessitates the use of a metal hardmask such as Ni, which is capable of withstanding the extended etch times required to form micropillars with heights greater than 1 μm. This thick Ni hardmask must be removed from the micropillars in order to maximize η_{EXT}. In devices which use self-masked n-metal deposition, in which the micropillars themselves act at the mask for

deposition of a universal n-contact, wet etching of the Ni hardmask following deposition of the n-metal (which itself often contains Ni) is not possible, because the chemistries commonly used to etch Ni will also attack the other metals in the n-metal stack (Ti, Al, Ni, etc.). For this reason, an alternative method of removing the Ni hardmask is desired. Here we present a novel method for removing a metal hardmask from the tops of dry-etched GaN micropillars which does not involve metal etch chemistry, but instead relies upon an underlying "liftoff" layer to separate a thick metal "cap" from the tops of the micropillars.

5.2.2 Micropillar Array Fabrication

The epistack used in this work was purchased from a commercial vendor, and was grown on a sapphire substrate using MOCVD. A cross-sectional view of the epistack is shown in the top left of Figure 5.2.1. After cleaning of the wafer using a standard RCA clean, a 300 nm layer of SiO_2 (TEOS) was deposited on the wafer (Figure 5.2.1(a)), followed by patterning of the Ni hardmask through a liftoff process (Figure 5.2.1(b)). The Ni was then used to mask a CF_4/CHF_3 dry-etch of the underlying SiO_2 (Figure 5.2.1(c)), and a subsequent Cl_2/Ar dry-etch of the GaN (Figure 5.2.1(d)), with ~200 nm of Ni capable of withstanding etch depths of more than 7 μm. The micropillars were then etched in a hydroxyl-based solution containing 40% AZ400K in DI water at 80°C to remove dry-etch damage and smooth the sidewalls of the micropillars (Figures 6.7(e-g)). A universal n-metal (20/150/80/100 nm Ti/Al/Ni/Ag) contact, masked by the micropillars themselves (Figure 5.2.1(h)), was then deposited and annealed at 850 C for 60 seconds. A 10:1 buffered oxide etch (BOE) solution was then used to remove the SiO_2 layer, releasing the thick metal caps (Ni/Ti/Al/Ni/Ag) which are washed away in the etch solution (Figures 6.7(i-l)).

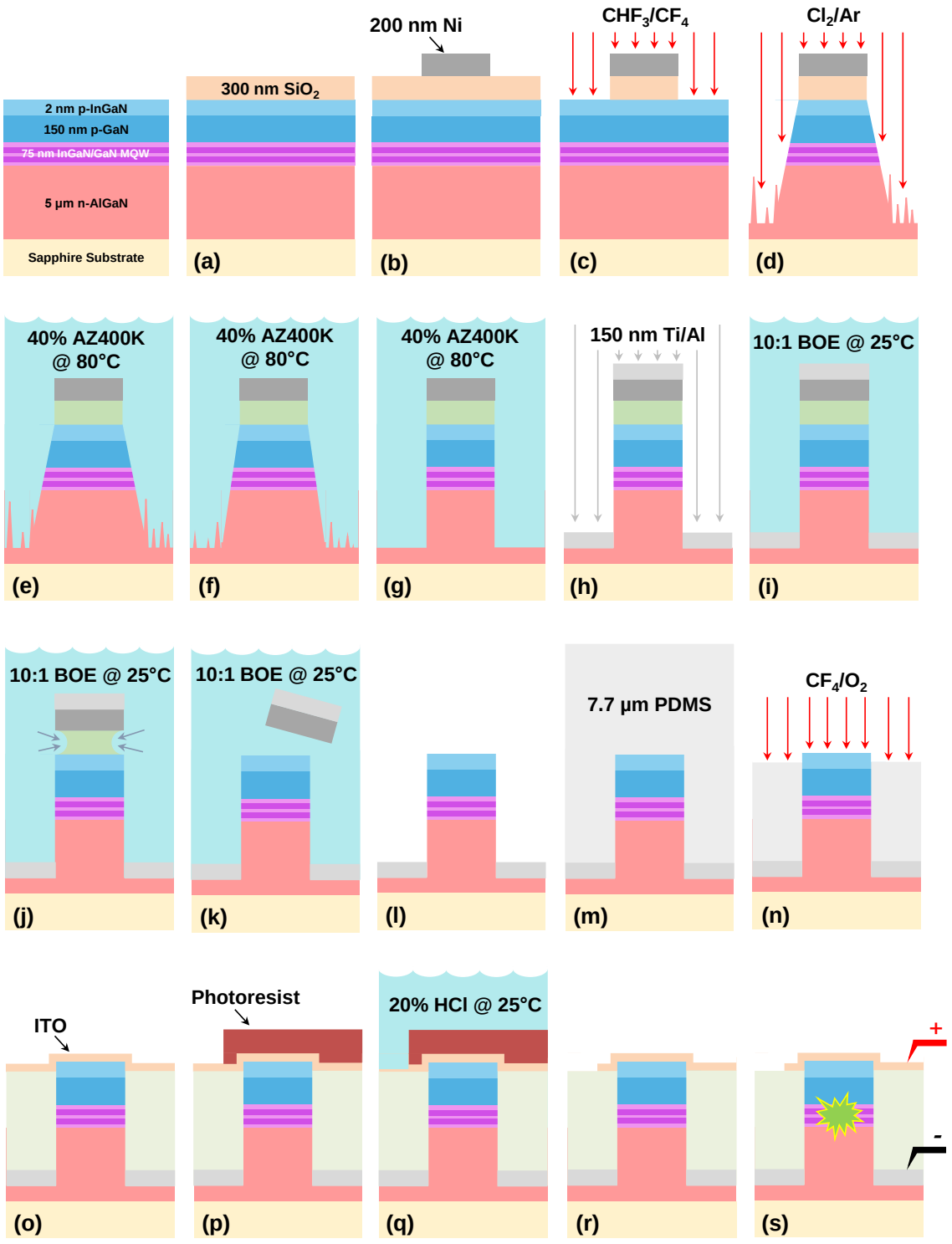

Figure 5.2.1: Fabrication process schematic for green nanowire LEDs (not to scale).

Polydimethylsiloxane (PDMS) was then coated over the "bare" micropillars and etched-back to expose the p-GaN micropillar tips (Figures 6.7(m-n)). A 100 nm thick layer of transparent Indium Tin Oxide (ITO) was then deposited via sputtering (Figure 5.2.1(o)). The ITO layer was then patterned and etched using a solution of 20% HCl at 25°C, linking many micropillars in parallel and allowing for electrical excitation of arbitrarily large arrays simultaneously (Figures 6.7(p-s)).

Using this process, we fabricated high brightness arrays of electrically driven micropillars emitting at 550 nm with a linewidth of ~60 nm. The arrays consisted of micropillars approximately 2.5 μm in diameter with heights of 3 μm on a 10 μm pitch. Figure 5.2.2 shows SEM images of the micropillar arrays following the hydroxyl-based wet etch step. Removal of the metal caps from the micropillars in critically important in allowing increasing the light extraction efficiency from top-down fabricated micropillars, while the use of a universal n-metal contact allows for decreased series resistance and more uniform emission intensity from larger arrays.

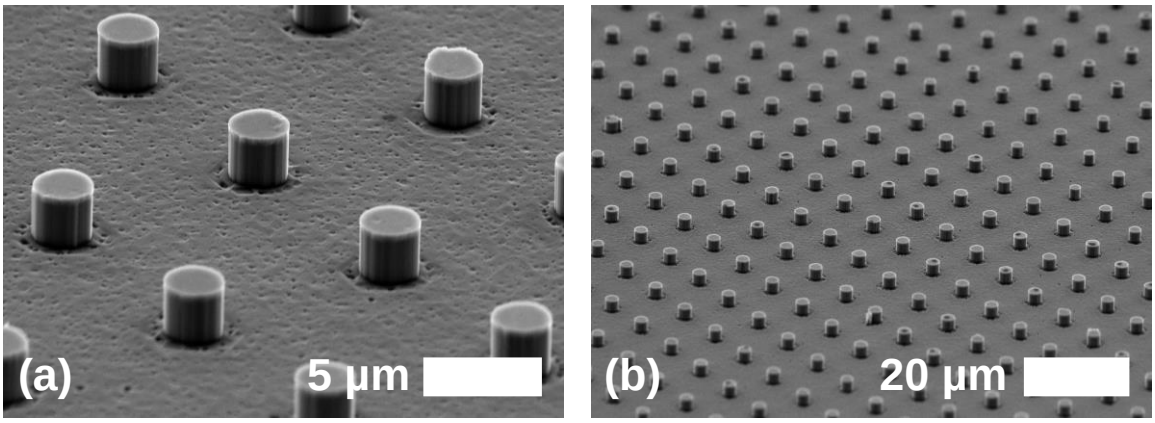

Figure 5.2.2: SEM images show the nanowire arrays after the hydroxyl-based wet etch step.

5.2.3 Device Characterization

The turn on voltage of the micropillar arrays LEDs was found to be around 7 V, which is significantly higher than that of conventional GaN/InGaN mesa LEDs emitting at the same wavelength. This increased turn on voltage is likely due to the high resistivity of the IT p-contact. Figure 5.2.3 shows the electroluminescence (EL) spectra of a green micropillar array LED at different current densities. The peak emission wavelength is located at 550 nm with an unexpectedly broad linewidth of around 60 nm. This broad linewidth is likely due to the each micropillar in the array emitting at a different wavelength, subject to a variety of factors such as diameter, defect density, and current density. As can be seen in Figure 5.2.4, each micropillar in these arrays is not uniformly illuminated, likely due to inconsistency of the PDMS etchback and subsequent quality of the ITO contact layer. As such some array elements appear yellow, while others appear

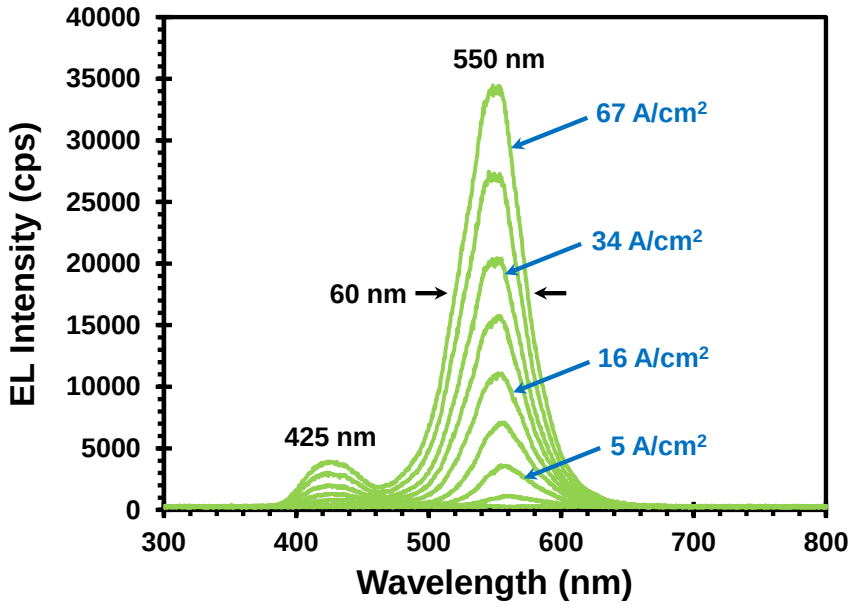

Figure 5.2.3: EL spectra of a micropillar array LED at various current densities, showing a peak emission wavelength of ~550 nm and a linewidth of ~60 nm.

blue. In the case of green emitting quantum wells, higher current densities in micropillars with higher quality ITO p-contacts will experience blueshift, while micropillars with lower current densities will appear redshifted. While the linewidth of an entire array may be 60 nm, the linewidth of an individual micropillar is likely much narrower. The secondary higher energy emission peak at 425 nm visible in Figure 5.2.3 is likely due to population of a second excited state in the QWs at higher current densities.

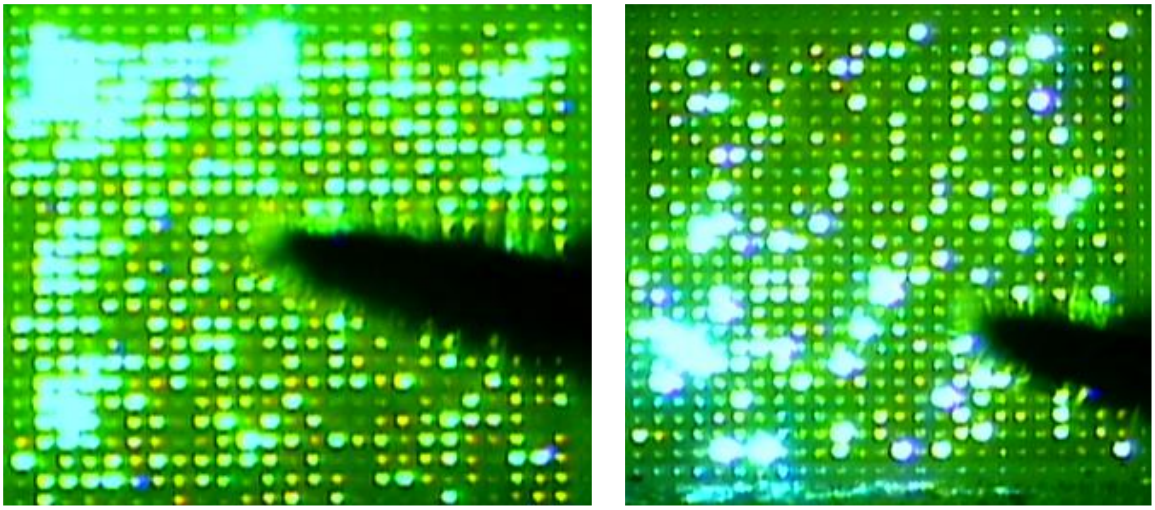

Figure 5.2.4: Optical images of the illuminated nanowire arrays taken using a microscope camera.

5.2.4 Conclusions

These results are quite promising despite the poor emission uniformity across the micropillar arrays. Liftoff of the Ni etch mask using an underlying sacrificial TEOS layer was found to be very effective as a means to increase the brightness of high aspect ratio micropillars. The primary disadvantage of this fabrication approach lies in the use of PDMS as the interlayer dielectric. Planarization and etchback of PDMS, while serviceable, is not ideal, and leads to issues with uniformity and reliability of devices. These issues were

later addressed through development of a TEOS interlayer dielectric process, as described in sections 3.6.2 and 5.5.2. P-contact resistivity could also be improved by using a lower base pressure to sputter the ITO film and optimizing the ITO annealing process.

5.3 Passive Matrix μLED Arrays Emitting at 540 nm

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5.3.1 Introduction

Micro-LED (μLED) displays have seen a massive increase in research interest over the past decade due to their potential to replace both backlit displays and self-lit organic light emitting diode (OLED) displays in applications which require extremely high pixel densities [54–65]. These applications range from high resolution next-gen smart phone displays to near eye displays for alternate and virtual reality (AR and VR) devices [54–65]. The primary advantage of μLED displays over other technologies is their efficiency and lifespan [54,62]. Back/edge-lit displays waste the majority of emitting light, while OLED displays degrade with use because they utilize organic light emitting polymers [66,67]. Semiconductor μLED displays combine the benefits of back/edge-lit and OLED displays, utilizing fully inorganic self-lit pixels which gives them both high power efficiency and very long lifespans, as well as additional benefits such as massively higher switching speeds and improved thermal stability. While μLEDs seem like the ideal replacement for existing high-resolution display technologies, there are many practical hurdles inhibiting their development. These include a complex fabrication process, low external quantum efficiency due to surface losses scaling inversely with device size, and difficulty in combining red, green, and blue emitters into an RGB display [61–63].

Existing fabrication approaches for RGB μLED displays tend to rely on either a combination of GaN based blue and green emitters, and AlInGaP based red emitters [54,61–63], or on phosphor down-conversion to convert two thirds of the pixels in a

natively blue emitting GaN display to red and green [54,55,58]. The first approach requires use of a pick-and-place technique, in which individual pixel elements are placed on a thin film transistor (TFT) backplane. This technique is inherently through-put limited and has poor yield, which often necessitates the use of redundant pixels, driving up fabrication costs and severely limiting the scalability of this method. The second approach allows for the theoretical use of a monolithic blue emitting GaN display, with some pixels converted to green and red emission by application of phosphors [68–70]. In a monolithic GaN display, current leakage between pixels is an issue due to challenges in growing truly intrinsic, insulating u-GaN [71–78]. In a basic m x n passive matrix array with m rows and n columns, m + n control signals are used to address the elements of the display. In a setup in which LED p-contacts are addressed by row signals (m) and n-contacts are addressed by column signals (n), failure to properly isolate each column of pixels from one another will lead to current leakage between columns through the n-GaN. It is very difficult to grow "intrinsic" undoped-GaN (u-GaN), and this material tends to end up moderately n-doped, giving it non-negligible conductivity [79]. As such, even growing a u-GaN layer beneath the n-GaN and etching through the n-GaN into this u-GaN in an attempt to isolate the pixels will still allow for significant current leakage between all pixels addressed by the active row. The consequence is that all pixels in a single row will illuminate at the same time, albeit not at the same intensity as the addressed pixel.

In lieu of the ability to effectively isolate devices using a buried u-GaN layer, two alternate isolation approaches are possible. The first involves growing a buried p-GaN layer beneath the n-GaN, forming a PN junction which opposes the flow of leakage current between adjacent n-GaN regions. While this approach is effective, it requires activation of

the buried p-GaN layer *after* the isolation etch so that Mg passivating hydrogen can diffuse out through the etch sidewalls [80–83]. Mg activation becomes less effective as device dimensions increase, due to increased out-diffusion path lengths for hydrogen. The second approach is to simply etch completely through the GaN LED epi all the way to the substrate [75–78,84]. Most GaN is grown on sapphire, an excellent insulator, so a through-epi etch fully eliminates leakage between pixel columns. However, in order to obtain low defect densities in the LED active region, the GaN epi must be grown fairly thick to allow for termination of screw dislocations. As such, an isolating through-epi etch must generally be at least several microns deep. If high pixel densities are desired, this necessitates the use of deep, high aspect ratio isolating "trenches." In order to connect the p-contacts in a row of pixels, a conductive trace must bridge this deep, high aspect ratio trench. This process is difficult for a number of reasons. Even if conformal metal deposition is used, it may not fully coat into the bottom corners of a deep trench, especially if the trench has an aspect ratio (depth/width) > 1. If metal coating is not in issue, patterning of the metal, either through metal etching or liftoff becomes a problem as it is difficult to fully expose photoresist at the bottom of high aspect ratio features. Several approaches, such as tiered isolation etches or sloped trench sidewalls have been used to mitigate these issues[75,77], however these approaches increase the footprint of the device which is undesirable when high pixel densities are desired.

In this work, we introduce a novel fabrication process which enables reliable bridging of deep, high aspect ratio isolation trenches for InGaN/GaN μLED arrays. As first described in our previous work [85], this is accomplished by coating and patterning a photoresist layer such that resist is left only within the trenches between μLED columns.

This resist layer is then baked at 250°C for 30 minutes to completely cross-link and carbonize it, making it fully resistant to most etch chemistries and common solvents such as isopropanol, acetone, and n-methyl-2-pyrrolidone (NMP). This photoresist coating, patterning, and baking process is repeated several times until the carbonized resist layer is level with edges of the trenches, allowing for metal interconnects to be deposited across the trenches via liftoff or metal etching without any need for step coverage. Here, we demonstrate 4x4 and 10x10 passive matrix InGaN/GaN μLED arrays with pixels as small as 10 μm emitting at a wavelength of ~520 nm using this technique, and show that n-contact current leakage can be reduced into the femto-amp range by trenches as narrow as 30 μm with depths of ~6.5 μm. We also show that the interconnects formed over photoresist planarized trenches do not exhibit increased resistance compared to those deposited on control samples, indicating that use of photoresist as a planarizing material does not lead to increased p-trace resistivity. This novel fabrication approach could aid in the creation of monolithic μLED displays and other devices in the GaN materials system which utilize deep trench isolation to prevent current leakage.

5.3.2 μLED Array Fabrication

Passive matrix displays were fabricated on green-emitting InGaN/GaN epi grown on 50 mm diameter, 430 μm thick sapphire wafers using metal organic chemical vapor phase epitaxy (MOVPE). The epistructure consisted of a 20 nm AlN buffer following by 3 μm u-GaN, 3 μm n-GaN, a 3 period InGaN/GaN superlattice, an 8 period InGaN/GaN MQW (2.5 nm $In_{0.19}Ga_{0.81}N$ QWs), 150 nm p-GaN, and 1 nm p-InGaN to improve contact

resistance. A simplified version of this epistructure is shown in Figure 5.3.1, displaying only n-GaN, MQW, and p-GaN layers. The fabrication process began with patterning of the mesa etch mask using 405 nm laser direct write (LDW) lithography, as shown in Figure 5.3.1(a). The resulting 1500 nm thick, patterned AZ1512 photoresist was used to mask a 530 nm deep $Cl_2/BCl_3/Ar$ etch consisting of 32/8/5 sccms $Cl_2/BCl_3/Ar$ with 75/225 W RF/ICP power at a pressure of 10 mtorr to form the µLED mesas (Figure 5.3.1(b)). Mesas were patterned to have dimensions of 10, 30, 60, or 120 µm. This photoresist mask was then removed using a combination of acetone and ashing (Figure 5.3.1(c)). LDW was then used to pattern AZ1512 on LOR 5A to allow for liftoff of the p- and n-metal contacts. The p-metal contact was deposited first, and consisted of 60 nm of electron beam evaporated Ni. The p-metal was annealed in O_2 at 550°C for 2 minutes. Following p-metal annealing, the n-metal contact, consisting of 20/45/50 nm Ti/Al/Ni was deposited, also via electron beam evaporation, and annealed in N_2 at 650°C for 2 minutes (Figure 5.3.1(d)).

Following completion on the metal contacts and initial testing of the LEDs, 1100 nm of tetraethyl orthosilicate (TEOS) was deposited via plasma enhanced chemical vapor deposition (PECVD) to act as an etch mask for the trench isolation etch. This thick TEOS layer was pattered using LDW of AZ1512 on LOR 5A, and etched using a 70/60/6 sccm $CF_4/CHF_3/O_2$ dry etch at 200 W RF power and a pressure of 130 mtorr. The long duration of this etch and insulating nature of the sapphire substrate caused significant heating of the photoresist, causing it to crosslink and "burn." The underlying LOR layer ensured easy removal of this burnt resist in NMP (Figure 5.3.1(e)). Following patterning of the TEOS trench-etch mask, the aforementioned $Cl_2/BCl_3/Ar$ dry etch was used etch through the epistack to the sapphire at an etch rate of ~500 nm/min. This etch was performed for 25

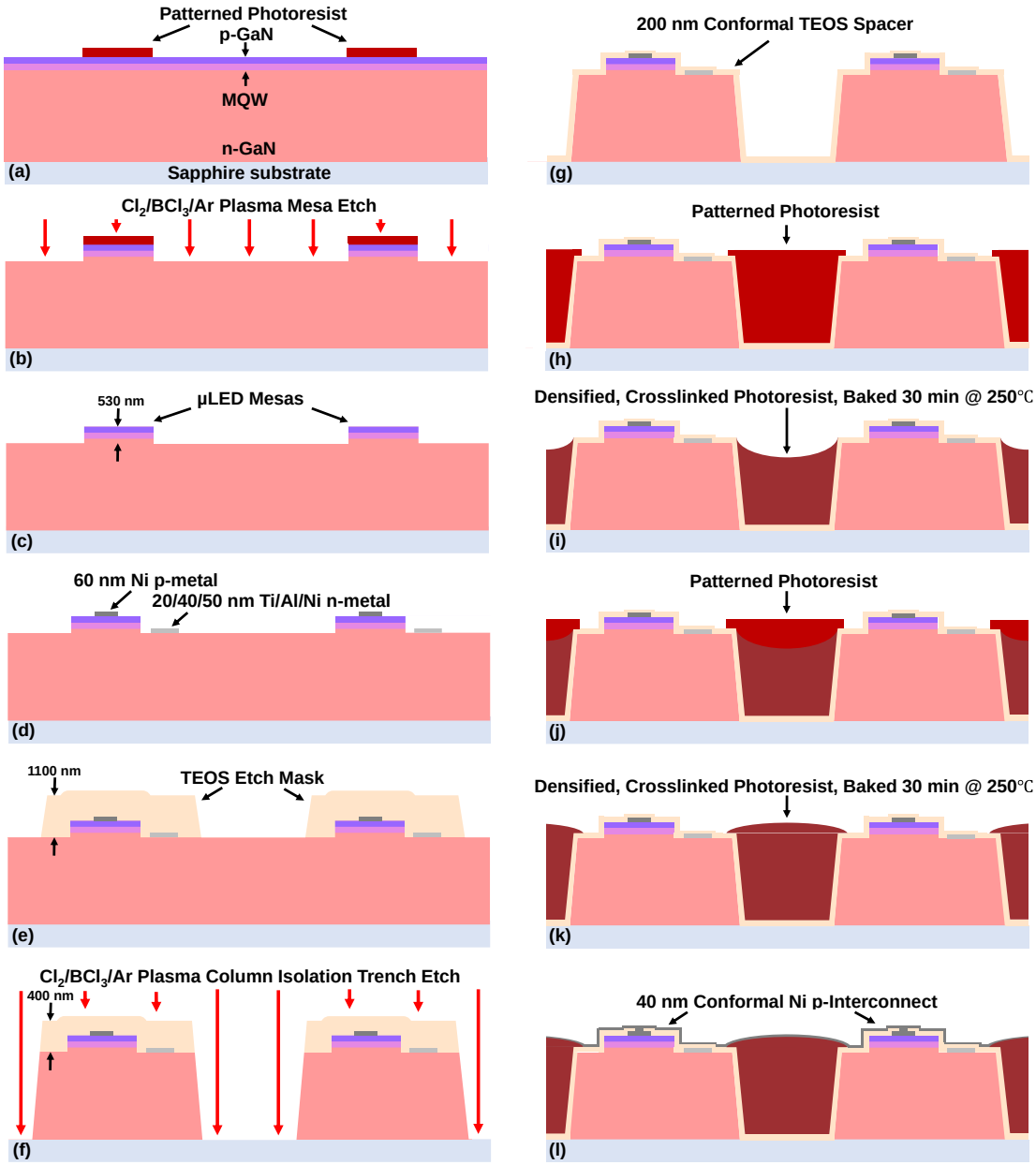

Figure 5.3.1: Cross sectional schematic of the passive matrix display fabrication process, showing a cross section of two pixel elements parallel to the direction of the p-interconnect. In this view the n-interconnect extends into the screen. (a) Patterning of the mesa etch mask, (b) dry etching of the mesas (~ 530 nm in height), (d) formation of the n- and p-metal contacts, (e) patterning of the 1100 nm thick TEOS trench etch mask, (f) etching of the column isolation trench, (g) deposition of the 200 nm thick conformal TEOS spacer layer, (h,j) patterning of the trench fill photoresist, (i,k) planarization of the trench fill photoresist, and (j) deposition of the conformal, 40 nm thick p-interconnect.

min to ensure complete removal of all GaN and AlN and exposure of bare sapphire. This etch reduced the TEOS etch mask to a thickness of 400 nm from its previous 1100 nm, indicating a TEOS etch rate of ~28 nm/min (Figure 5.3.1(f)). A wet etch was then performed in 40% AZ400K (a photoresist developer containing 2 wt% KOH) at 80°C for 30 min to remove dry etch damage as well as any GaN/AlN remaining at the bottom of the trenches which could enable unwanted current leakage. The remaining 400 nm of TEOS was then removed using a 5 minute etch in 10:1 BOE.

Following removal of the TEOS etch mask, an additional, passivating TEOS layer was conformally deposited to a thickness of 200 nm via PECVD to prevent shorting of the p-interconnect metal to the n-contact and n-GaN (Figure 5.3.1(g)). AZ1512 photoresist was then coated and patterned using LDW, such that it remained only within the trenches (Figure 5.3.1(h)). This resist was then baked at 250°C for 30 min, ensuring the removal of all solvents and forming a crosslinked, densified, carbonized polymer which is completely inert in all (unheated) solvents and most etch chemistries such as HF, HCl, etc. During the first few minutes of this high temperature bake, the photoresist "reflows" and the lithographically defined pattern loses edge definition, with resist flowing to an equilibrium position where it wets to the trench sidewalls. During this process, the volume of the resist is reduced, leading to the cross section shown in Figure 5.3.1(i). This process of coating, patterning, and baking photoresist is repeated twice more to thoroughly planarize the trenches, resulting in the cross section shown in Figure 5.3.1(k). Repetition of this process eliminates slope discontinuities between the n-GaN and filled trench, improving the reliability of subsequent lithography and metallization steps. Following trench planarization, AZ1512 on LOR 5A is patterned using LDW and a contact open etch is

performed over the p-contacts and n-metal pads using the aforementioned $CF_4/CHF_3/O_2$ etch. LOR is again used here to aid in removal of burnt resist as a precautionary measure. After this resist is stripped in NMP, AZ1512 and LOR 5A are again patterned via LDW and used to lift off a conformally deposited 40 nm thick Ni layer which forms the trench bridging p-interconnects (Figure 5.3.1(l)). Figure 5.3.2 shows a layout view of a 4x4 display (top) and an enlarged view of a single pixel element (bottom). µLED mesas are

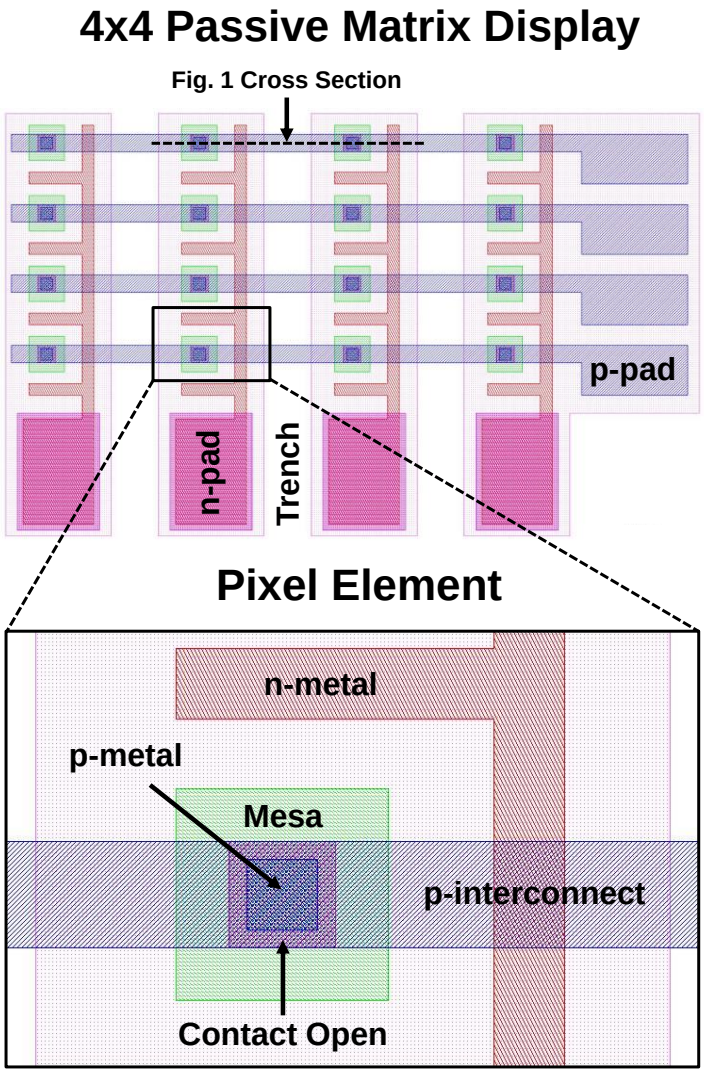

Figure 5.3.2: Layout view of a 4x4 passive matrix array (top) and an enlarged view of a single pixel element of the display (bottom). The location of the cross section described in Figure 5.3.1 is shown in the top center of the 4x4 display at top.

shown in green, n-metal in red, p-metal in blue, p-interconnects in purple, and contact opens in pink. The position of the cross section used in Figures 5.3.1(a-l) is represented by a dashed line bisecting two pixels in the top part of Figure 5.3.2. To better illustrate the sizes of these devices, Figure 5.3.3 shows images of a passive matrix display sample at the

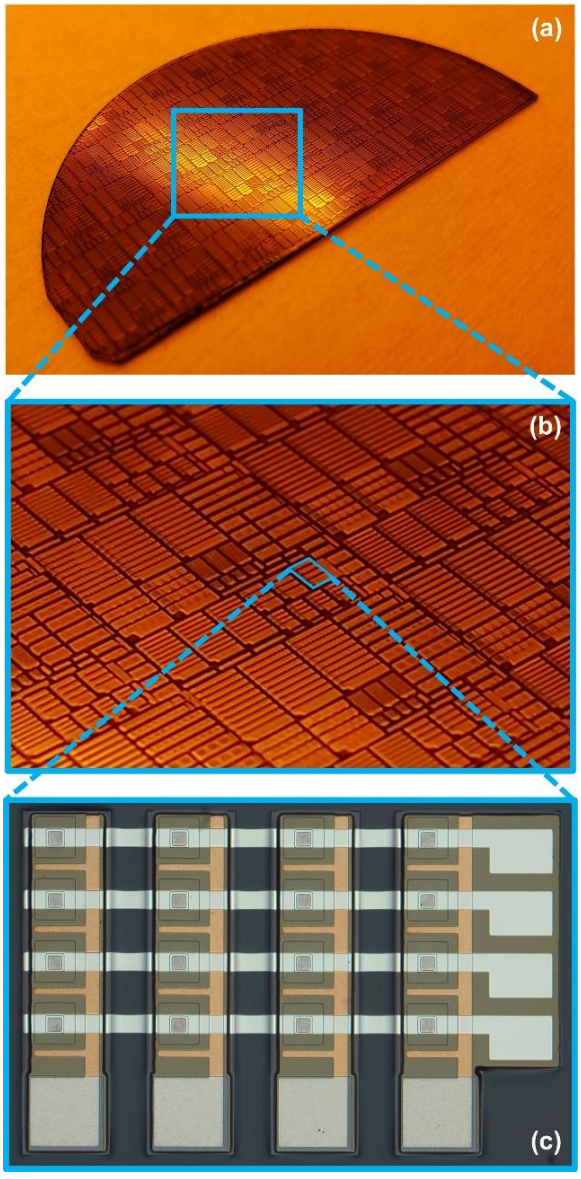

Figure 5.3.3: Images showing the passive matrix display samples at the wafer level (a), the die level (b), and the device level (c). The shown device is a 4x4 display with a pixel size of 60 µm and x/y pixel pitches of 180/90 µm.

wafer level ((a), 1/2 of a 2-inch wafer), the die level ((b), die area 25 mm^2), and the device level (c). The device shown in Figure 5.3.3(c) is a 4x4 display with 60 um pixels on an x pitch of 180 µm and a y pitch of 90 µm, with a trench width of 50 µm. The larger x pitch is necessary to allow for a wide trench to be used, but could be reduced to be more in line with the y pitch given additional optimization of the trench etch and reduction in trench width to < 10 µm. In addition to the device highlighted in Figure 5.3.3(c), 4x4 and 10x10 displays with 10, 30, 60, and 120 µm pixels were fabricated. The x pitch/y pitch/trench width of 10, 30, 60, and 120 µm devices are, in order, 65/25/20 µm, 130/30/40 µm, 180/90/50 µm, and 280/70/60 µm.

Figure 5.3.4 shows scanning electron microscope (SEM) images of various displays. Figures 5.3.4(a-b) show a 4x4 10 µm display after the KOH etch and prior to removal of the masking TEOS. The vertical height of the features shown in these images is ~6.5 µm. Figure 5.3.4(c) shows the same 4x4 display following a single planarization step. It is clear from this image that even a single planarization step is nearly sufficient to achieve full planarization of the trenches. Figures 5.3.4(d-h) show completed devices, showing both the p-interconnect metal and fully planarized trenches. Figures 5.3.4(f-h), imaged at 80° off normal, highlight the profile of the planarizing photoresist. The overlap of the hard-baked resist and the n-GaN region is easily seen in these images. This allows the p-interconnect metal to drop directly onto the n-GaN surface without interaction with the edge of the trench. As opposed to the simplified concave down surface shown in Figure 5.3.1(j), the curve of the resist surface appears to have three critical points, a global minimum in the center of the trench, with a thickness slightly less than the depth of the trench, and two symmetric global maxima around 5 µm outside the trench over the n-GaN.

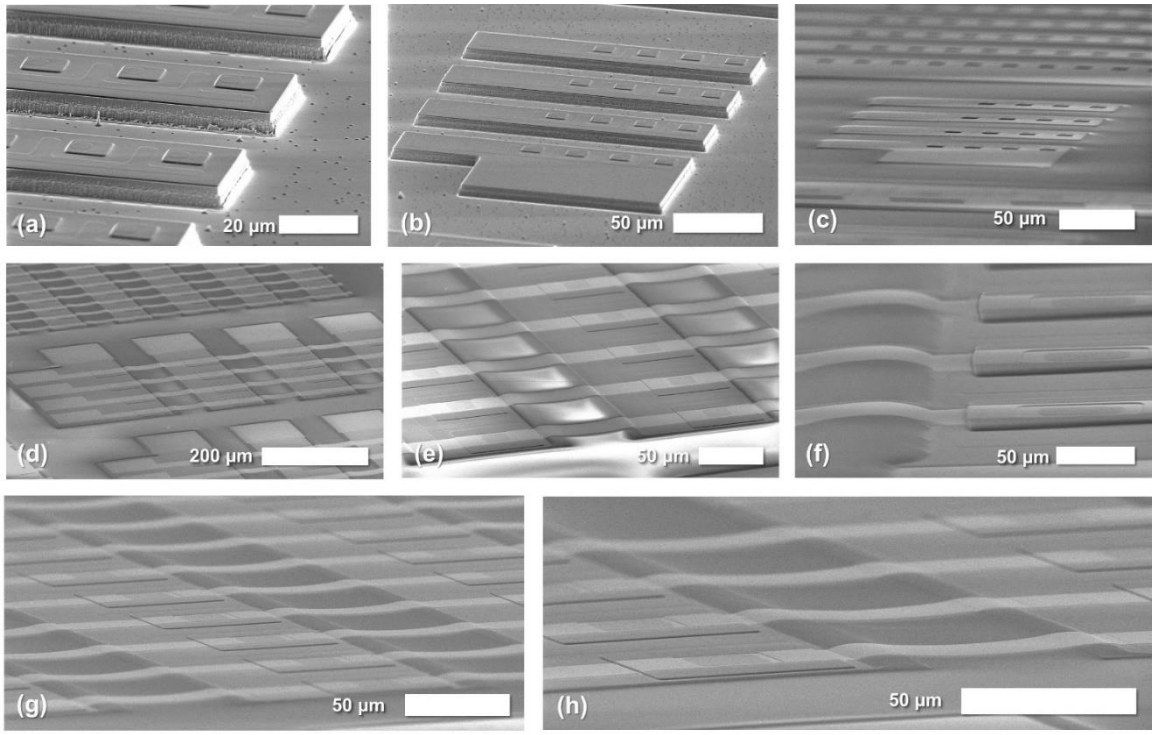

Figure 5.3.4: SEM images showing passive matrix displays prior to trench planarization (a,b), following trench planarization (c), and following p-interconnect formation (d-h). (a, b, d, and e) are imaged at 70° off-normal, while (c, f, g, and h) are imaged at 80° off-normal.

This continuous surface, which lacks any discontinuities, enables improved coverage by the p-interconnect metal and more reliable electrical performance. Early iterations of these devices utilized only a single planarization step, which resulted in a cross-sectional profile similar to that shown in Figure 5.3.1(i). This was found undesirable as the insufficient step coverage of sharp corners lead to increased series resistance and sometimes shorting of the p-intereconnect to the n-GaN.

5.3.3 Device Characterization

Completed devices were first tested to characterize leakage current, as low leakage is essential for realizing functional trench isolated passive matrix displays [73–76,84]. Current leakage across trenches was characterized by applying a 0-30 V sweep across the

n-contacts of adjacent test devices separated by trenches of variable width. Figure 5.3.5 (inset) shows the current-voltage (I-V) characteristics across a 40 µm wide trench. The average leakage current is ~ 600 fA, which is effectively at the noise floor of our measurement tool, a Keysight B1500A parameter analyzer. This indicates that a trench of this width was effective at fully isolating adjacent devices from one another. Figure 5.3.5 shows the average leakage current as a function of trench width. A slight trend indicates that leakage current is inversely proportional to trench width, with leakage increasing from ~520 fA at 100 µm to 610 fA at 30 µm. This trend is insignificant enough to have no practical effect on device performance.

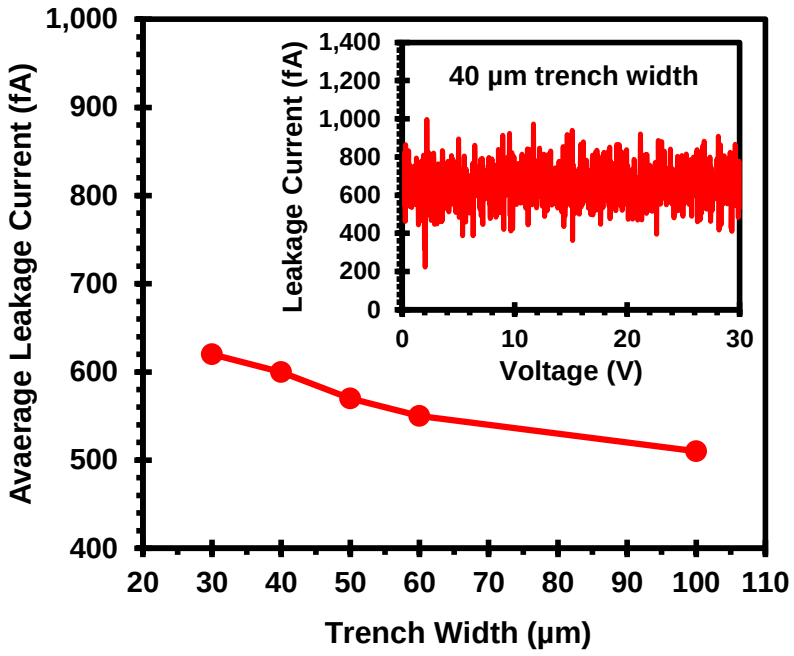

Figure 5.3.5: Leakage current as a function of trench width. (inset) Leakage current as a function of applied bias for a 40 µm wide trench.

The I-V characteristics of 10 µm, 30 µm, and 60 µm devices are shown in Figure 5.3.6(a). Threshold voltage is moderately lower for larger devices, with the average being around 3 V. Post-threshold characteristics are series resistance dominated, and could be improved by reducing the resistivity of the p-interconnect metal as well as improving the

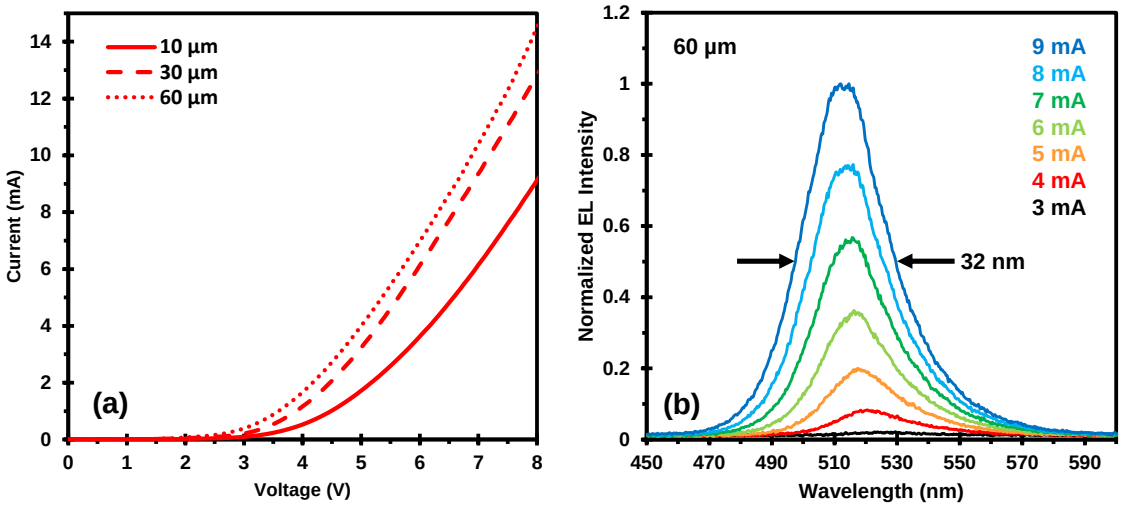

Figure 5.3.6: (a) Current voltage characteristics for 10, 30, and 60 µm µLEDs. (b) Electroluminescence spectra of a 60 µm µLED driven at between 1 mA and 9 mA, showing peak emission at ~515 and a FHWM of ~32 nm.

quality of the epitaxial p-GaN layer. Trenches, and the number of trenches crossed by the p-interconnect, were found to have no effect on I-V characteristics of devices, with identical interconnects deposited across photoresist planarized trenches and on TEOS control surfaces having identical resistances. This indicates that our photoresist planarization process is an effective means of filling isolation trenches without impacting device performance. Figure 5.3.6(b) shows the electroluminescence (EL) spectra of a 60 µm pixel at drive currents from 3 - 9 mA. A uniform increase in peak EL intensity is observed for each 1 mA increase in drive current. The full width half max (FWHM), or linewidth of emission was ~ 32 nm, with an emission peak centered around 515 nm.

Blue shifting of the emission spectra is observed, as expected, as drive current density is increased, as shown in Figure 5.3.7(a). When the 60 µm pixels in Figure 5.3.7(a) were driven at 10 V, a blue shift of 13 nm from 517 nm to 530 nm was observed when increasing drive current from 1 mA (27 A/cm^2) to 30 mA (830 A/cm^2). This blueshift is expected as increased current densities populate energy levels further from the band-edge, leading to higher energy, shorter wavelength recombination events which decrease the average wavelength of emitted photons. EL intensity was also found to increase with pixel size as expected, and a slight blueshift of 6 nm from 517 nm to 511 nm was observed between the 120 µm and 30 µm devices (Figure 5.3.7(b)). This blueshift is due to increased current density of 1110 A/cm^2 in the 30 µm pixel, as opposed to 70 A/cm^2 in the 120 µm pixel. Figure 5.3.8 shows the conversion of the 60 µm device spectra shown in Figure 5.3.7(a) into the CIE 1931 color space. At a drive current/current density of 5 mA/140

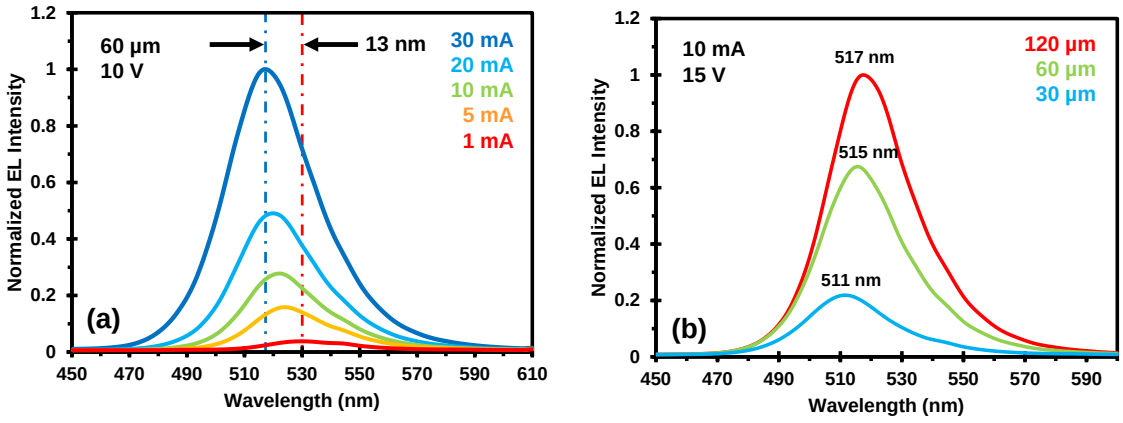

Figure 5.3.7: (a) Blueshift characteristics for a 60 µm µLED driven at 10 V and 1-30 mA. A blueshift of 13 nm is observed when drive current is increased from 1 mA to 30 mA. (b) Size dependent EL characteristics for devices driven at 10V and 10 mA. A moderate blueshift of 6 nm is observed between the 30 µm and 120 µm µLEDs.

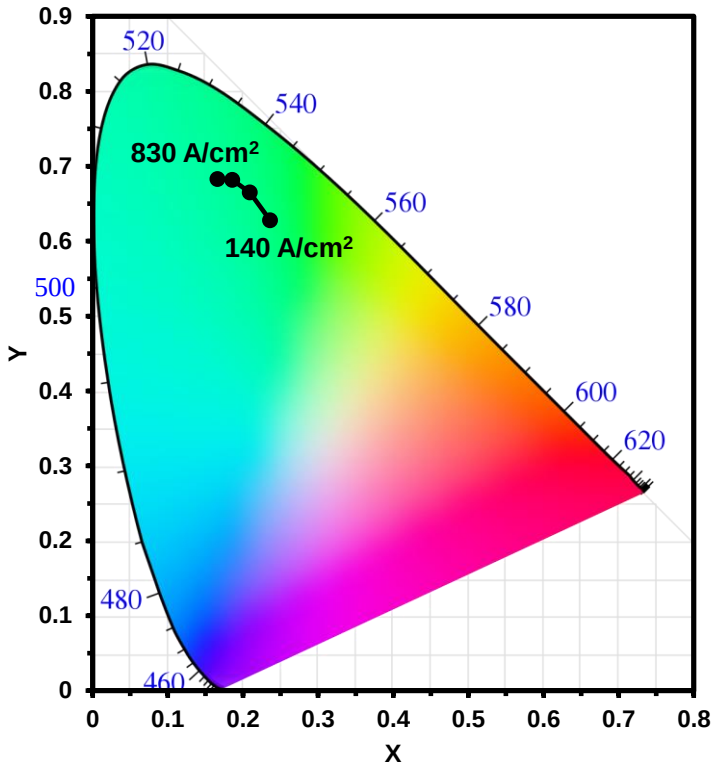

Figure 5.3.8: CIE 1931 coordinates of 60 µm devices driven between 140 A/cm^2 and 830 A/cm^2.

A/cm^2, the CIE 1931 coordinate is (0.236, 0.628). As current is increased to 30 mA/830 A/cm^2, this coordinate changes to (0.166, 0.683) in line with the blueshift observed in Figure 5.3.7(a).

Figure 5.3.9 shows images of a 4x4 passive matrix display with pixel dimensions of 60 µm and an x pitch/y pitch/trench width of 180/90/50 µm, captured through a 10x objective lens. In Figure 5.3.9(a-c), single pixels are driven at 10 mA by applying 10 V to the p-interconnect pad (anode, right end of each row), while the corresponding n-interconnect pad (cathode, bottom of each column) is held at ground. This approach allows any pixel in the display to be illuminated, and if these devices were diced and wire-bonded, an 8-channel driver could be used to rapidly turn on/off pixels in the display,

allowing for “image” formation. In (d-f), columns are driven at 25 mA and illuminated by holding their cathode at ground while applying 20 V to the cathode of an adjacent column. This approach allows for illumination of 4 pixels (an entire column) simultaneously by reverse biasing the column to which 20 V is applied, allowing current to flow in reverse through the pixels of this column, into the p-interconnect, and through the forward biased, illuminated column. 10x10 and 4x4 arrays of 10 µm, 30 µm, 60 µm, and 120 µm pixels were fabricated and tested successfully, but are not included in Figure 5.3.9 for compactness. These devices

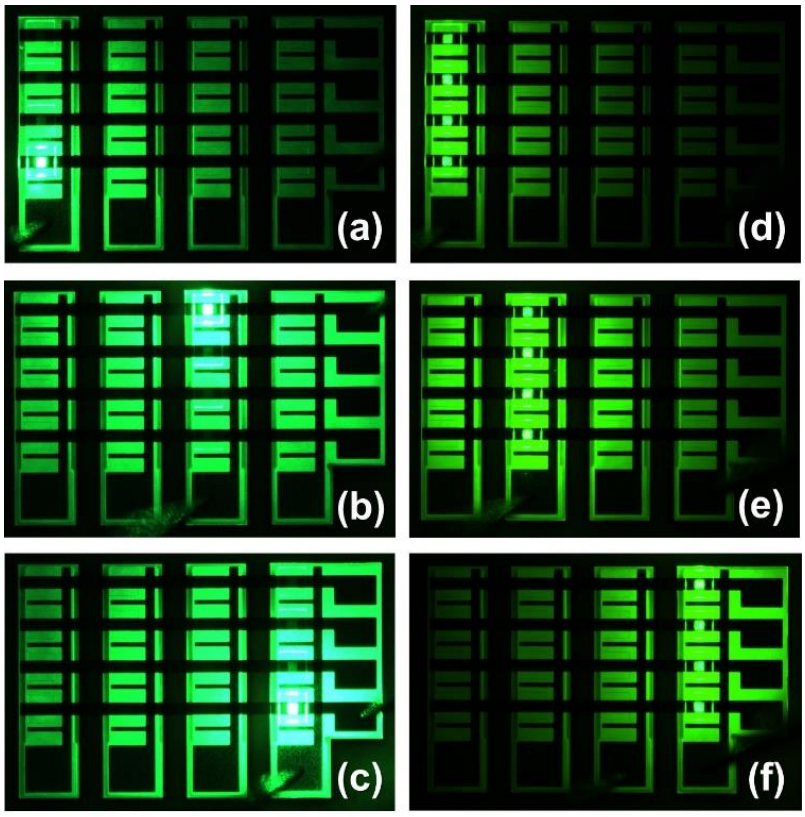

Figure 5.3.9: Illuminated µLEDs in a 4x4 passive matrix display. µLEDs have dimensions of 60 µm, with an x pitch/y pitch/trench width of 180/90/50 µm. In (a-c), single pixels are driven at 10mA by applying 10 V to the p-interconnect pad (anode), while the corresponding n-interconnect pad (cathode) is held at ground. In (d-f), columns are driven at 25 mA and illuminated by holding their common anode at ground while applying 20 V to the anode of another column. This reverse-biases the column to which 20 V is applied, and increases the turn on voltage of the grounded column.

are much smaller than those which are typically referred to as “displays,” which usually have dimensions of dozens to hundreds of pixels on a side, and were designed this way in order to maximize yield and provide as many testable devices as possible for characterizing the effectiveness of our photoresist planarization process. The preceding results demonstrate the effectiveness of photoresist planarized trench isolation as a means to electrically isolate device arrays fabricated monolithically in GaN.

5.3.4 Conclusions

This work demonstrates the fabrication of monolithic InGaN/GaN single color passive matrix μLED displays using photoresist planarized trench isolation to electrically isolate columns of pixels driven by a common n-GaN anode. This method was shown to be extremely effective at eliminating leakage current and preventing unwanted illumination of adjacent pixels. As opposed to isolation approaches which utilize a buried p-GaN layer to create a PN junction at the bottom of the n-GaN layer, this method can be applied easily to larger devices in which activation of a buried p-GaN layer is difficult or impossible. The fabricated displays were shown to emit at wavelengths between 510 and 530 nm with a linewidth of 32 nm, with turn on occurring around 3 V. Blue-shifting was observed in single pixels as drive current/current density was increased, and between different pixel sizes under equivalent drive currents. This fabrication approach for electrical isolation of device arrays formed monolithically in GaN could allow for advancement of display technologies based around use of monolithic RGB emitting displays utilizing a trench isolation approach. In addition, this process could prove useful in the fabrication of other III-V and Si devices which host high aspect ratio features which require bridging by conductive interconnects.

5.4 Nanowire Quantum Dot Single Photon Emitters

Published as "Melanson et al, Conference on Lasers and Electro-Optics, 2020" [86]

5.4.1 Introduction

Single photon sources based on III-Nitride quantum dots (QDs) emitting within the visible spectral range are promising candidates for quantum information technologies such as quantum computing, communications, and cryptography [87]. As research into quantum photonic technologies accelerates over the coming decades, high quality single photon sources capable of operation at room temperature will be of critical importance. In contrast to conventional single photon emitters, which are usually based on non-deterministic down conversion of photons using non-linear optical materials, III-nitride quantum dots, could potentially emit deterministic single photons at room temperature and allow for scalable fabrication of emitter arrays [87–90]. While single photon emission from epitaxially grown III-nitride nanowire quantum dots has been demonstrated, the linewidths of the emission spectra for these devices are typically very large at room temperature, making deterministic emission of identical single photons nearly impossible [88,90,91]. This issue arises primarily from poor carrier confinement and quantization of energy levels within the quantum dots due to their relatively large dimensions, on the order of several tens of nanometers [87]. To narrow the emission linewidth of larger quantum dots, it is necessary to cool them to cryogenic temperatures in order to suppress or eliminate spectral diffusion and other thermally dependent linewidth broadening mechanisms. While this is easily achievable with modern cryostats, use of cryogenic cooling systems is highly undesirable in practical applications in which scalability and operating cost must be considered.

An alternate approach for reducing emission linewidth may be to shrink the diameter of the nanowire towards the single nanometer regime in order to further confine the charge carriers in the quantum dot and quantize the energy levels available to charge carriers in the valence and conductions bands. Our previous work has explored methods of anisotropically etching GaN nanowires using a heated KOH-based solution with extremely high selectivity against the non-polar crystal planes in wurtzite-GaN [92]. We have demonstrated the ability to shrink the diameter of c-plane GaN nanowires with a starting diameter of 150 nm down to as small as 20 nm with no corresponding loss in height, as the etch rate of the exposed c-plane at the top of the nanowire is effectively negligible [92]. In this work, we show the preliminary results of a study which applies our previous research on KOH-wet etching of GaN nanowires to produce nanowires with diameters in the sub-20 nm range with room-temperature optical characteristics for potential use as single photon emitters.

5.4.2 Nanowire Fabrication Process

A schematic of the fabrication process for the InGaN/GaN nanowires is shown in Figure 5.4.1. Here, nanosphere lithography is used to mask the initial dry etch of the nanowires. An aqueous solution of 150 nm SiO_2 nanospheres is diluted to the desired concentration and spin-coated onto the InGaN/GaN epi-stack (Figure 5.4.1(a-b)). A Cl_2-based reactive-ion-etch is then used to form the initial nanowire structure using the SiO_2 spheres as a low-selectivity etch mask (Figure 5.4.1(c)). The resulting nanowires have normal taper profile as shown in Figure 5.4.1(d). These structures are then immersed in 40% AZ400K heated to 80 °C for approximately 70 minutes, in order to reduce the

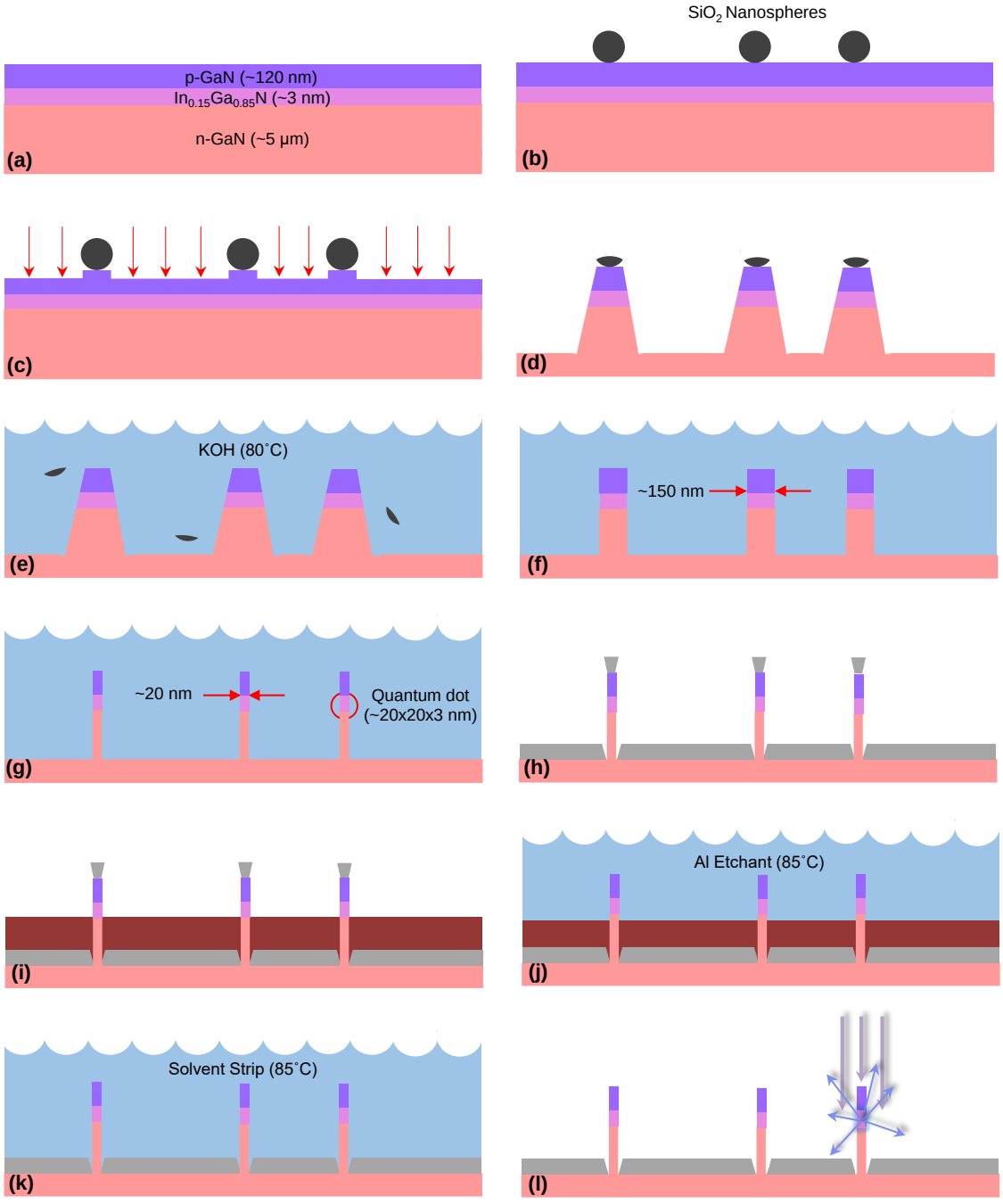

Figure 5.4.1: Nanowire QD SPE fabrication schematic (not to scale).

diameters of the nanowires to around 20 nm (Figures 5.4.1(e-g)). Figure 5.4.2(a) shows an SEM image of a nanowire following the dry etch, with a top diameter of around 150 nm, while Figure 5.4.2(b) shows the same nanowire following a 70 minute etch in the heated AZ400K solution, with its diameter reduced to around 20 nm. Following the wet etch, 100 nm of Al was deposited using thermal evaporation to screen the substrate and prevent emission from Ga defect states (Figure 5.4.1(h)). A 150 nm layer of polymethyl methacrylate (PMMA) was then spin coated onto the sample to mask the substrate metal (Figure 5.4.1(i)) before the sample was subjected to a Al wet etch at 85°C for around 2 min to remove the Al from the tips of the nanowires (Figure 5.4.1(j)). The PMMA was then stripped using acetone (Figure 5.4.1(k)) and rinsed in DI water before being dried with nitrogen and readied for testing (Figure 5.4.1(l)). This top-down fabrication approach avoids the primary issues of bottom-up epitaxial nanowire growth in that it is both more

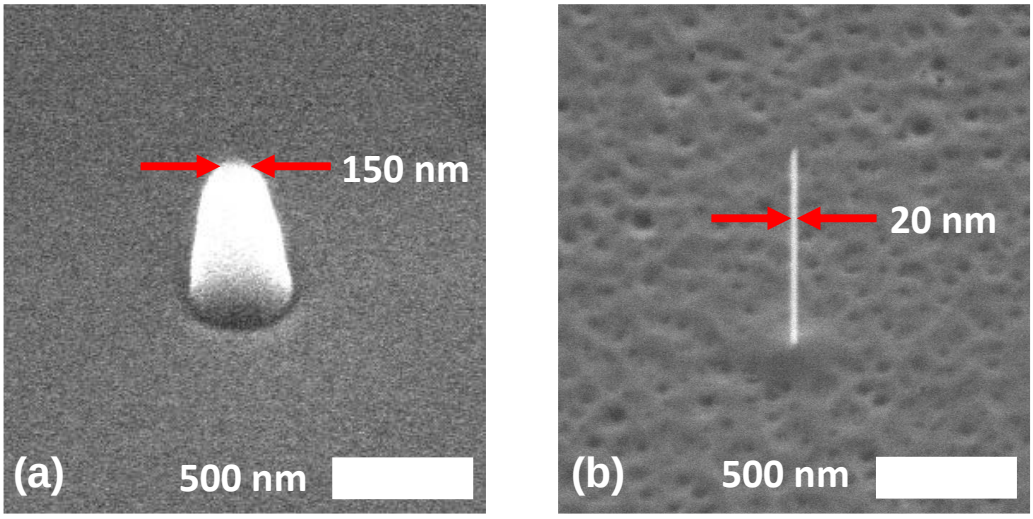

Figure 5.4.2: SEM images showing a nanowire after dry etch (a) and after 70 min in 40% AZ400K (b).

cost effective and allows nanowire site-control without the need for expensive selective area epitaxy.

5.4.3 Emitter Characterization

To test the optical properties of these QD nanowires, we used a custom-built micro-photoluminescence (μPL) system capable of optically exciting and imaging individual nanowires. Optical excitation with a 405 nm continuous wave laser revealed the power and diameter dependent emission characteristics of the nanowire QDs. We found that larger nanowires (~100 nm) which had not been subjected to extensive KOH etching showed broader emission peaks centered around 440 nm, while smaller nanowires (~20 nm) formed through extended KOH etching emitted narrower spectra with PL peaks blue shifted down to ~418 nm. These results are consistent with the well-studied behavior of energy

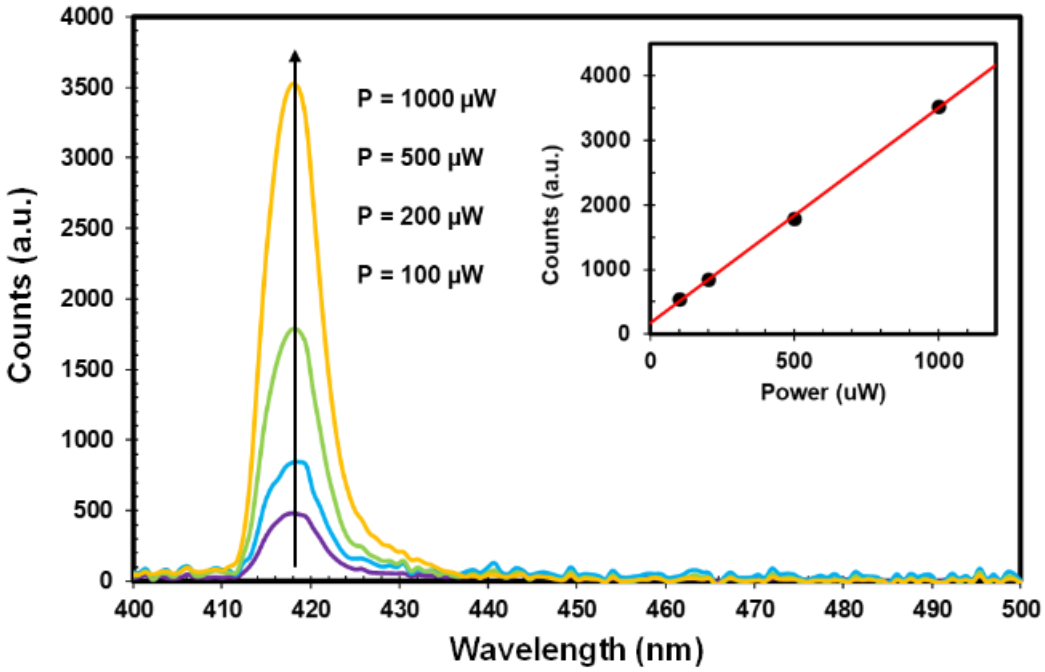

Figure 5.4.3: Power dependent PL spectrum of a single nanowire QD. Inset shows the linear dependence of emission intensity on pump laser power.

eigenstates in InGaN/GaN nanostructures, with enhanced physical confinement of the QD region leading to improved separation of available energy states and a corresponding blueshift of all allowed electron-hole transition energies. The power-dependent PL spectra of a representative 20 nm nanowire are shown in Figure 5.4.3. The full width at half maximum (FWHM) of each emission peak is approximately 7.1 nm, and the emission peak intensity shows near perfect linear dependence on excitation power. As can be seen in Figure 5.4.3, these emitters exhibit excellent signal to noise ratio even for relatively low excitation powers down to 100 μW at room temperature, in stark contrast to the spectra of previously demonstrated room-temperature InGaN/GaN single photon emitters [88,90].

5.4.4 Conclusions

The demonstrated InGaN/GaN nanowire QDs show great potential for use as scalable, room-temperature single photon emitters with narrow emission linewidths. The well-developed top-down process used to fabricate the nanowires could also allow for straightforward electrical excitation of single photon emission, the “holy grail” of quantum emitters still very much in its infancy [89,93–95]. This fabrication process could also allow for QD site control, enabling integration with on-chip photonic circuitry.

5.5 SiO_2 Nanosphere Arrays for Light Out-Coupling

Unpublished work (2019)

5.5.1 Introduction

UV LEDs offer many advantages over conventional UV light sources such as mercury vapor arc lamps, most notably enhanced lifetime, switching time, durability, and environmental compatibility [96–98]. UV LEDs can also be produced in small form factors, making them much more portable and easier to integrate into complex systems [96–98]. UV light has found use in many applications, including water purification, surface sterilization, biosensing, photolithographic microfabrication, resin curing for 3D printing, and many others [96–107]. Despite the effectiveness of UV light in these various roles, UV LEDs have not yet seen widespread commercial adoption due primarily to their low external quantum efficiencies (η_{EQE}). The inability of modern UV LEDs to match the efficiencies of other emitters such as blue LEDs makes it difficult for them to compete with conventional UV light sources in terms of power output [96]. The low external quantum efficiencies of UV LEDs can be attributed primarily to their poor light extraction efficiency (η_{EXT}), which is often less than 10%.

Extensive research has been focused on improving light extraction from LEDs over the past few decades, with most research efforts concerned primarily with visible wavelength LEDs. Random surface roughening [108], substrate patterning [98,104], diffraction gratings [109], photonic crystals [110], nanowires [107], microlens arrays [111-117], and laser direct writing of microholes [118] have all been investigated as means to enhance η_{EXT} from visible light LEDs, often with very promising results. Some of these

approaches have also been applied to UV LEDs, for example, nanowires and photonic crystals have been investigated as means to improve η_{EXT} from the top of UV LEDs primarily via top-down etching approaches [97,103], and while these methods have been found fairly effective, they require many additional fabrication steps. Some research groups have achieved UV LEDs with η_{EQE} values greater than 20% by utilizing a complex, comprehensive fabrication approach which addresses multiple factors affecting η_{EXT}. For example, Takano *et al.* achieved 20.3% η_{EQE} for an LED emitting at 275 nm by utilizing a patterned sapphire substrate, transparent p-contact layer, mirror-like p-contact electrode, and resin encapsulation [104]. While these results are promising, the inclusion of many additional, specialized fabrication steps to enhance η_{EXT} make the fabrication of these devices unsuitable for profitable high-volume manufacturing. The use of self-aligned nanosphere arrays has been shown to enhance the total light extraction efficiency of LEDs emitting in the visible range [115,117], however this approach has not yet been applied to UV LEDs.

In this work, we propose a simple approach for producing moderate improvements to the η_{EXT} of 280 nm AlGaN multiple quantum well (MQW) UV LEDs. This approach utilizes self-assembled, monolayer arrays of hexagonally close-packed SiO_2 nanospheres, deposited directly onto the surface of the sapphire growth substrate, to reduce Fresnel reflection and scatter light at the sapphire air interface, widening its escape cone. In addition to SiO_2 nanosphere arrays, nanohemisphere arrays were also investigated and found to exhibit even greater η_{EXT}, though at the cost of a more complex fabrication process. FDTD simulations were utilized to investigate the effects of different nanosphere and nanohemisphere diameters on the η_{EXT} and angular distribution of extracted light.

Angle-dependent EL measurements were performed on the patterned UV LEDs to investigate the effects of nanosphere and nanohemisphere arrays on the intensity of extracted light at different angles relative to the surface normal of the sample. Our simulation and experimental results show good agreement with respect to the angular distribution of emitted light, which indicates that the use of nanospheres and nanohemispheres shows promise for enhancing the low angle η_{EXT} of UV LEDs emitting around 280 nm.

The external quantum efficiency of an LED is a measure of its ability to convert injected charge carriers into photons which are fully extracted from the device into free space, and is a product of three subcomponents - the light extraction efficiency, carrier injection efficiency (η_{INJ}), and radiative recombination efficiency (η_{RAD}). The internal quantum efficiency (η_{IQE}), given by the product of (η_{INJ}) and (η_{RAD}), which quantifies the fraction of injected charge carriers which successfully recombine within the active region of the LED to produce light, has been fairly well optimized over the past decade [96,107]. While advancements in epitaxial growth techniques have allowed for reduction of threading dislocation densities and optimized active region design, leading to attainment of injection efficiencies greater than 60% by some research groups [119–121], η_{EXT} remains the limiting factor in achieving high η_{EQE} for UV LEDs [96,102,107]. On average, η_{EXT} is less than 10% in LEDs emitting within the UV spectral range due to the large refractive index contrast between the growth substrate and air [96].

UV LEDs are most commonly based on the AlGaN materials system, and are grown on sapphire substrates or other high index materials such SiC or AlN. It is common practice to package UV LEDs in a “flip-chip” configuration, with light extraction achieved through

the growth substrate. In accordance with Snell's Law, light passing from a medium with a high index of refraction such as sapphire ($n_{sapphire} = 1.82$) to a low index medium such as air ($n_{air} = 1$) will have a small critical angle and a correspondingly narrow escape cone, permitting only a small fraction of the light generated within the LED to escape. For example, the critical angle for light passing from sapphire into air is $\theta_c = 33.33°$, corresponding to $\eta_{EXT} = 0.082$, or 8.2%. Such a low η_{EXT} is a significant hindrance to the implementation of UV LEDs in many applications which require high luminous intensity. The low critical angle of the sapphire-air interface means that the majority of light incidence upon the interface will experience total internal reflection, and propagate within the sapphire indefinitely until it is either absorbed or emitted out the side of the device where it is of little use. Total internal reflection is most pronounced when the sapphire-air interface is perfectly planar. Studies have shown that surface roughening and surface nanostructuring can serve to mitigate the impacts of a narrow escape cone and allow enhanced light extraction from UV LEDs [97,98,102–104,108–117]. When periodic or random geometries are present at the sapphire-air interface, light incident beyond the critical angle, which would normally be reflected entirely, has a much higher probability of escaping. While direct patterning of the sapphire-air interface through dry etching has achieved promising results, simpler techniques such as the use of self-assembled nanosphere arrays are also promising. The presence of SiO_2 nanosphere arrays at the interface serves not only to introduce periodic geometry, but the intermediate refractive index of SiO_2 ($n_{SiO_2} = 1.49$) acts to increase the critical angle for light passing from sapphire into SiO_2. The non-planar geometry of the nanospheres then aids in transitioning the light into free space. More complex interactions between UV light and SiO_2

nanostructures can arise when interference patterns emerge within the nanospheres, and careful optimization of wavelength and nanostructure diameter can, in theory, allow for tuning of η_{EXT} as well as the angular distribution of emitted light.

5.5.2 Simulation Results

Three-dimensional FDTD simulations were performed in order to investigate the effects of nanosphere and nanohemisphere arrays on η_{EXT} through the sapphire substrate of UV LEDs emitting at 280 nm using Synopsys Fullwave [122]. Transverse-electric (TE)-polarized dipole sources were used for all simulations, as the majority of photons generated with wavelengths near 280 nm within conventional AlGaN/GaN LEDs have TE polarization [123]. Additionally, previous studies have shown that light with this polarization exhibits much higher extraction efficiency than transverse-magnetic (TM)-polarized light due to reduced reflection at material interfaces [97,98,124]. As a result, TM-polarized light contributes a negligible fraction of the total luminous flux escaping into free space. The simulation structure, which can be seen in Figure 5.5.1, is representative of a typical AlGaN MQW UV LED, and is inverted with respect to the growth direction.

In the UV LED studied here, AlN is grown on sapphire to act as a buffer layer, impeding the propagation of lattice mismatch induced dislocations into the active region of the device. Following growth of AlN, the AlGaN and GaN layers are grown. Because UV LEDs are usually packaged in a flip-chip configuration, with light generated within the MQW region emitted through the sapphire substrate, our simulation structure inverts the orientation of the epitaxial layers to mimic this configuration. The size of the domain was set to be 30 μm in width and depth, and 2 μm in height in order to optimize simulation

convergence and simulation run time. A non-uniform 3D mesh with cell dimensions between 5 and 10 nm was used to optimize simulation accuracy and run time.

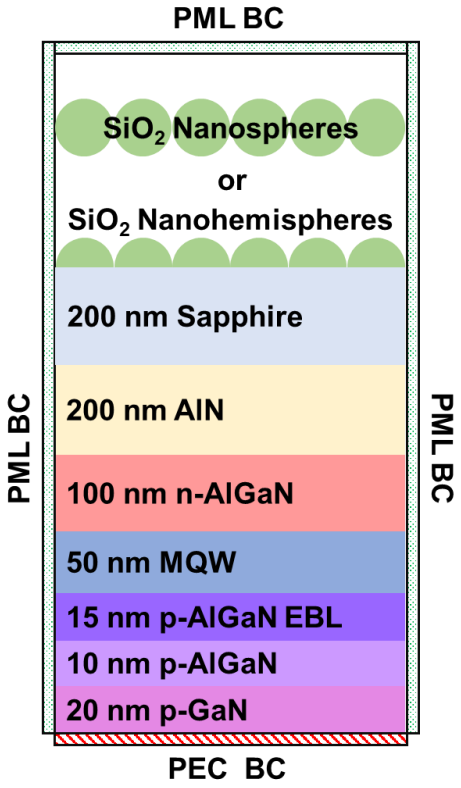

Figure 5.5.1: Cross-sectional representation of the three-dimensional structure used for FDTD simulation. Perfectly matched layer (PML) and perfect electric conductor (PEC) boundary conditions (BC) are shown at the domain surfaces.

Although a physical device would be grown on a sapphire substrate at least 200 µm thick, simulating such a device with an acceptable degree of accuracy would require significant simulation time for a single run, so we opted to use much thinner, 200 nm thick sapphire. Use of a growth substrate of significantly reduced thickness is common practice when performing FDTD or ray tracing simulation of LEDs, as it allows for order of magnitude reductions in simulation run time while maintaining the accuracy of the simulation [62], [63], [75]. Although our 200 nm sapphire layer imparts orders of magnitude less

attenuation than 200 μm sapphire, the low value of the extinction coefficient of sapphire at 280 nm, a mere 0.001, makes this discrepancy negligible. Refractive index and extinction coefficient values for all materials were taken from Palik *et al.* [98,125].

A perfect electric conductor (PEC) boundary condition was used at the bottom of the simulation domain to replicate the reflective p-metal contact, while perfectly matched layer (PML) boundary conditions were used for all other domain surfaces, as shown in Figure 5.5.1. To measure the η_{EXT} of a given structure, a three-dimensional power monitor was positioned to enclose the dipole source and measure its luminous power flux. Another two-dimensional monitor was located at the top of the simulation domain, 1.4 μm above the sapphire surface, to measure the luminous power flux passing through the sapphire-air interface. By calculating the ratio of the luminous power flux through these two monitors over the course of each simulation run we were able to determine the fraction of light emitted by the dipole source which successfully escapes across the sapphire-air interface into free space. The monitor at the top of the simulation domain also served to record the spatial intensity of incident radiation, allowing for generation of far field intensity plots and determination of the angular distribution of light escaping across the sapphire-air interface. Additional two-dimensional monitors were placed vertically within the simulation domain to record the spatial electric field intensity to allow for further characterization of the angular distribution of light within different regions of the simulated structures.

Figure 5.5.2(a) shows the η_{EXT} for 280 nm UV LEDs with arrays of SiO_2 nanosphere and nanohemisphere structures with diameters ranging from 50 nm to 700 nm.

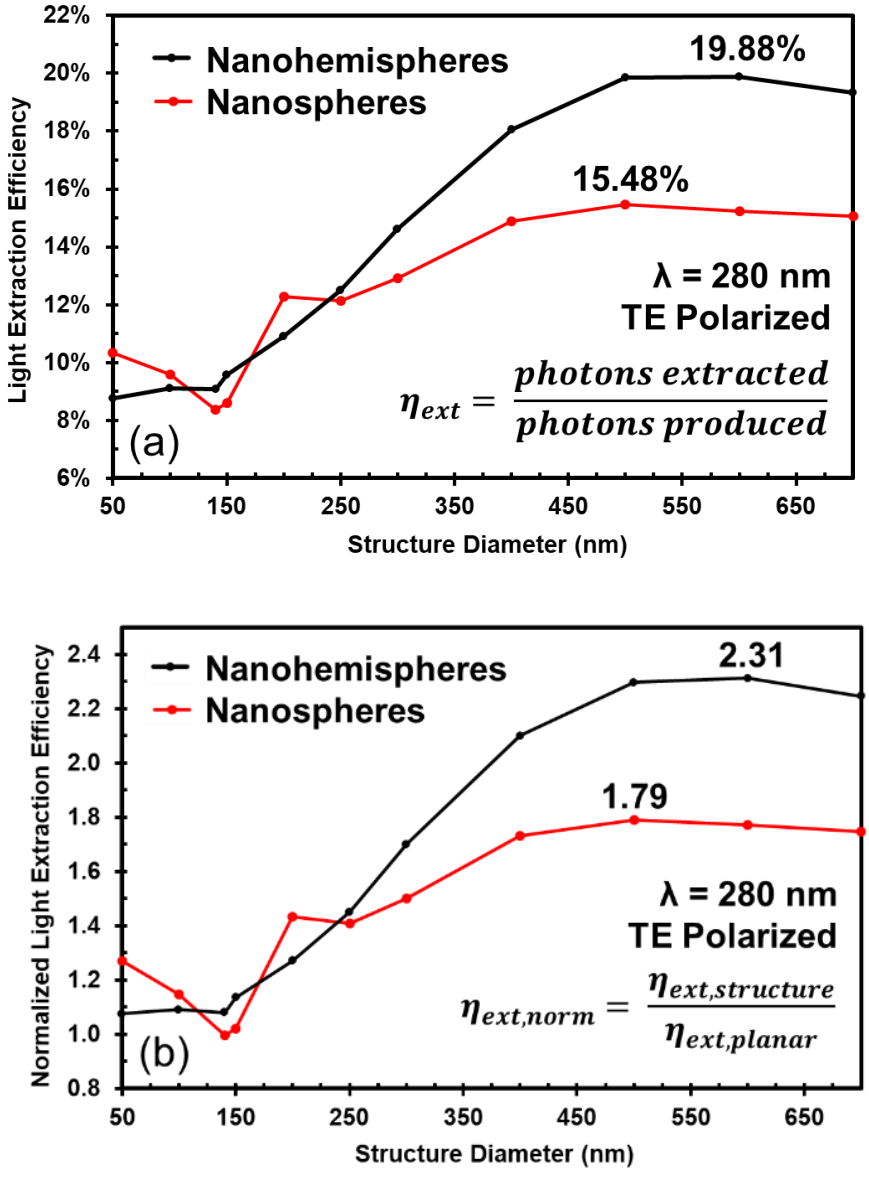

Figure 5.5.2: (a) η_{EXT} of SiO_2 nanospheres and nanohemispheres of variable diameter. (b) Normalized η_{EXT}s of SiO_2 nanospheres and nanohemispheres calculated by dividing the values shown in (a) by the η_{EXT} of a planar sapphire structure with no SiO_2 nanostructures (8.57%).

Both structures show significantly enhanced η_{EXT} for diameters upwards of 400 nm. A peak η_{EXT} of 19.88% was achieved at a nanohemisphere diameter of 600 nm, while 15.48% η_{EXT} at a diameter of 500 nm was achieved through use of nanospheres. These peak

enhancements can be attributed to constructive interference of light within the nanostructures which acts to suppress reflection and amplify transmission into free space. The "normalized" η_{EXT} values shown in Figure 5.5.2(b) are of greater importance and represent the η_{EXT} enhancements produced by nanostructure arrays of differing diameter, relative to a planar sapphire structure lacking any surface nanostructuring.

By dividing the η_{EXT} values shown in Figure 5.5.2(a) by the η_{EXT} for a planar UV LED (8.57%), we obtained the "normalized" η_{EXT} values ($\eta_{EXT,\ norm}$) which are plotted in Figure 5.5.2(b). These normalized results show that η_{EXT} is enhanced ($\eta_{EXT,\ norm} > 1$) for nearly all nanostructure diameters for both nanospheres and nanohemispheres. Enhancement of 2.31x (131%) is seen for nanohemispheres at 600 nm, while 1.79x (79%) enhancement is seen for nanospheres at 500 nm. Only in the case of 140 nm nanospheres is a decrease in η_{EXT} seen, and is likely due to destructive interference within nanospheres whose diameters are exactly half that of the 280 nm wavelength light used for the simulations.

In addition to investigating η_{EXT}, we also examined the angular distribution of escaping radiation using a combination of cross-sectional electric field intensity and far field radiation intensity plots in order to better understand the interaction of 280 nm light with arrays of variable diameter nanostructures. The diameters of the nanostructures used in our simulations and experiments, which are within a few multiples of the wavelength under examination, are smaller than those of the much larger "microlens" structures which have been investigated by other research groups [111–117]. Structures on the order of several wavelength multiples allow for complex interaction with light, leading to establishment of standing waves within the nanostructures which can enhance light

extraction and alter the angular distribution of emitted light. Likewise, nanostructures of certain diameters can serve to suppress light emission when destructive interference occurs within the SiO_2 structures. Figure 5.5.3 shows cross-sectional electric field intensities for

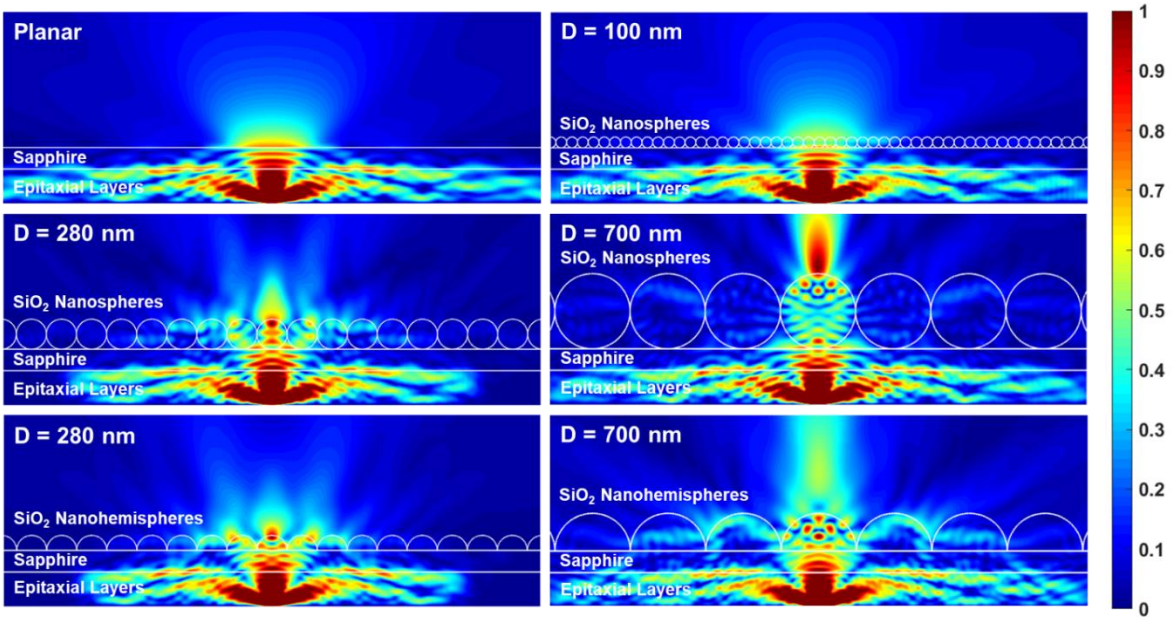

Figure 5.5.3: Cross-sectional electric field intensities for simulation structures of variable nanosphere and nanohemisphere diameters, showing spatial variation in electric field intensities with nanostructure diameter.

six different structures; a baseline "planar" structure with no SiO_2 nanostructures, and the others with nanospheres and nanohemispheres with diameters ranging from 100 nm to 700 nm. Comparing the case of 100 nm nanospheres to the baseline, it is apparent that these subwavelength nanostructures have little to no effect on the angular distribution of the light which escapes into free space. The cross-sectional electric field for 100 nm nanohemispheres was found to be nearly identical to that shown for 100 nm nanospheres in Figure 5.5.3. For near-wavelength nanostructures, i.e. those with diameters of 280 nm, a significant increase in electric field intensity at higher angles (relative to the surface

normal) is evident, due to the formation of standing waves within the nanostructures and destructive interference of low angle light. Increasing the diameter of the nanostructures to 700 nm reduces the emission of higher angle light, and produces a massive increase in the intensity of light emitted at low angles into free space. The establishment of a more complex standing wave pattern within these larger nanospheres seems to assist the emission of light through the tops of the nanostructures. Results for 280 nm and 700 nm nanospheres and nanohemispheres were found to be nearly identical, as shown in Figure 5.5.3. The most prominent difference between the two structures is a reduced number of electric field nodes within the nanohemispheres, which can be attributed to their smaller height and reduced volume.

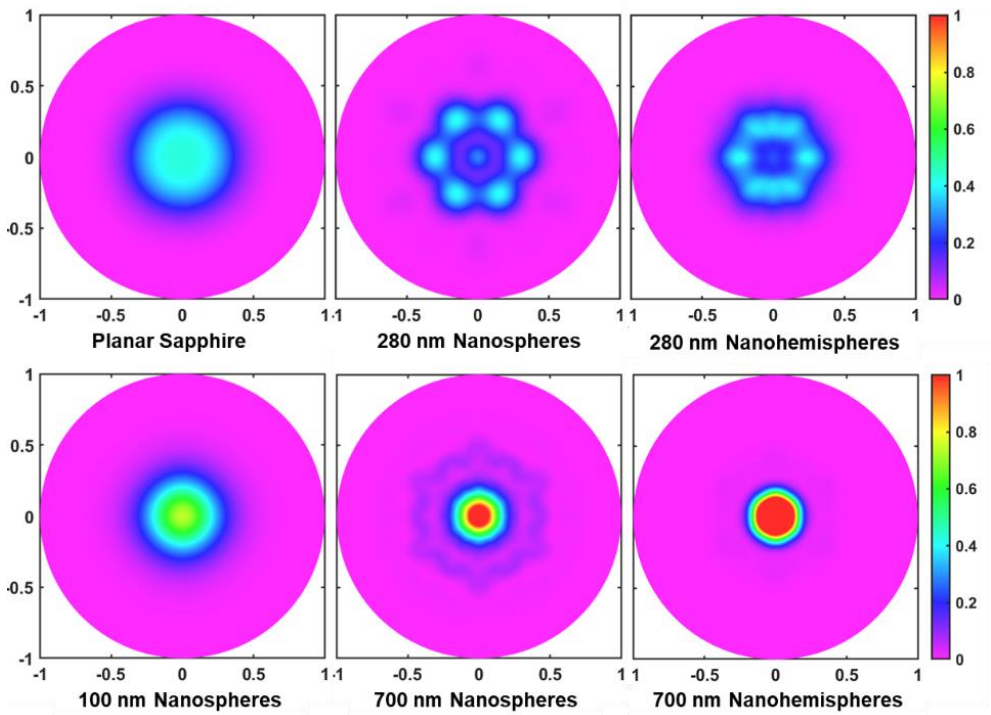

Figure 5.5.4: Far field radiation intensity patterns for simulation structures of variable nanosphere and nanohemisphere diameters showing spatial variation in far field radiation intensity with nanostructure diameter. The centers of these plots ($x = y = 0$) represent emission at 0° off-normal while the plot edges ($x = y = \pm 1$) represent emission at 90° off-normal.

Measurements of the radiation intensity incident upon the top of the simulation domain paint a clearer picture of the angular distribution of escaping light. Figure 5.5.4 shows the far field radiation intensity patterns for the six structures whose cross-sectional electric field intensities are shown in Figure 5.5.3, with the centers of these plots ($x = y = 0$) representing emission at 0° off normal and the edges of the plots ($x = y = \pm 1$) representing emission at 90° off normal. It is again evident that 100 nm subwavelength nanospheres have very little effect on the far field radiation pattern, producing only a negligible increase in intensity at 0°, while 280 nm nanostructures show more clearly the preferential emission at higher angles suggested by Figure 5.5.3. The use of 700 nm nanostructures shows a strong propensity to emit light at very low angles with high intensity in agreement with Figure 5.5.3. These far field radiation plots allow for easier visualization of the angle dependent radiation intensity.

It is evident that near-wavelength 280 nm nanostructures suppress low angle emission and enhance higher angle emission while larger 700 nm nanostructures serve to produce large enhancements in low angle emission. The hexagonal symmetry of the far field patterns evident for 280 nm nanostructures is representative of the hexagonally close-packed arrays used for the simulations. The data from these far-field radiation intensity plots is collected and reformatted in Figure 5.5.5, which presents overlaid polar intensity plots of the far field data for each of the six simulation structures. These plots allow for easy quantitative comparison between nanostructures of different diameters, and clearly shows the striking contrast between the angular emission profiles of subwavelength, near-wavelength, and super-wavelength nanostructures. The polar intensity profiles for the planar and 100 nm nanosphere structures are shown to be nearly identical, in agreement

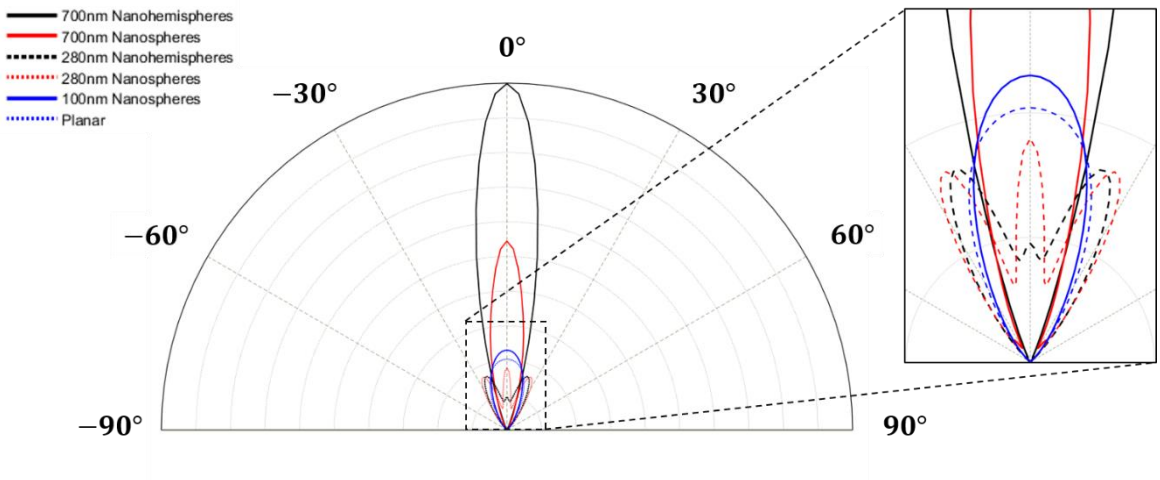

Figure 5.5.5: Overlaid polar intensity plots of the far field radiation intensity data presented in Figure 5.5.4, allowing for easier quantitative comparison of simulation structures with variable nanosphere and nanohemisphere diameters.

with Figures 5.5.3 and 5.5.4. The profiles of the 280 nm nanosphere and nanohemisphere structures are similar, with the exception that the nanosphere structure shows slightly higher emission intensity at higher angles. Most importantly, it is evident that 700 nm nanohemispheres show greatly enhanced emission at low angles when compared with nanospheres, with a nearly 2x enhancement realized at 0°.

The results of three-dimensional FDTD simulations show not only that the overall η_{EXT} of UV LEDs can be improved through application of SiO_2 nanosphere and nanohemisphere monolayers to the sapphire surface, but also that the angular distribution of emitted light can be controlled by varying the diameters of these nanostructures. The marked improvement in η_{EXT} achieved through this approach could be of significant benefit to the UV LED lighting industry, which has thus-far struggled to produce devices with acceptable η_{EXT}. The ability to manipulate the angular distribution of emitted light is also of interest, as low angle light emission from the surface of an LED is often desirable, as

this light is more useful for bulk lighting applications than light emitted at higher angles to the surface normal.

5.5.3 Experimental Results

In order to verify the results of our FDTD analysis, experiments were carried out to further elucidate the effectiveness of using nanosphere and nanohemisphere arrays to enhance the η_{EXT} of UV LEDs. In order to repeatably test the ability of nanosphere and nanohemisphere arrays to enhance η_{EXT}, we adopted an approach in which nanosphere and nanohemisphere arrays were fabricated on pieces of 200 μm sapphire. These nanostructure-on-sapphire samples were then positioned on top of a prepackaged 280 nm UV LED. Light emission from the LED was stimulated through EL and the intensity of light emitted through the sapphire and SiO_2 nanostructures was measured using a spectrometer. The angle at which light was collected relative to the surface normal of the sample was altered through careful angling and positioning of the spectrometer optical fiber.

A cross-sectional view of the UV LED used in these experiments is shown in Figure 5.5.6(a). The LED was composed of AlGaN epitaxial layers grown on a 300 μm thick sapphire substrate. An 80 nm 20x $Al_{0.6}Ga_{0.4}N$/AlN superlattice was first grown atop a 1 μm AlN buffer layer, followed by 2 μm of n-$Al_{0.55}Ga_{0.45}N$, a 65 nm 5x n-$Al_{0.35}Ga_{0.65}$-N/n-$Al_{0.43}Ga_{0.57}N$ MQW, a 20 nm $Al_{0.6}Ga_{0.4}N$ EBL, 40 nm p-$Al_{0.55}Ga_{0.645}N$, and a 160 nm of p-GaN. Electrical contacts were made to the n-$Al_{0.55}Ga_{0.45}N$ and p-GaN layers using a planar mesa-etching approach. Si and Mg were used for the n and p-dopants respectively. The LED die was mounted to the package shown in Figure 5.5.6(b) in a flip-chip configuration, lending it the inverted orientation displayed in Figure 5.5.6(a), with

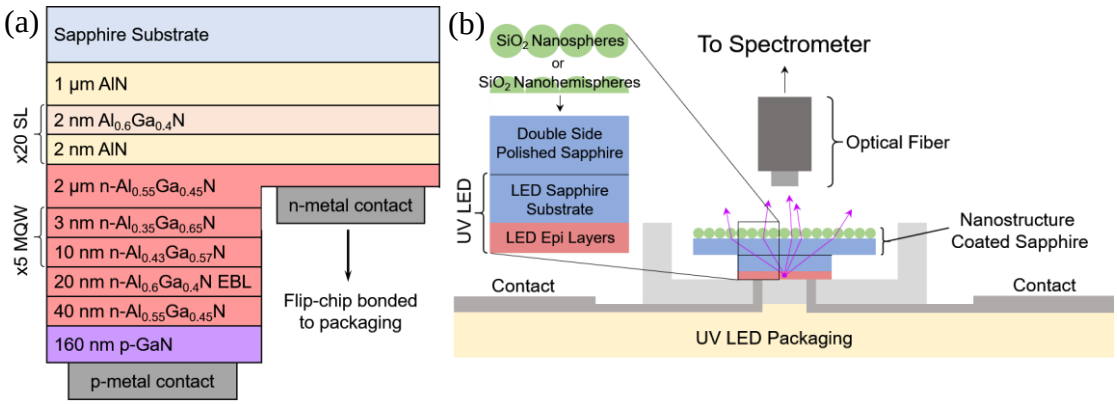

Figure 5.5.6: (a) Cross-sectional view of the UV LED epitaxial structure used to test η_{EXT} through nanosphere and nanohemisphere arrays. (b) Cross-sectional view of the angle-dependent EL setup used to measure normalized η_{EXT} through a nanostructure-on-sapphire sample.

light generated within the MQW active region emitted through the sapphire growth substrate at the top of the device. Nanostructure-on-sapphire samples were prepared using 200 µm thick sapphire wafers cleaved into pieces of area approximately 2 cm^2. These samples were then subjected to an oxygen plasma for 30 seconds in order to remove surface contaminants to improve the adhesion of the SiO_2 nanospheres to the sapphire. Nanospheres suspended in an aqueous, non-colloidal solution, obtained from Polysciences Inc., were then deposited on the surface of the sapphire samples via spin coating at approximately 1700 rpm. The nanospheres self-assemble into hexagonally close-packed monolayers. Fabrication of nanohemisphere samples followed this same process, with the addition of a reactive ion etch (RIE) in O_2/CF_4 plasma to shrink the diameters of the 700 nm SiO_2 nanospheres by approximately 200 nm. A 300 nm layer of conformal SiO_2 was then deposited using plasma enhanced chemical vapor deposition (PECVD) to form a hemispherical cross-section.

Following fabrication of SiO_2 nanosphere and nanohemisphere arrays on sapphire, these nanostructure-on-sapphire samples were cleaved into approximately 1 mm^2 pieces, to allow for placement on top of the packaged UV LEDs. The test setup is shown in cross-section in Figure 5.5.6(b). The UV LED, recessed within a protective metal ring to prevent physical damage to the bonded die, acted as a platform upon which the 1 mm^2 SiO_2 nanostructure-on-sapphire samples were placed. The dimensions of the metal ring protecting the LED die limited the size of the cleaved samples to 1 mm^2, and samples were placed onto the LED die, bringing the sapphire side of the sample into direct contact with the sapphire growth substrate of the LED with care taken to ensure flush contact between the two surfaces and prevent accidental damage to the LED die. Electrical contact was made to the packaged LED by probing a pair of contact pads located near the edge of the package. EL of the LED was achieved by biasing at 10V, which was found to induce a stable light emission intensity of approximately 25,000 counts per second at 280 nm, as recorded by an Ocean Optics Flame-S spectrometer. Angle dependent measurements were

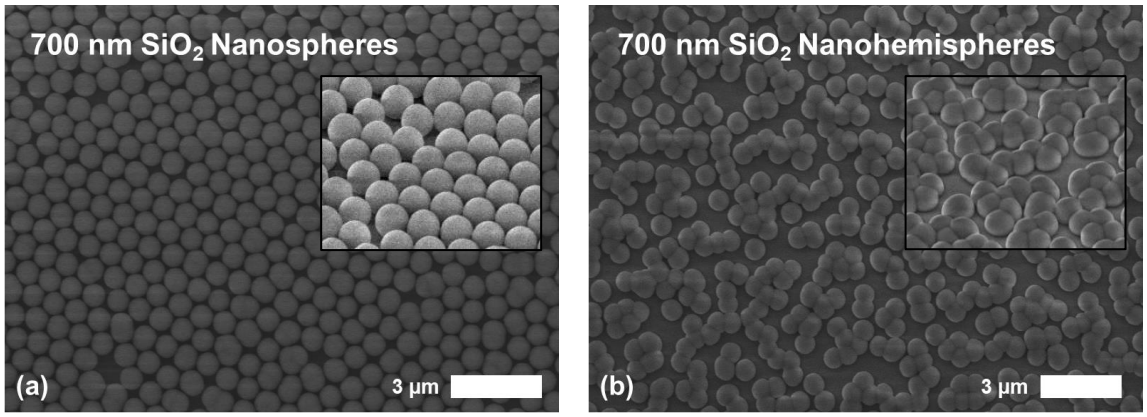

Figure 5.5.7: SEM images of 700 nm SiO_2 nanosphere (a) and nanohemisphere (b) arrays, formed through spin-coating of aqueous nanosphere solutions and subsequent RIE and PECVD SiO_2 deposition in the case of (b). Insets show the sample surfaces at 45°.

taken for nanosphere coated UV-LED samples by rotating the optical fiber shown in Figure 5.5.6(b) up to 60° off-normal, taking measurements every 10° to allow for construction of a rough far field intensity polar-plot similar to Figure 5.5.5 [123].

Figures 5.5.7(a) and 5.5.7(b) show SEM images of the 700 nm nanosphere and nanohemisphere samples respectively. The nanosphere coating in Figure 5.5.7(a) appears uniform, with only minor dislocations and vacancies present in the hexagonally close-packed array due to the non-spherical nature of some SiO_2 nanostructures. Figure 5.5.7(b), showing the nanohemisphere coating, appears distinctly different from the well-ordered, close-packed structure in Figure 5.5.7(a). This deviation may be due to interaction of oxygen and fluorine ions with the SiO_2 nanospheres during the RIE step which leads to development of surface charge states on the nanospheres. These surface charges could lead to electrostatic attraction between nanospheres, causing them to move across the sapphire surface and agglomerate as they shrink during RIE. This phenomenon leads to the short-range disorder seen in Figure 5.5.7(b), while long range order appears to be maintained over the surface of the sample. Subsequent PECVD SiO_2 deposition then serves to form the intended hemispherical cross section. While we believe these results to be non-optimal, as around 30% of the sapphire surface remains exposed, enhanced light extraction is still achieved as predicted by our FDTD simulations. In subsequent experiments, we believe it may be possible to prevent agglomeration of the nanospheres during the RIE step by spin-coating a thin layer (~100 nm) of poly (methyl methacrylate) (PMMA) to act as a "sticking layer". While this polymer will be attacked and eventually removed by the oxygen component of the plasma, it should remain in place long enough to allow the nanospheres to shrink down enough such that the attractive electrostatic forces

between the SiO_2 surfaces are no longer great enough to move the nanospheres across the sapphire surface, thus preventing nanosphere agglomeration.

Figures 5.5.8(a) and 5.5.8(b) show the averaged EL intensity spectra at normal incidence of the nanosphere and nanohemisphere samples between 260 nm and 315 nm. By comparing the integrated EL of each peak in Figure 6.5.8(a), it was found that the

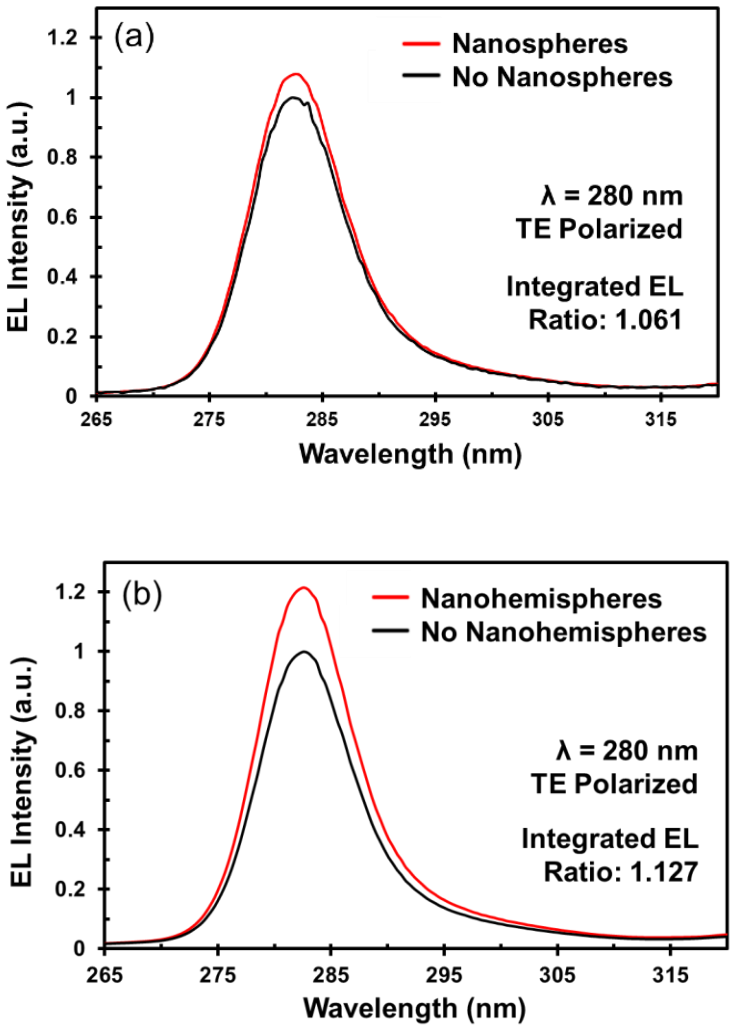

Figure 5.5.8: EL spectra for 700 nm nanospheres (a) and nanohemispheres (b) plotted taken at normal incidence between 260 nm and 315 nm. The much larger η_{EXT} enhancement of the nanohemisphere array is evidenced by the larger variation in the maxima of the curves for samples with and without nanohemispheres.

nanosphere coating enhanced light extraction by 6.1% when compared to a sample consisting only of sapphire with no SiO_2 nanospheres. The maximum emission intensity of the nanosphere-on-sapphire samples was measured to be 7.9% greater than that of the samples with no nanospheres. For nanohemispheres (Figure 5.5.8(b)), 12.7% enhancement in integrated EL and a 21.6% enhancement in maximum emission intensity was observed at normal incidence. These results, which show that nanohemispheres are more effective at enhancing low angle light extraction, agree with our simulation results. However, simulations showed nearly 2x greater intensity for nanohemispheres at normal incidence. The suboptimal uniformity of nanosphere and nanohemisphere coatings on sapphire likely accounts for this large deviation between simulation and experimental results for low angle η_{EXT} enhancement. Additionally, electrostatic agglomeration of SiO_2 nanospheres during the RIE step of nanohemisphere formation (as previously discussed) represents significant

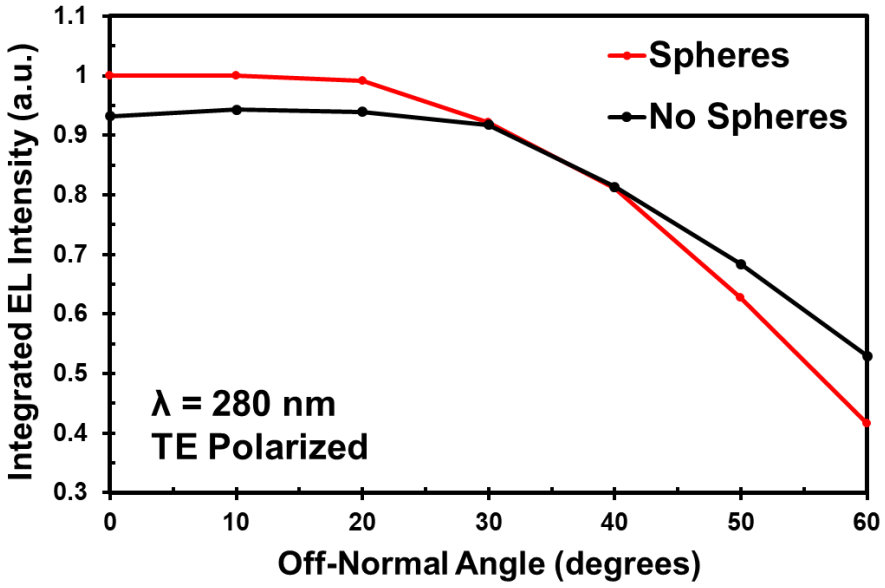

Figure 5.5.9: Angle-dependent EL data for 700 nm nanospheres, showing a clear increase in emission intensity at low angles less than 30° for samples with nanospheres when compared to samples with no nanospheres.

deviation from ideality, and contributes to a reduction in η_{EXT} enhancement from nanohemisphere-on-sapphire samples. The results of the angle dependent intensity measurements performed on nanosphere coated samples are presented in Figure 5.5.9, and show a clear increase in emission intensity at low angles less than 30° when compared to the sample with no nanospheres. Likewise, the nanospheres are seen to decrease emission intensity at angles greater than 40°. These results are likewise consistent with our simulations of the angle dependent intensities for 700 nm nanospheres, detailed in Figures 5.5.3-5.5.5.

5.5.4 Conclusions

In summary, the effects of monolayer SiO_2 nanosphere and nanohemisphere arrays on the light extraction efficiency of UV LEDs was investigated in this study for the first time. FDTD simulations were used to investigate the theoretical effects of these nanostructure arrays and further our understanding of how nanostructures of different diameters interact with 280 nm UV light. Angle dependent-EL measurements were carried out to verify the accuracy and legitimacy of the simulations results. Our experimental findings agree well with the results of our FDTD simulations with regard to the angular distribution of emitted light. Our simulations gave projected η_{EXT} enhancements of 75% and 124% for 700 nm nanosphere and nanohemispheres arrays respectively, and predicted that nanohemisphere arrays should produce 2x greater extraction enhancement normal to the sample surface than nanosphere arrays. Experimentation yielded 6.1% and 12.7% enhancement at normal incidence for 700 nm nanospheres and nanohemispheres respectively. Rigorous analysis of the angular distribution of emitted light through use of FDTD generated cross-sectional electric field and far field radiation intensity plots

indicates that 700 nm nanosphere and nanohemisphere arrays serve to focus emitted light towards lower angles relative to the surface normal of the sample, while near-wavelength 280 nm nanostructures suppress low angle emission and enhance high angle emission. Our experimental findings confirmed these predictions for 700 nm nanosphere arrays. These results confirm that SiO_2 nanostructure arrays show potential to improve the low angle η_{EXT} of UV LEDs and make them more viable across a range of applications, and the simplicity of this approach gives it an advantage over more complex procedures which require additional photolithography steps. We believe that the surface nanostructuring technique presented here could be further optimized and evolved in order to improve the performance of UV LEDs and allow them to penetrate a wider range of applications.

Chapter 5 References

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