Fabrication of Interdiffused Dual Work Function Metal Gate CMOS Capacitors

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Abstract-- Metal gate CMOS capacitors were formed using a metal interdiffusion process at RIT. First silicon dioxide was grown on the wafer. The first metal, titanium, was deposited. Then the second metal, nickel, was deposited. The nickel was selectively etched away from the top of half the capacitors to form the different work function regions. The wafers were then heated so that the nickel diffused into the titanium. The work function could not be determined of the metal gates because the MOS capacitors did not function correctly. The capacitance stayed constant across the allowable gate voltage. This is likely due to contamination of the silicon surface from spin on dopant.

1. INTRODUCTION

Currently CMOS transistors are made using polysilicon gates. The NMOS transistor uses a polysilicon gate that is heavily doped n-type with a work function around 5eV. The PMOS transistor uses a polysilicon gate that is heavily doped p-type with a work function around 4 eV. This allows the work function of the gate and the substrate to be closely matched resulting in surface channel devices with the desired threshold voltage and is the main reason that polysilicon is used for a gate material. However, there are two main disadvantages to using polysilicon as a gate material. Heavily doped polysilicon has high resistivity when compared to a metal. The polysilicon gate can also form a depletion region that will add to the capacitance-equivalent thickness of the gate. Below the 0.1 μm the polysilicon-depletion effect becomes significant to the MOSFET's performance. This has lead to the examination of using metals as a gate material. The interdiffusion of one metal into another can be used to change the work function of a gate without subjecting the dielectric to potentially harmful etches.

2. EXPERIMENTAL PROCEDURES

Table 1: Table of Oxide Thickness and Gate Material

Scribe	Oxide Thickness (nm)	Gate Material
1	35	Ti
2	35	Al
3	35	Ni
4	35	Ti / Ni CMOS
5	35	Ti / Ni
6	80	Ti
7	80	Ni
8	80	Al
9	80	Ti / Ni CMOS
10	80	Ti / Ni

The capacitors were fabricated on 100mm n-type wafers with a substrate resistivity of 1 to 25 ohms per centimeter and a crystal orientation of <100>. Aluminum gate wafers were used as a reference and different combinations of titanium and nickel gate wafers were used as shown in table 1 above. The back side of the wafers were four point probed to obtain the resistivity. Emulsitone Corp. N-250 spin on n-type dopant was coated on the back of the wafers to form the n+ region. The wafers were placed in a diffusion furnace for 20 minutes at 1000 °C. The wafers were etched in 50:1 buffered oxide etch for 5 minutes to remove any oxide grown. Next the 35 nm and 80 nm gate oxide was grown in a diffusion furnace. Titanium was then sputtered on top of the oxide using a 4 in. target in a pulsed DC magneto sputtering system (the CVC601)., The power was 300 W and the pressure was 2 mTorr. The target thickness of the titanium was 20nm, but the actual average thickness was 15 nm. Nickel was then sputtered on top of the titanium using a 4 in. target in a pulsed DC magneto sputtering system (the CVC601)., The power was 300 W and the pressure was 2 mTorr. The target thickness of the titanium was 40nm, and the actual average thickness was 41nm. Half of the Ti / Ni CMOS wafers were patterned with photo resist to form the NMOS and CMOS sections of the wafer. Nickel was then selectively removed these wafers using a solution of 20 parts deionizer water, 2 parts phosphoric Acid, and 1 part hydrogen peroxide at room temperature. The nickel etch rate was 60 nm/min and the

titanium etch rate was neglect able. The standard RIT capacitor mask was used to form the individual capacitors. It consists of four columns of round and square capacitors ranging in size from 100K μm^2 to 2 M μm^2. The nickel on was then etched using the same etch solution as before. The titanium was etched using a solution of 5 parts deionizer water, 1 part Ammonium Hydroxide, and 1 Hydrogen Peroxide at room temperature. The titanium etch rate was around 24 nm/min. The fronts of the wafers were coated with photo resist so that the oxide on backs of wafers could be etched with 50:1 buffered oxide etch. Aluminum was then sputtered on the backside of the wafers to form the back side contact. The wafers were then placed in a diffusion oven at 400°C for 45 minutes with a flow of 11 lpm of nitrogen gas. Forming gas consisting of nitrogen and hydrogen was not available on the tube used.

3. RESULTS AND DISCUSSION

The capacitors were tested using a Keithly CV analyzers connected to a PC computer with software to collect and analyze the data. The gate voltage went from -20 to 20 volts at a frequency of 1MHz. The results are shown in the graphs below.

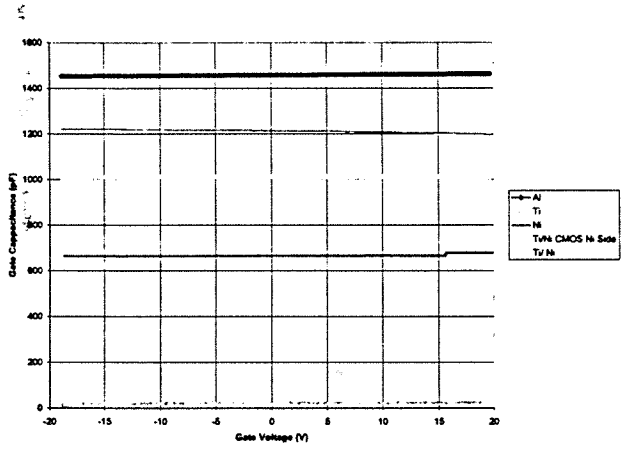

Figure 1: CV Plot of Capacitors with 0.01 cm^2 Gate Area and 35nm Oxide Thickness

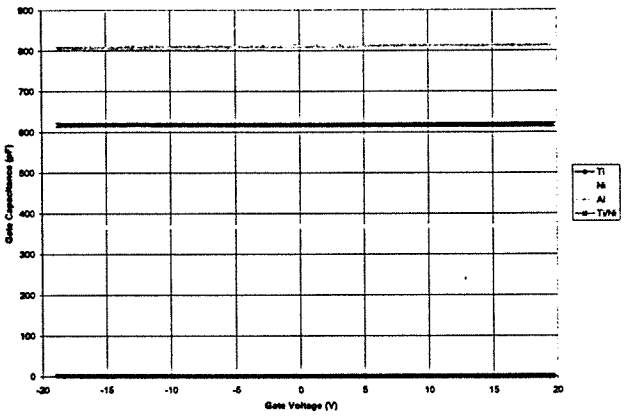

Figure 2 CV Plot of Capacitors with 0.01 cm^2 Gate Area and 80nm Oxide Thickness

The graphs shows that MOS capacitors were not formed on any of the wafers. The most likely source of failure of the devices was contamination of the front side of the wafers during application of the spin on dopant and diffusion of the spin on dopant.

4. CONCLUSION

Metal gate CMOS capacitors were formed using a metal interdiffusion process. The metal work function could not be determined because the capacitance stayed constant across the allowable gate voltage. This is likely due to contamination of the silicon surface from the spin on dopant. To reduce the chance of contamination, the dopant should have been implanted.

REFERENCES

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Michael Meagher, originally from Gouverneur, NY, received B.S in Microelectronic Engineering from Rochester Institute of Technology in 2002. He attained co-op work at Inficon and Microchip.