Fabrication and Characterization of Silicon Nitride Sacrificial Replacement Gate Technology

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Abstract—Silicon Nitride (Si3N4) sacrificial replacement gate were fabricated using the nitride cast method. The purpose of the Si_3N_4 cast was to develop a stand-in gate, which is then replaced by metal after source/drain formation. The technique was developed by using hot phosphoric acid etch (at 160 ° C) to form nitride cast. The phosphoric acid has nitride etch rate of about 4nm/min and good selectivity over oxide and good uniformity over silicon. A cross sectional analysis was done to view process steps.

1. GOALS

The main goal was to develop an etching technique, which can etch silicon nitride selectively and form a silicon nitride micro cast. So, single implantation can be done for drain and source after silicon nitride cast form.

2. BACKGROUND

The main objective of etching in microelectronic fabrication is the transfer of a pattern to a film on a wafer with no bias and acceptable tolerance. So the objective can be accomplished by removing regions of the film according to a specific pattern with the use of a selective etch process. Wet etch chemistry is generally isotropic in nature, and therefore the critical dimension (CD) can be lost due to bias when etching sub-micron features. Even though some an-isotropic wet etch chemistry exists, the wet chemical commonly suffers from high surface tension, which ultimately limits resolution. Dry etch process can achieved an an-isotropic etch profile and offer benefits over wet processing in terms of chemical handling, consumption, and disposal. However, the selectivity of dry etching is often not as high as it is in wet etch processing and this problem be address [6, 7]. In this project, silicon nitride (Si_3N_4) micro cast was investigated to feasibility of using as sacrificial or replacement gate. In this replacement or "cast" process, the metal gate is deposited after the S/D formation, which is performed with a temporary silicon nitride "microcast".

The silicon nitride film has been under cut by an etching technique to form t-shape Si_3N_4 "microcast". One of the critical part of this project was to develop an etch technique that can etch Si_3N_4 film selectively. The etching of the silicon nitride Local Oxidation of Silicon (LOCOS) structure has been traditionally done by hot phosphoric acid bath. The phosphoric etch has a nitride etch rate of about 4 nm/min and excellent nitride selectivity over oxide (>50) and Silicon as well as excellent uniformity [4]. Therefore this technique has good potential achieving manufacturability for <0.1 um device. Also, it is more advantageous than the technique for using poly-silicon stand-in gate, as reported recently [1].

3. PROCESS

Wafers were processed at RIT's Microelectronic Engineering facility, where all three layers and lithography steps were completed. Analytical part was done at Failure analysis Department of Micron Technology Manassas, VA.

A. Process steps

About 500A° of pad oxide was grown using Bruce Furnace tube 4. Then about 3500A° silicon nitride was deposited on pad oxide and 3000A° oxide deposited on silicon nitride by LTO. Lithography steps were performed to create window for oxide and silicon nitride etch. Figure1 shows the cross sectional view of the process.

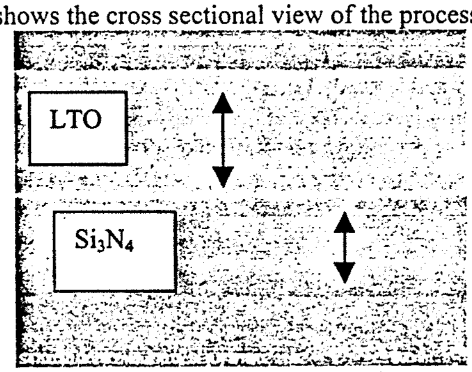

Figure1. Cross sectional view before etch

B. Etch steps

In order to get an-isotopic etch, RIE tool STS320 was used, which can etch Si_3N_4/SiO_2 at the rate of about 1000

A° per minute. After seven minutes of Reactive Ion Etch (RIE), it etched away the Si_3N_4/SiO_2 layer where no photo resist exists on the Si_3N_4/SiO_2 layers. Photo resist was removed before samples where prepared for wet etch. Fresh phosphoric acid poured into designated quart containers and covered with designated lid to prevent evaporation. Solution was heated to 160°C on the hot plate. Then samples were immersed into hot phosphoric solution and the lid was replaced to prevent evaporation which effect the etch rates. The summary of RIE tool (STS) setting is listed in Table 1.

Etching time	Pressure	Gasses	RF	Rate
7minute	300mT	CHF3=25% CF4 = 6%	400 Watts	1000 A/minute

Table1. RIE tool setup

C. Cross section

Samples were cut such a way that they can mount easily in the SEM sample holder. Polymer glue was used on when sample was hot (about 130°C) and then sample immediately under microscope while the glue is still hot. After the alignments, allow the sample holder to cool for few minutes and then mounted in the tripod. Different sand papers starting from 50um to.5um and spin speed of 150rpm to 50rmp respectively were used to polished samples. To prevent charging sample in the SEM, platinum was coated on the sample.

4. RESULTS AND FUTURE WORK

Hot phosphoric acid etch can etch silicon nitride very selectively while it maintains excellent uniformity on silicon substrate. At 160°C hot phosphoric acid can etch Si_3N_4 at the rate of about 4nm/minute over oxide. By using hot phosphoric acid etch, silicon nitride microcast can be formed on silicon substrate and can achiev gate line width reduction. Therefore this technique has good potential achieving manufacturability for <0.1μm devices. Also, it is more advantageous than the technique of using poly-silicon stand-in gate, as reported recently [1]. For simplicity a single implantation can be done for both source and drain and after the implantation Si_2O_4 can be deposited by LTO to fill up to Si_2O_4 cast. Then the wafer can polish down to the top of the nitride cast, then Si_2O_4 can be remove again by hot phosphoric acid etch. Figure2,3and 4 show cross section of nitride cast without oxide layer on top of it. Oxide layer lost during the cross-sectional process, because there was not any protecting layer on top of it.

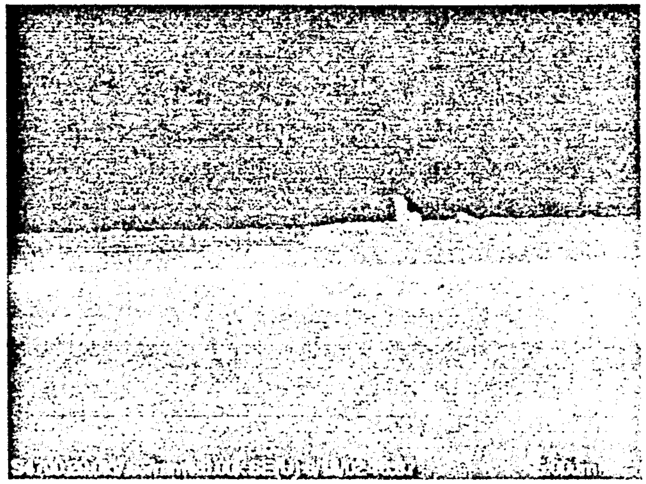

Figure2. Cross-section before hot phosphoric acid etch

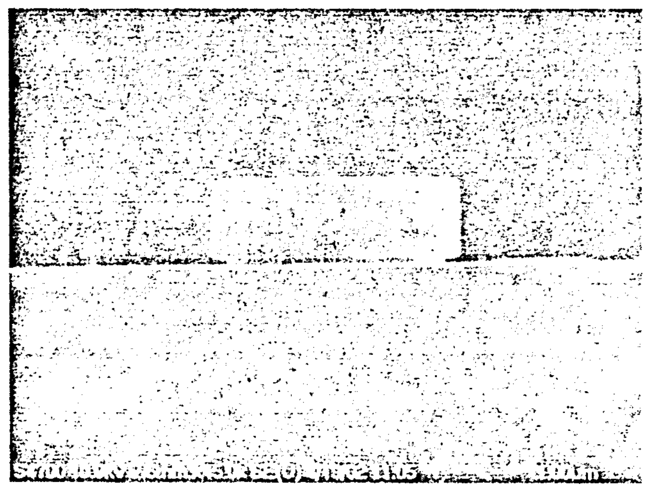

Figure3. Cross-section of Silicon Nitride cast after hot phosphoric acid etch.

Figure4. Cross-section after gate line width reduction

5. CONCLUSION

Overall, the hot phosphoric etch process and formation of silicon nitride cast have been demonstrated to be successful. In this process flow, gate width has reduced significantly and excellent nitride selectivity over oxide and silicon. This technique has good potential achieving manufacturability for less 0.1 μu devices at minimal cost opposed to other existing methods like poly-silicon stand-in gate.

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