Copper Gate MOS Capacitors Utilizing Chemical-Mechanical Planarization

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Abstract—Applying chemical mechanical planarization techniques to form the gate for a Cu/Ti/SiO_2/Si capacitor stack has shown to be a viable alternative to conventional etching techniques used in the fabrication of MOS devices. Furthermore, it is reported that CMP does not compromise the integrity of the dielectric nor does it have an adverse affect on device performance.

1. INTRODUCTION

The International Technology roadmap indicates a transition to metal gates for transistors by 2007[1]. With the replacement of poly-Si doped gates with metal will be eliminated gate depletion effects and higher drive currents achievable at lower voltages.[2] These advantages will be crucial for the industry to keep up with Moore's contention that the number of transistors on a microprocessor doubles every 18 months.[3] However, with the move to metal gates, comes the need for metals that can be used as pMOS or nMOS gates, with work functions as the design of the IC demands.

Designing IC's with metal gates will prove to be much more difficult than with the currently used doped poly-Si gates. Instead of simply changing the amount and type of dopant needed to achieve a threshold voltage, work functions will be fixed by the metal used.[4] Since there is a finite number of metals available, each with unique electrical properties, designing with metal gates will be far more difficult. The capability to etch these metals selectively by contemporary methods will most certainly force designers to eliminate particular metals as candidates for their designs. The use of CMP techniques at the gate level could be the solution to this future problem.

2. FABRICATION

To determine the feasibility of CMP techniques on the gate, a damascene process was created and can be seen in figure 1. In this process great emphasis was placed on the integrity of the gate oxide. To accomplish this, steps were taken which included using industry grade (PPB contaminates) chemicals for the RCA cleans, as well as shielding the substrates from airborne particulates and metallic contaminates as much as possible. Additionally, since Copper is known to diffuse through oxide, Titanium was used as a barrier and adhesion layer. This was accomplished through sublimation directly prior to Cu evaporation.

The background wafers were 4" P-type Boron doped 8-12 -cm (100) CZ grown. A 5000Å field oxide was grown followed by lithography patterning. An RCA clean was a precursor to the gate oxide growth of roughly 200Å. Next, approximately 200Å Ti and 6000Å Cu were deposited, forming step 5 in figure 1. Lastly, CMP was performed and a backside Ohmic contact was formed using Aluminum.

For comparison purposes, two other capacitor designs were fabricated. These comprised an Al gate evaporated/sputtered design and a Cu/Ti shadow mask design. The steps to fabricate each one respectively were standard.

3. RESULTS

The damascene formed capacitors worked at an average breakdown strength of 7.54MV/cm with very low leakage. The standard deviation for these was the lowest of the three designs as well, indicating a high yield from devices made in this fashion. Equation 1 is the relation of break-down field strength to the applied voltage.

$$\mathcal{E}_{BR} = \frac{v}{t}$$

Where v is voltage and t is the thickness of the dielectric material. Table 1 shows the average result from all three designs. Data was acquired by testing a 500μm^2 round capacitor on each die at 25 test sites on every wafer. The test setup can be seen in figure 2. Since this was a pMOS device, voltage was swept from 0 to -40V and graphed versus –I. Figure 3 shows a typical breakdown strength for a device under test.

Based upon the data in table 1, it is interesting to note the difference in standard deviation between the Al gate sputtered and evaporated capacitor breakdown strength.

As can be seen, sputtered Aluminum had an adverse effect on the oxide integrity, due mostly to the plasma radiation in the chamber.

Figure 4 is a graphical representation of the results acquired from the three separate designs. It shows the breakdown strength and the standard deviation.

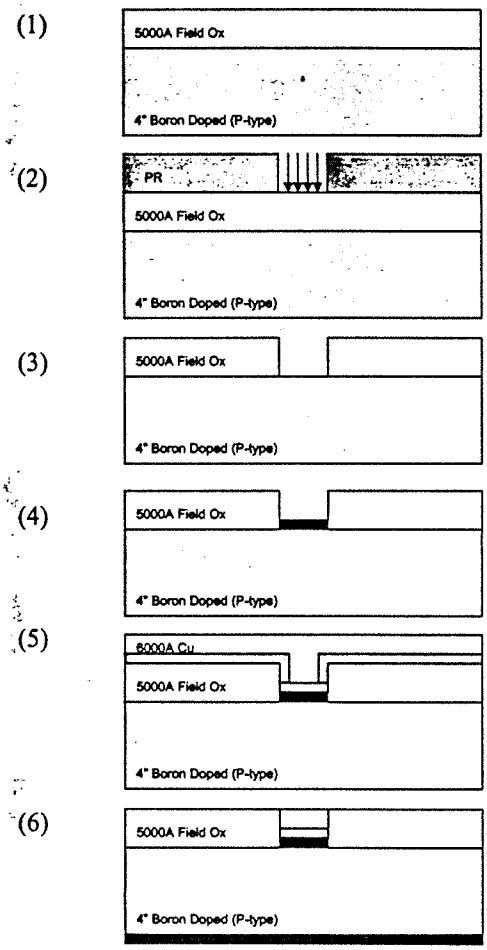

Figure 1 – damascene process flow

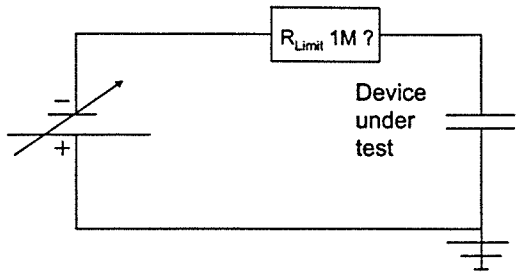

Figure 2 – test setup equivalent circuit

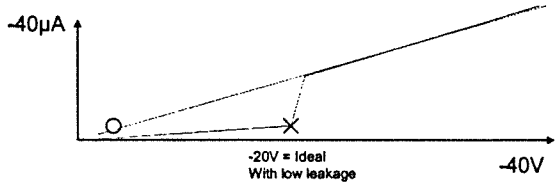

Figure 3 – breakdown demonstration of capacitor

4. CONCLUSIONS

Following the data, CMP is a viable alternative to conventional etching techniques used to form the gate. As is shown, the oxide integrity was not compromised by use of CMP, as the standard deviation was the lowest with the damascene formed gates. Finally, the devices did not suffer from adverse affects that were noticeable, and were not leaky.

5. REFERENCES

[1] "The International Technology Roadmap for Semiconductors: 2001." http://public.itrs.net/Files/2001ITRS/FEP.pdf, p. 32.
[2] Peter Singer, "Engineering a Better Transistor." Semiconductor International, March 1st, 2000.
[3] CNet Glossery. http://www.cnet.com/Info/Glossery/Terms/mooreslaw.htm
[4] Laura Peters, "Outlook on New Transistor Materials." Semiconductor International, October 1st, 2001.

	Al Gate (sputtered)	Al Gate (evaporated)	Cu/Ti Shadow	Cu/Ti Damascene
Breakdown (V)	15.8V	17.2V	11.7V	15.1V
Breakdown (ε)	7.6MV/cm	8.6MV/cm	5.9MV/cm	7.5MV/cm
σ	4.35V	1.6V	5.09V	1.0V

Table 1 – data from all three designs

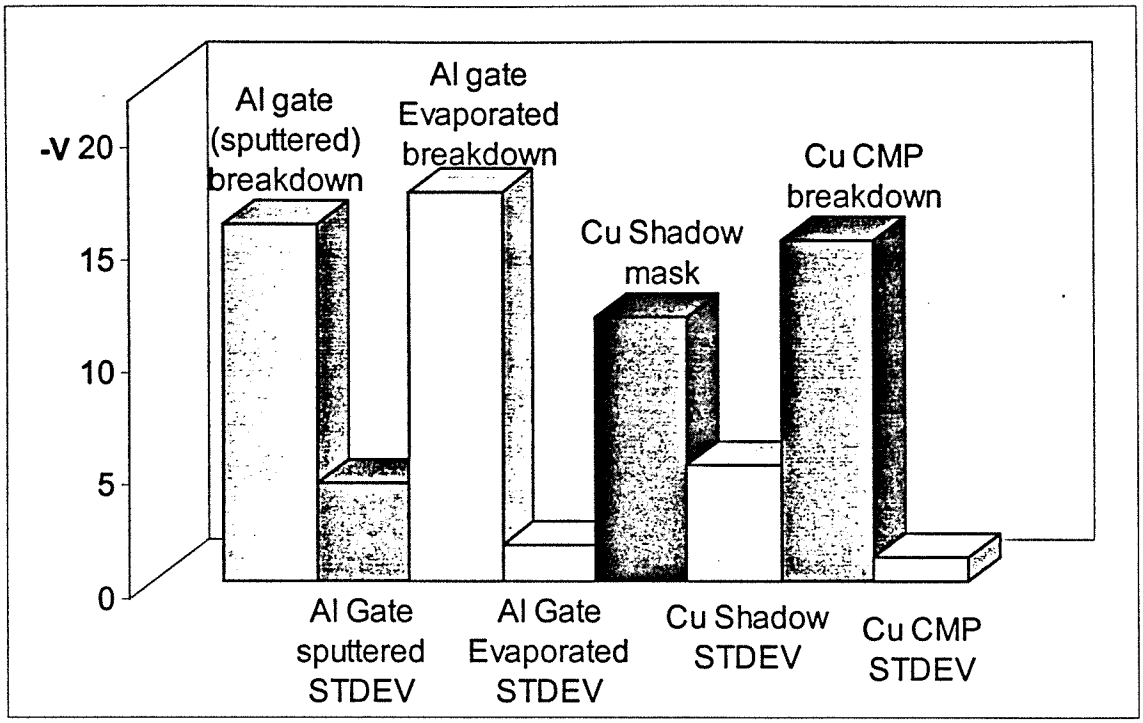

Figure 4 – graphical representation of table 1

6. ACKNOWLEDGMENTS

The author acknowledges Dr. Michael Jackson and Mike Leathem, M.S. for guidance in this project and the Semiconductor and Microsystems Fabrication Laboratory staff at the Rochester Institute of Technology for equipment support.

Luc Dupré, originally from Burlington, VT, received a B.S. in Microelectronic Engineering from the Rochester Institute of Technology in 2003. He has attained co-op work experience with St. Gobain Advanced Ceramics and Asyst Technologies.