Development of a PECVD Tetraethylorthosilicate (TEOS) Fill Process for Shallow Trench Isolation

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Abstract—As transistors have decreased in size and increased in packing density, a need has arisen for an alternative to the LOCOS method of isolation. Shallow trench isolation (STI) offers superior packing density and stronger immunity to latch up with other side benefits. A TEOS oxide fill for STI is a good choice because its mobile chemical precursors offer a high level of conformality. A plasma enhanced deposition of this oxide allows for greater control over film characteristics. A designed experiment was created to examine the effects of temperature, RF power, and substrate position (measured through electrode spacing) on the oxide quality and fill ability. High quality oxide with void free fill ability was found with the processes conditions: temperature of 350C, RF power of 350W and electrode spacing of 225mils.

1. INTRODUCTION

Shallow trench isolation (STI) has become the dominant isolation technology in the semiconductor industry since the processing of the first 0.35 μm devices. STI provides many benefits over the typical LOCOS process including tighter transistor packing, better immunity to latch-up, reduced topography and less channel-width infringement. These benefits come at the expense of process complexity. Extra steps are needed to create the trenches in silicon, fill them and CMP or etch the trench fill back.

The objective of this study is to develop a trench fill process focusing on TEOS deposited oxide as the dielectric fill. TEOS is an excellent choice for the dielectric since it exhibits better step coverage than traditional silane based chemistries. Improved step coverage is important to STI since it is crucial that the dielectric conforms to the sidewall of the trench and does not void or "keyhole". In addition to being conformal, TEOS is a safe alternative to silane and dichlorosilane.

2. THEORY

A. Plasma Theory

Introducing plasma into a chemical vapor deposition (CVD) system has two effects on the process. First, the energy for the ions in the plasma is sufficient to break down the reactant gases in the manner that an elevated temperature would in a conventional CVD system. This allows for processing at reduced temperature, providing savings in the thermal budget of a process [1].

Additionally, plasma has many influencing factors. These factors play a role in three main descriptive characteristics of the plasma: stability, density or plasma-surface interactions. The plasma stability is influenced by location of the plasma within the process chamber. Stable plasma will be confined between the electrodes and away from the system walls. The plasma density is a function of the RF power, system pressure, and reactant gas flows. The density will influence the deposited film uniformity and the deposition rate of the film. Plasma-surface interactions (if any) will be influenced by the temperature and position of the substrate with respect to the plasma. In most cases, plasma-surface interactions are undesirable and result in damage to the substrate surface due to ion bombardment. All of the factors that influence the plasma characteristics indirectly influence the film quality. Therefore the addition of plasma to the CVD reaction provides more control over the film quality.

B. TEOS Chemistry

The TEOS source for oxide deposition is typically a liquid transported to the process chamber via carrier gas (typically nitrogen or helium) through heated lines to prevent condensation. Once in the chamber the TEOS source will break down in the presence of heat or plasma:

$$Si(OC2H5)4 \Rightarrow SiO2 + 4C2H4 + 2H2O$$

In some processes, ozone is introduced into the reaction:

$$Si(OC2H5)4 + O3 => SiO2 + 10H2O + 8CO2$$

This ozone is added to ensure an adequate supply of oxygen for oxide formation [2].

3. EXPERIEMTNAL DESIGN

The three factors that impact the fill ability and oxide quality the greatest are: temperature, RF power, and electrode spacing. Table 1 shows the design setup used in this experiment.

Table 1. Experimental Conditions

Factor	Range
Temperature	350 to 400 C
RF power	200 to 500 Watts
Electrode spacing	150 to 300 mils

A designed experiment (DOE) was created using the above factors consisting of seventeen treatment combinations. At each treatment combination there was one trench patterned wafer and one blanket wafer deposited. The trench wafer was cross sectioned to determine fill ability. The blanket wafers were measured for oxide quality by refractive index through ellipsometry. Also, electrical parameters were collected by building metal oxide semiconductor (MOS) capacitors out of the blanket oxides and testing these devices. Table 2 lists the response variables for this experiment.

Table 2. Response Variables

Response	Indicator	Tool
Fill Capability	Voids in trenches	SEM
Oxide Quality	Refractive index	Ellipsometer
Electrical Characteristics	Breakdown strength	Semiconductor parameter analyzer

In addition to processing the TEOS oxide wafers according to the designed experiment, thermal oxide and low temperature CVD oxide (LTO) wafers were created to compare to TEOS in oxide quality and electrical characteristics.

4. EXPERIMENTAL PROCEDURE

The original focus of this work was to be completed using the Applied Materials P5000 PECVD tool recently acquired by the RIT department of microelectronic engineering. Issues with completing the installation of this tool forced the TEOS deposition to be outsourced to a facility with an identical P5000 tool and chamber configuration.

A. Processing

Silicon wafers, p-type, 6" in diameter were obtained and a silicon nitride layer (thickness = 185nm) was deposited to act as a hard mark. The nitride was patterned with the trench layout for this project. The layout consisted of line space pairs with a 1:1 duty ratio of width ranging from 0.2μm t0 3.0μm. The pattern was transferred to the silicon through a reactive ion etch (RIE) with SF6 and HBr gases. The nitride mask and the pad oxide was stripped and a thin thermal oxide (thickness = 1000nm) was grown to anneal surface damage in the trench due to aggressive RIE. Finally the TEOS oxide was deposited across the entire wafer according the DOE conditions.

For blanket deposition wafers, the oxide was deposited on the bare silicon. Aluminum was sputtered on the front and backsides, and a capacitor pattern was transferred to the aluminum on the front side. This completed the MOS capacitor fabrication. The thermal and LTO capacitors were created with the same methodology.

B. Parameter Analysis

The primary parameter analyzed was the fill capability of the oxides. If the oxide does not fill the trench, there is no meaning to measuring the other characteristics. The trench fill was examined by scanning electron microscope (SEM) cross sections. The wafers were cleaved across the trench patterned and polished to provide an enhanced visualization of the region of interest.

Oxide quality was examined through comparison of refractive indices of each type of oxide; TEOS, thermal or LTO. The standard accepted value for refractive index of silicon oxide is 1.46. The refractive indices were measured using a Rudolph ellipsometer.

Electrical characteristics were measured using an HP 4145 semiconductor parameter analyzer. A curve was traced plotting current versus voltage to determine the voltage at which the capacitor began to pass current. This is defined as the breakdown voltage. Along with knowledge of the size of the capacitor and the thickness of the film, the breakdown voltage can be used to calculate the breakdown strength.

5. RESULTS

By and large, all the wafers exhibited successful trench fill. All trench widths appeared to be filled without voiding. A typical cross sectional SEM is shown in Figure 1. The DOE settings for this run were: temperature of 350C, RF power of 350W and electrode spacing of 225mils.

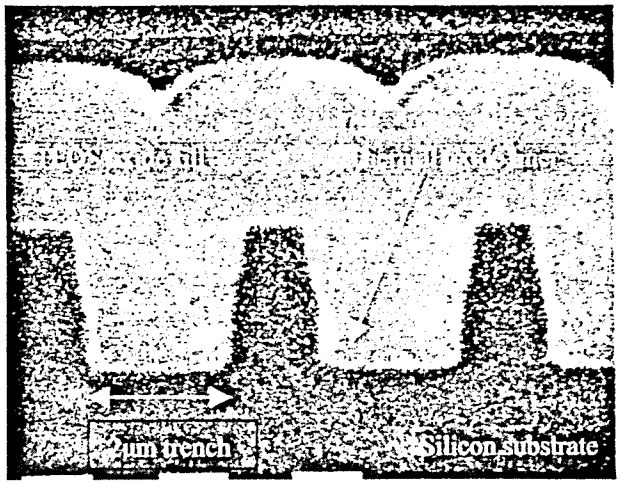

Figure 1. SEM cross-section of 2μm trench showing void free oxide fill. The tapering of the trench walls is due to a failure of the silicon nitride hard mask.

The SEM cross section of Figure 1 does not exhibit any voiding of the TEOS oxide fill. The thermal oxide is not immediately apparent but can be discerned as a faint darker grey along the edges of the trench.

One note of interest in the SEM cross section is the tapered tops of the trench areas. This is due to the failure of the hard mask near the end of the trench etch step. As the hard mask gave way, the RIE began to remove material that was previously covered. In order to implement this process into a factory flow, a thicker hard mask will need to be developed.

All of the wafers exhibited high quality with respect to refractive index, regardless of deposition or growth method. The results of the refractive indices measurements are provided in Table 3.

As with the refractive indices, the electrical characteristics of all oxides were of high quality. The lowest breakdown strength was of LTO oxide (as expected). Both the thermal and TEOS oxides exceeded the ability to breakdown the oxides, indicating breakdown strengths in excess of 10MV/cm. This is also tabulated in Table 3.

Table 3. Experimental Results

Oxide	Refractive index, Standard = 1.46	Breakdown strength, max = 12MV/cm
TEOS	1.444	>10MV/cm
Thermal	1.467	>10MV/cm
LTO	1.463	9MV/cm

6. CONCLUSIONS

The objective of this project was to develop a process for depositing void free TEOS oxide fill via PECVD for STI. This objective has been met, and the recommended process conditions are: temperature of 350C, RF power of 350 Watts, and electrode spacing of 225 mils.

Prior to implementation of this process into manufacturing, a thicker nitride mask needs to be developed in order to etch trenches into the silicon which are completely anisotropic, not just at the bottoms.

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ACKNOWLEDGMENTS

The author would like to thank Tharveen Sawhney and Steve Barnes for out of fab processing expertise and overall help with this project. The author would also like to recognize Dr. Karl Hirschman, Dr. Mike Jackson, and Dr. Santosh Kurinec for valuable technical advice.

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