Silicon Dry Etch Process for Shallow Trench Isolation

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Abstract—Shallow Trench Isolation (STI) holds many advantages to that of its predecessor isolation technology in that STI increases the packing density, has superior latch-up immunity, smaller channel-width encroachment, and better planarity, allowing for smaller and thus faster and/or less power hungry devices. The goal of this project was to develop an anisotropic silicon etch process for use in the Drytek Quad 482 Reactive Ion Etch system, yielding a depth of at least 0.5µm and steep sidewall angle of the trench. For this study, varying plasma chemistries of consisting sulfur hexafluoride, oxygen and argon are examined to etch the bulk silicon for formation of the trench using a 3000Å silicon nitride and 500Å pad oxide as a hard mask layer. Some anisotropy was seen in the etch process using a scanning electron microscope to examine the etch profile.

1. INTRODUCTION

Localized Oxidation of Silicon or LOCOS has been used as a device isolation technique for the past few device generations. LOCOS involves selective growth of silicon dioxide by blocking oxidants from reaching the surface of the silicon. The oxidation is prevented by a silicon nitride layer that is deposited using chemical vapor deposition. Some disadvantages of LOCOS is the encroachment of the active region by the "bird's beak" effect, where some oxide is grown at the edges of the active region, lifting the silicon nitride layer in that region causing high stresses in that region. The stresses cause defects by providing interstitial regions for metal ions and other defects to accumulate. Also the high temperatures required to grow the field oxide in the open regions also reduces control on dopant profiles in the wells regions as well as in the channel stop implant area. Planarization is also a concern of LOCOS as there are no polishing steps typically involved in the LOCOS formation.

Shallow Trench Isolation provides a solution to many of the concerns and disadvantages that LOCOS possesses with the main cost of adding complexity to the process. The additional complexity is due to need for an anisotropic silicon etch, tetra-ethyl ortho-silicate (TEOS) plasma enhanced chemical vapor deposition (PECVD), and chemical mechanical planarization (CMP) of the thick TEOS that was deposited, among additional simpler steps needed to process the wafers.

The anisotropic etch required for the trench formation is one of the key enabling technologies for STI. The goal of the etch is to etch the silicon at a fast rate with very steep sidewalls around 85° to usually just shy of 90° and not etch or undercut the etch masking layers at all. This means that the etch must be done using highly anisotropic dry etching techniques. Dry etching is used due to the fact that the level of anisotropy can be controlled as well as the sidewall angles. Reactive Ion Etching, or RIE as it is usually referred to, is a type of dry etching technique that combines two components of etching: Physically and Chemically. The physical etching component is usually governed by pressure and presence of ions which are driven to the substrate surface with the purpose to impart momentum on the surface atoms or molecules, causing the atoms or molecules to leave the surface in a way similar to sputtering. The ions do no typically react at the surface, and so RIE is actually a misnomer because in actuality it is ion-assisted etching. The physical component provides the anisotropic portion of the etch, but is typically slow and etches everything at the same rate. The chemical component of the process is similar to a chemical vapor deposition process except instead of the products depositing on the surface it leaves the surface. The reactant radical (a charge neutral atom/molecule with open valence electrons causing it to be reactive) diffuses from the plasma to the surface of the substrate, absorbs to the surface, reacts with the surface molecules, becomes a volatile product, desorbs from the surface and is swept away in to the vacuum system of the chamber. The chemical component of the etch is typically isotropic but provides very high etch rates and good selectivity between levels. Typically, the RIE of the silicon trench is performed at very low pressures, using a high density plasma generation system such as inductively coupled plasma (ICP), and a wide variety of chemistries both chlorine and/or fluorine based depending on the processes and the desired profile of the etch. Occasionally, some sidewall passivation of the etch needs to be performed depending on the desired depth to keep the sidewall angle

close to vertical and prevent undercutting of the masking layer(s).

Prior experimentation was performed at examining Shallow Trench Isolation feasibility and etch process characterization for RIT student factory processing. The first of the experiments examining the trench formation etch was performed in 2000 by Jerome Mc Naughton in which he examined sulfur hexafluoride (SF_6) and oxygen as the etch gases. The etch process was performed at 400 mTorr with 40 watts of forward power. The etch was highly isotropic due to the high pressure of the process along with the low power used for the etch. The high pressure and low power allows the etch process to be governed mostly by the chemical component of the RIE causing it to be mostly isotropic. The next experiment examining the etch process was performed by Patrick Reese in 2001. The results of his experimentation using a plasma mixture of SF_6 and tri-fluro methane (CHF_3) at 70 mTorr of pressure with ~270 watts of forward power yielded some results appearing to be anisotropic. However, the nitride masking layer was severely undercut by removal of the pad oxide layer below it. This was possibly due to the silicon etch process in combination with the use of a buffered oxide etch used to pattern the pad oxide prior to silicon etching. Etches greater than 0.5µm deep showed some isotropy in the etch profile when the cross-section was viewed in a SEM.

2. EXPERIMENT GOAL

The goal of this experiment it to provide the sub-micron CMOS process at RIT with an anisotropic etch of silicon to use in future implementation of STI. The etch needed to provide sidewall angles of 80° or greater with no undercutting of the silicon nitride or pad silicon dioxide layers and a depth of at least 0.5µm.

3. PROCEDURE

Since the goal of the etch is eventual implementation into the sub-micron CMOS factory process, much of the process flow leading up to the etch experiment was used. The starting substrate was an n-type wafer. The process started from the point where the n-well and p-well would have already been implanted and driven-in and the current process starts the LOCOS formation.

The substrates are first put into a diffusion furnace to grow 500Å of pad oxide. The purpose of the pad oxide is to reduce the stress of the subsequent silicon nitride layer on the silicon substrate. The pad oxide is grown at 1000°C for approximately an hour in an dry oxygen ambient. The growth was approximately 485Å. (See figure 1 for diagram)

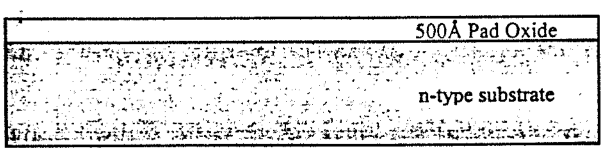

Figure 1

Wafers were then placed into an low pressure chemical vapor deposition (LPCVD) tube to deposit 3000Å of silicon nitride. Silicon nitride can multiple purposes in the process, such as an implant mask for the channel stop implant or an oxide growth mask in the case of LOCOS, but for this experiment it is being used preventative etch masking layer should the photoresist be completely removed. For further implementation, the nitride will provide a channel stop implant mask and a polish stop layer for the CMP of the TEOS fill. The nitride deposition ended up being ~2800Å thick.

After the nitride growth, wafers were coated with approximately ~1µm of photoresist using an SVG 88 coating system. Wafers were then exposed using a GCA 6700 g-line stepper for 0.3 seconds of exposure per die. The photoresist was then developed using the SVG 88 develop line. The resist was hard baked after development on the SVG track. (See figure 2 for diagram).

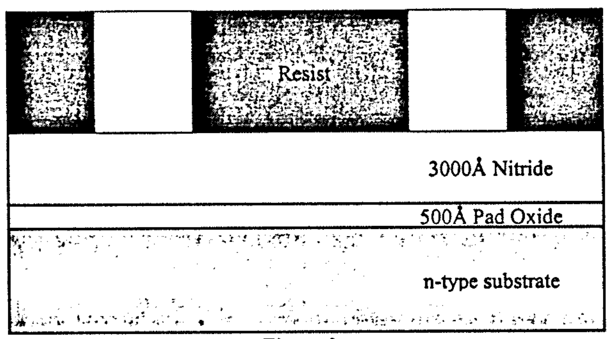

Figure 2

Wafers were then placed in the Drytek Quad 482 RIE system to pattern the nitride layer using the photoresist as the mask. The nitride was etched using a standard factory recipe consisting of 30 sccms of SF_6, 300 mTorr of pressure and 300 watts of forward power. This etch is fairly isotropic but it is used as the standard recipe for the process flow. The etch time used was about 3 minutes for an etch rate of about 1000Å/minute.

After the nitride was patterned, the pad oxide needed to be patterned. This process could have been done multiple

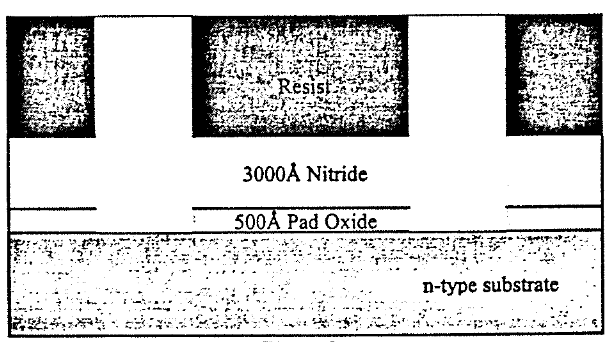

Figure 3

ways. The chosen was to again use RIE to pattern the oxide to avoid undercutting due use of buffered oxide etch which is incredibly isotropic. The oxide was etched using an oxide recipe in the quad that yielded ~450Å/minute thermal oxide etch rate. The process consisted of 70 sccms of CHF_3 and 10 sccms of O_2 with a forward power of 390 watts and a pressure of 70 mTorr. The etch was performed for 1 minute and 20 seconds to ensure that the pad oxide was etched through to the silicon. (See figure 3 for diagram)

The silicon etch was then examined. Knowing that low pressure was required to attain steep sidewalls, the pressure of the process was reduced to 40 mTorr. SF_6 is the main gas used to etch the silicon with the addition of oxygen to increase the etch rate of silicon and increase slightly the selectivity of the etch to the pad oxide. Argon was also added to promote more of a physical etch component to increase the ion bombardment of the surface and thus increasing the anisotropy of the etch.

Step heights were measured using a profilometer to ensure that the silicon was etched and to gather etch rate data. SEM cross-section were used to examine etch profile. (See figure 4 for diagram of ideal cross-section)

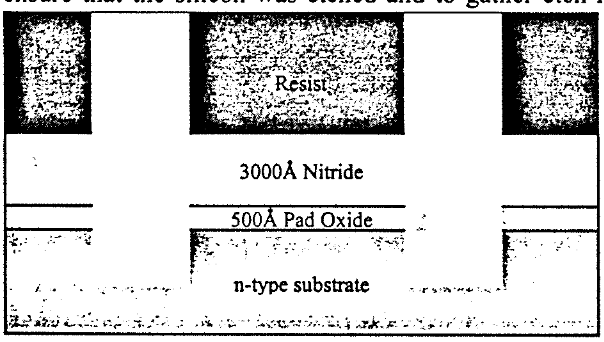

Figure 4

4. RESULTS

The initial results of the experimentation were measure by a profilometer to determine if the silicon was etched. Etch rates were also determined.

Table 1: Resulting Silicon Etch Rate

Run	Wafer	Oxygen (sccm)	Argon (sccm)	Etch Rate (Å/min)
1	5	20	0	6113
2	6	10	10	7935
3	9	20	10	4931
4	2	0	0	6418
5	10	20	20	4435
6	4	0	10	5333
7	8	10	20	6675
8	3	0	20	5398
9	7	10	0	8475

Cross-sections of the wafers with the fastest etch rates were performed The following figures represent wafers 6 and 7.

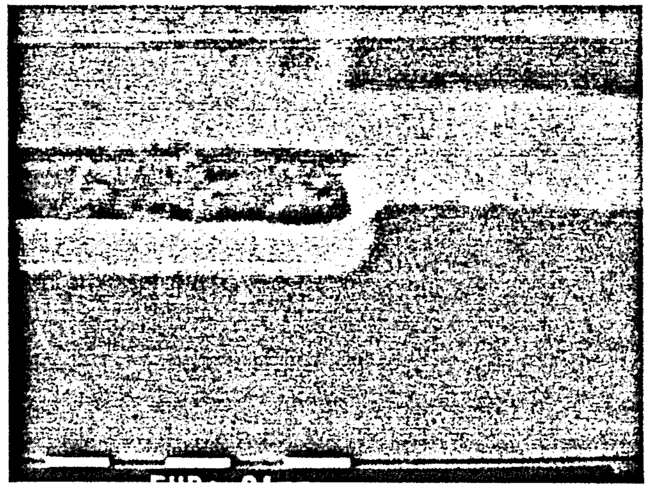

Figure 5: Wafer 6

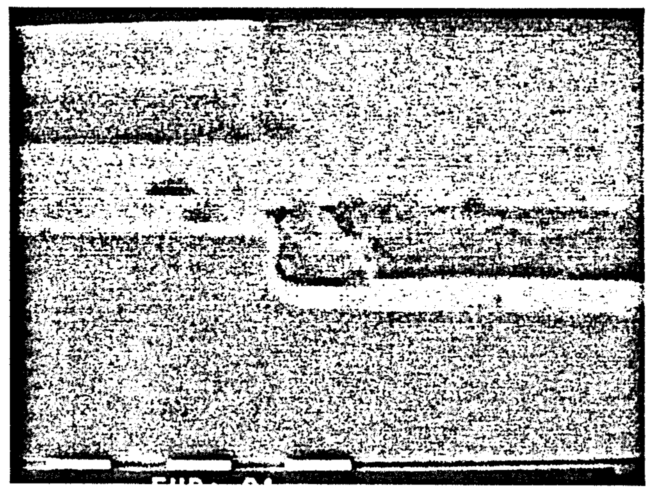

Figure 6: Wafer 6

Figure 5 and 6 are from wafer 6. The results show a slightly rounded bottom of the etch profile. The angle of the side wall is approximately 70°. It shows very limited undercutting of the nitride and oxide layers.

Wafer 7 (see figure 7) showed a slightly steeper sidewall of approximately 80°. This is close to the desired sidewall angle. The rounded bottom is also desirable due to allowing better filling of TEOS.

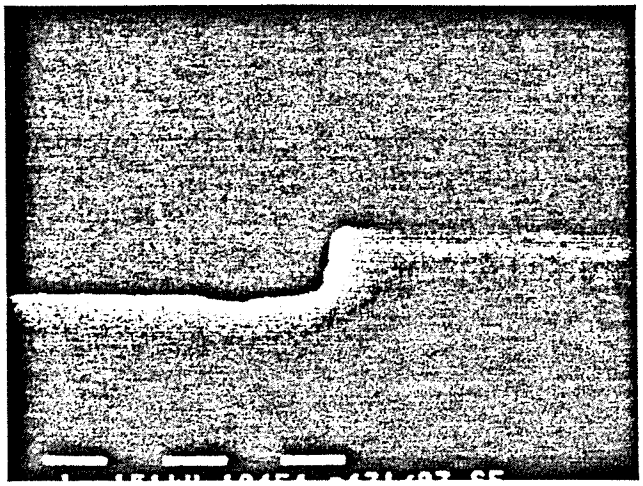

Figure 7: Wafer 7

5. CONCLUSIONS

An anisotropic etch of silicon is possible using the Drytek RIE tool. The optimal recipe examined was 30 sccms of SF_6 and 10 sccms of O_2 at a pressure of 40 mTorr and 200 watts forward power However, the further optimization of the etch process to produce steeper sidewalls approaching closer to 90° will need to be done as device sizes being fabricated decreases, this can be done by examining etch chemistries and processes utilizing sidewall passivation. By focusing on keeping the pressure low (40 mTorr) and the forward power high to promote the physical aspect of RIE.

Other tools could be looked at such as those utilizing a high density plasma system such as an ICP. RIT Semiconductor Microsystems Fabrication Laboratory (SMFL) has a tool such as this located in the cleanroom which is owned by Xerox and use is by permission. This tool could easily yield very steep sidewalls with a very high etch rate and excellent etch selectivity to a photoresist mask.

Other work that needs to be investigated for full implementation of STI is ion implantation of the channel stop implant in the p-well regions as well as PECVD of TEOS filling ability in the SMFL.

6. REFERENCES

[1] S. Wolf and R.N. Tauber, Silicon Processing for VLSI Era, Vol. 1-Process Technology, Chapter 16 – "Dry Etching for VLSI", Lattice Press, CA, 1986.

[2] S. Kurinec "Advanced Front End CMOS", Lecture 6. Dec. 2001.

[3] P. Reece "Dry Etch of Shallow Trench Isolation" Journal of Microelectronic Research Vol. XIX Rochester Institute of Technology, Microelectronic Engineering, May 2001

[4] J. Mc Naughton "Characterization and Development of Shallow Trench Isolation Process" Journal of Microelectronic Research Vol. XVIII, Rochester Institute of Technology, Microelectronic Engineering, May 2000

[5] L. Peters "Choices and Challenges for Shallow Trench Isolation" Semiconductor International, April 1999.

ACKNOWLEDGMENTS

The author would like to acknowledge and thank Dr. Lynn Fuller and Dr. Santosh Kurinec for guidance in this work. Bruce Tolleson and Jeff Peterson for equipment support. Michael Meagher and Erik Wheeler for processing help. Peter Terrana, Tina Prevost and Rich Battaglia for SEM help.

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