Analog IC Design and Fabrication

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Abstract-- The purpose of this project was to test the performance of analog integrated circuits and to characterize the MOSFET SPICE parameters. The data that can be obtained from this testing can be helpful for further research in the area of Analog IC design. The Semiconductor & Microsystems Fabrication Laboratory (SMFL) is a constantly evolving facility, with equipment constantly entering and leaving the lab. The process technology used was the RIT Subμ-CMOS Process, a vehicle used to teach students about process integration, semiconductor manufacturing, and the effects of process technology and device operation. Therefore, the Sub-Micron process must adapt to changes in the tool-set and still meet its process specifications. This project made minimal changes to the process.

1. INTRODUCTION

The device fabrication instruction laboratories at RIT have traditionally taken 8-9 weeks to complete. That leaves one or two weeks for device testing, in a traditional 10-week academic quarter. That amount of time is usually not sufficient for parameter extraction for device modeling and comparison to process variations.

The electrical devices currently fabricated at RIT are PMOSFETs, BJTs, and PMOSFETs with NMOSFETs in a CMOS technology. The PMOSFETs and BJTs are fabricated within one academic quarter, but the CMOS technologies can take several months to complete. There are two CMOS technologies being fabricated in the SMFL. CMOS fabrication is used as a vehicle to educate students about process integration, semiconductor fabrication, device physics, and digital and analog circuits.

The CMOS PW-3 process is an older technology that uses n+ poly gates, one level of metal, p-well technology and Field Oxide isolation. This technology is capable of MOSFETs with minimum channel lengths of 8μm. The Subμ-CMOS (Fig. 1) process is an improved PW-3 process. The process improvements include twin-well technology and Source/Drain Extensions (LDD). The minimum channel lengths that can be achieved on the Canon FPA 2000 i1 stepper are below 1μm.

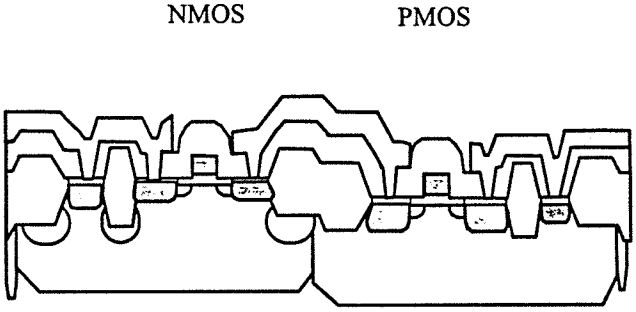

Figure 1. Subμ - CMOS process crossection.

The CMOS PW-3 test-chip had several analog circuits on it, including multiple operational amplifiers, digital to analog converters, analog to digital converters, voltage doublers, and other circuitry. The Subμ - CMOS process moved away from analog circuitry and only included two operational amplifiers to be tested. There is also a section in the testing sequence for extracting SPICE (Simulation Program with Integrated Circuit Emphasis) parameters for circuit modeling using RIT devices. The current time allotted for testing is not enough to extract SPICE parameters or to measure analog IC performance. These tests are necessary for accurate Analog IC design and fabrication to be performed at the RIT SMFL.

This paper presents an attempt at fabricating analog circuits designed at RIT for research purposes, in the SMFL. The approaches to this endeavor and the problems faced are documented. Improvements and suggestions are given to future investigators.

2. DEVELOPMENT

A. Circuit Layout and Simulation

The three circuits that were fabricated were a ring oscillator and two current amplifiers. The ring oscillator

was designed by Harikrishna Parthasarathy and the current amplifiers by Sripriya Bandi. They are both graduate students in the Electrical Engineering department at RIT. The ring oscillator (Fig. 2) was designed using regular CMOS technology. One of the purposes of the ring oscillator was to observe the effects of substrate noise on its operation. The current amplifiers (Fig. 3) were designed for use in CMOS imaging sensors. The low voltage requirements of many of today's circuits force many circuit designers to design in the current mode. The current amplifier contains a transconductance stage to transform an input signal into an output current.

B. Physical Layout

The physical layout was performed on the IC Station software on HP Workstations. Harikrishna and Sripriya's layout (Figure 4) was small enough that it could fit in the regular Subμ-CMOS Test-Chip (Figure 5). The only modification made to the Test-Chip was the removal of three ring oscillators near the middle of the design. The incorporation of the Test-Chip allows the use of alignment verniers, test devices, test structures, and the testing of the operational amplifier.

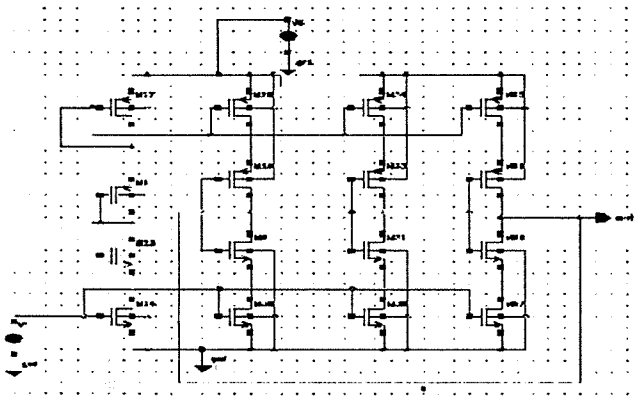

Figure 2. Ring oscillator designed by Harikrishna Parthasarathy.

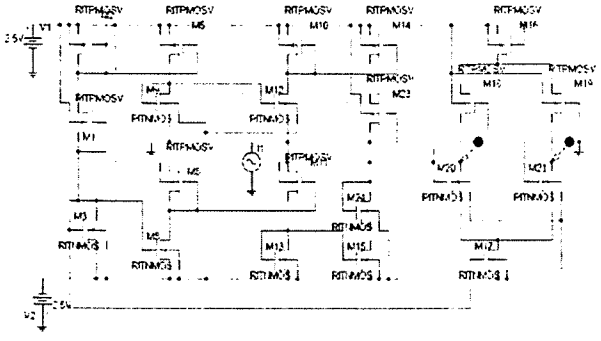

Figure 3. Current amplifier designed by Sripriya Bandi.

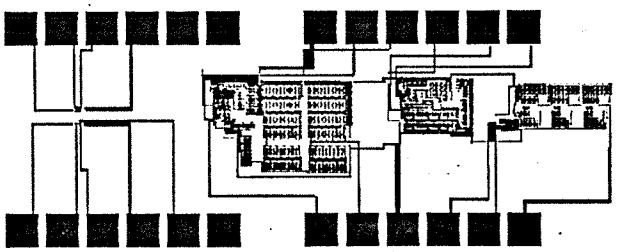

Figure 4. Physical layout of the ring oscillator and the two current amplifiers.

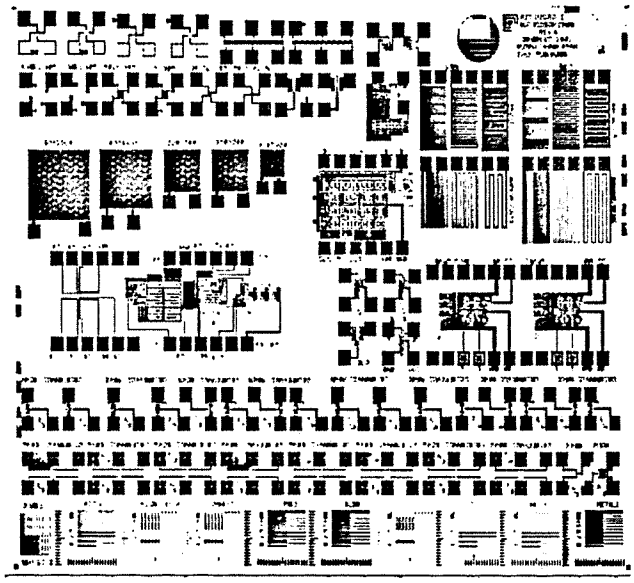

Figure 5. The ring oscillator and the current amplifier integrated into the RIT Subμ-CMOS Test-Chip.

C. Process Simulation

Process simulation using SUPREM-IV was performed on the Silvaco Athena software. Development and simulation of the Subμ-CMOS had already been done by Suraj Bhaskaran [1] for his Master's thesis at RIT. The simulation was needed for this project because the specifications were different for Harikrishna and Priya's devices. They specified a gate oxide of 500Å versus 150Å for the traditional process, and threshold voltages of +/- 0.5V for the NMOS and PMOS devices respectively, versus the traditional voltages of +/- 1V. The main components of the process that needed to be simulated were the gate oxide growth and the threshold voltage adjust implant. Table 1 below show the changes made to the process and Figure 5 display the simulated 2-D result of the MOSFET. The "+" notation for the V_T adjust dose

indicates using Boron ions and the "-" notation designate using Phosphorous ions.

	Process			
	Gate Oxide		V_T Adjust	
	Temp. (°C)	Time (min.)	Dose (ions/cm^2)	V_T (V)
Traditional	900	50	0	+1V
Traditional	900	50	+4E12	-1V
Adjusted	1000	47	-7.89E12	+0.5V
Adjusted	1000	47	+5.45E12	-0.5V

Table 1. Modifications made to the Subμ-CMOS process and the desired results.

3. FABRICATION

The fabrication sequence follows seventy processing steps. This includes eleven photolithography sequences. The Subμ-CMOS processing was done by Ivan Puchades for his Master's thesis and is currently processed regularly in the IC Processing Lab (0305-650). The processing targets are covered in detail in other sources [2], so they will not be discussed in this work. The only modifications made to the processing sequence were the gate oxide growth and the threshold voltage adjust implant.

The use of the Subμ-CMOS Test-Chip in the physical layout also allowed the Subμ-CMOS stepper job to be used in the GCA g-line stepper. The only modifications made to the stepper job were changes in the right and left key offsets. The original stepper job used key offsets of x = 2.198mm and y = -1.832mm. This resulted in alignment offsets between Level 1 and Level 2 lithography of as much as 4 μm on some areas of the wafer. The reason that the alignment was that poor was because there were changes made to the stepper alignment column after the stepper job was created. The stepper job was not updated to reflect these changes, thus the alignment suffered. The solution to this problem involved an iterative process. The alignment between the photomask and wafer is performed manually. The stepper keeps a record of how much the wafer was moved in the x and y direction to align the mask to the wafer. This number, the distance the wafer moved in the x and y direction, is added to the stepper job and the photolithography is repeated with the edited stepper job. This process is repeated until the desired alignment is reached. The best alignment was reached with x = 2.1956mm and y = -1.8378542mm with almost zero misalignment.

4. RESULTS

The fabrication sequence was only processed to step 40, which was Level 5 Lithography – Poly gate definition. The results from the processing steps actually performed are arranged in the following tables.

	Junction depth (μm)	Sheet Resistance (Ω/□)
N-well	N/A	301
P-well	1.65	995

Table 2. The junction depth and sheet resistance of the wells. The background substrate doping was n-type, therefore an n-well junction depth is not available.

Name	Temp (°C)	Time (min.)	Desired thickness (nm)	Measured thickness (nm)
Pad Oxide #1	1000	43	50	51
Alignment Oxide	1000	120	500	592
Pad Oxide #2	1000	43	50	47.7
Field Oxide	1100	50	650	538
Kooi Oxide	900	45	100	86.2
Gate Oxide	1000	43	50	49

Table 3. Results from all the oxide growths performed.

Name	Temp (°C)	Time (min.)	Desired thickness (nm)	Measured thickness (nm)
Nitride #1	810	17	150	291
Nitride #2	805	30	300	225
Poly	600	54	400	408

Table 4. Results from all the LPCVD film thickness.

5. DISCUSSION

A project of this magnitude requires at least two academic quarters, 20 weeks, to complete. The device fabrication alone takes as long as 14 hours a week for 10 weeks to complete. If the investigator has that much time to complete the project, then the other weeks can be used for circuit simulation, physical layout, and process simulation

The Subμ-CMOS does not currently have optimized processes running on the tools in the SMFL. The objective

of the Subμ-CMOS is to teach students about semiconductor manufacturing, not be a foundry process churning out product wafers. The goal of this project was to adapt the Subμ-CMOS into a process capable of fabricating working devices with a bent toward Analog IC research. Since the Subμ-CMOS process can be changed according to the research that is being performed, it is up to the investigator to determine how the process is to be edited. This work focused more on laying the groundwork for enabling further Analog IC research to be performed in the SMFL. Two practical ways to achieve these goals were to extract SPICE parameters from working devices and to test some working analog circuitry. The SPICE parameters allow circuit designers to model the devices in their circuit with the devices being fabricated in the SMFL. The successful fabrication of analog circuitry in the SMFL can be used to show that analog circuitry can be made and tested at the wafer level at RIT. It can used to show the performance of the processes at RIT.

Even though this project was not completed, the author hopes this work can be of some value to future investigators. It should be recognized that process development and simulation need to be performed in parallel with the circuit simulation. The complete process flow needs to be known by the time the mask is complete. When the mask is being designed, physical layout, intimate knowledge of the step and scan system being used for the process is needed. Knowledge of the stepper system allows the investigator to determine the adequate design rules to use in the layout. Minimum design rules might not always be the best rules to use, especially if the stepper system cannot meet those overlay requirements (Figure 6). Knowledge of the stepper system and mask fabrication can also allow the investigator to determine where alignment marks and such will be placed in the layout.

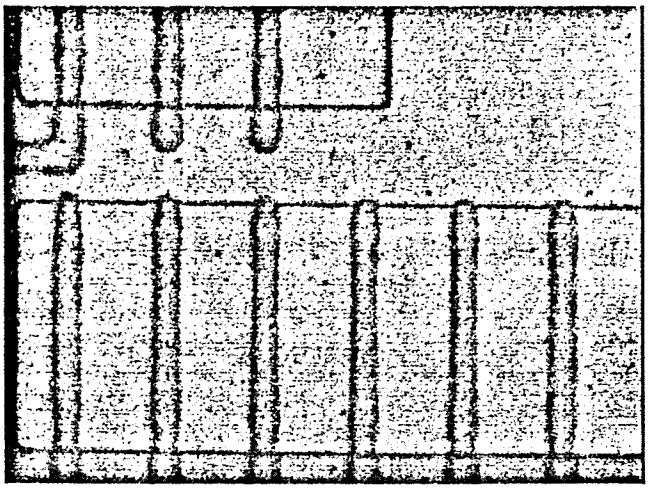

Figure 6. A possible short between the source and drain due to minimum design rules and bad overlay.

6. CONCLUSION

The RIT Subμ-CMOS process was used to fabricate Analog IC designs. The purpose of this project was to lay the groundwork for further Analog IC designs to be fabricated in the RIT SMFL. Analog IC design was chosen over other designs (digital, MEMS, etc.) because there is currently a deficiency in analog circuit and device testing in the Microelectronic Engineering department. Analog IC design complements the Microelectronic Engineering curriculum because it requires familiarity with semiconductor processing and semiconductor device physics. The author because of time constraints did not design the analog circuits, but the process simulation and fabrication were. The groundwork for further research would be accomplished by the following objectives of this project: Retrieve the SPICE parameters from the fabricated MOSFETs and test the analog circuitry. The SPICE parameters would be beneficial to future circuit designers intent on fabricating their design in the RIT SMFL, and the test results would provide a history for future reference.

The devices were only processed halfway in this project because of time constraints. The biggest issues with the processing involved reserving the tool for the actual processing. The obstacles involved in reserving a tool was that it needed to be up, and that it wasn't reserved by another party. This can be difficult if the tool was down often, or if different labs reserve the tool for the whole day. The processing that was done showed promise for working devices because the process parameters were within tolerance.

Researchers interested in fabricating circuits at RIT should have a timetable of at least two academic quarters. The first quarter needs to go into circuit simulation, physical layout and process simulation. A full process flow needs to be complete by the end of the first quarter. The fabricator needs to be certified on all the tools needed for the process ahead of time. The second quarter needs to be used for fabrication and testing. A schedule for the processing needs to be created and followed for deadlines to be met. Attention to details must be followed for all of these activities because any mistakes in any of the stages (circuit simulation, physical layout, process simulation or processing) can result in failure during electrical test.

REFERENCES

[1] S. Bhaskaran, "Design of RIT's Sub-Micron CMOS Process", Rochester, NY, 2000

[2] L. Fuller, "RIT's Advanced CMOS Process (1.0μm and 0.5μm)", PowerPoint Presentation, 2001

ACKNOWLEDGMENTS

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James Tom, originally from New York City, NY, received the B.S. in Microelectronic Engineering from the Rochester Institute of Technology in 2002. He attained co-op work experience at Lucent Technologies in 2000 and at the RIT SMFL in 2001. He is joining Intel Corporation as a product-engineering co-op for his last co-op assignment.