Raised Polysilicon Source / Drain FinFET Fabrication

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Abstract—The FinFET is a novel transistor that is fabricated using silicon on insulator (SOI) technology. The body of the transistor is etched out of the top layer of silicon. The device's polysilicon source / drain are deposited. The gate is self-aligned to the source drain. Contact cuts are made and metal is etched and patterned. The devices did not show field effect as anticipated. Analysis suggested breakdown of the gate oxide.

1. INTRODUCTION

The need for sub-50 nm transistor technology is forcing the microelectronics industry to examine various design schemes to successfully circumvent short channel effects and punch-through. One of the devices capable of achieving this is called a FinFET, a self-aligned double gate silicon device that is scalable down to 20 nm. The FinFET fabricated in this project was processed using g-line lithography, making the actual gate and fin size closer to 1 micron. While this is much larger than devices that have already been fabricated it shows that RIT has the capacity to develop these devices. A cross section of the polysilicon source/drain FinFET is seen in figure 1 [3].

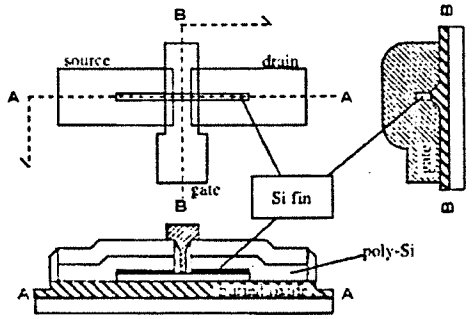

Fig. 1. FinFET typical layout and schematic cross sectional structures.

The FinFET overcomes many of the problems associated with scaling down silicon transistors. These include punch-through, where the drain and source depletion regions reach each other, creating an electrical short without any influence from the gate. Another problem that results from scaling down silicon transistors is that of oxide tunneling. This occurs when the electric field that the gate oxide experiences is greater than 4 MV/cm (80% of Fowler-Nordheim Tunneling), a serious problem as gates are becoming sub-40 Å in an effort to control the ever shrinking gate. Even at 40 Å the maximum voltage that can be applied to the gate is 1.6 V.

The channel of the FinFET is defined by the fin, a thin structure fabricated from the single crystal silicon of the SOI wafer. The advantage of the fin is using only the silicon necessary for the transistor, reducing short channel effects by effectively removing a path for shorts to occur. A thin fin also allows for a fully depleted device that will conduct current more readily when turned on and be much less likely to leak current when off.

The FinFET is a quasi-planar device, unlike a traditional MOSFET that is much more planar. This is because the source and drain of the FinFET are deposited polysilicon instead of bulk silicon. By engineering the height of the source and drain the parasitic resistance of the device can be reduced, resulting in a higher drive current.

The FinFET is also a double gate device, as the gate wraps around the thin fin. The double gate increases the gate control of the device. This raises drive current and reduces power consumption.

2. DEVICE FABRICATION

This process uses pre-existing semiconductor processing technologies. Five photolithographic layers were used to fabricate the FinFET. These layers are: Fin Etch, Poly 1 (source/drain), Poly 2 (gate), Contact and Metal. All lithography will be performed using the GCA 6700 tool.

The device design was an array of fins that ranged from 1 micron to 3 microns in 0.5 micron steps in the x-direction and from 1 fin to 5 fins in the y-direction. This design should allow comparison between fin size and

number of fins and the influence they have on transistor characteristics.

Both single crystal silicon and polysilicon were etched using a deep reactive ion etch tool. The process gasses used in the DRIE tool were SF_6 and C_4H_8. This provided the necessary selectivity between silicon dioxide and silicon, that allowed for a very thin masking silicon dioxide layer to be used.

The process flow employed is given below:

1. RCA clean SOI wafers
2. Grow SiO_2 – 150 Å
3. Deposit Si_3N_4 – 250 Å
4. Photo 1 – Fin Etch
5. Etch SiO_2/Si_3N_4 stack
6. Etch silicon using DRIE
7. Deposit polysilicon source / drain
8. Lightly dope polysilicon via spin on dopant
9. Deposit CVD oxide (Low Temperature Oxide)
10. Photo 2 – Poly 1 (Source/Drain)
11. Etch CVD oxide and polysilicon. The SiO_2/Si_3N_4 stack protects the fin.
12. Dry oxide to form SiO_2 spacers, insulating the drain and source from the gate
13. Deposit polysilicon as gate
14. Photo 3 – Poly 2 (Gate)
15. Etch polysilicon, stopping on CVD oxide
16. Photo 4 – Contact
17. Etch CVD oxide
18. Deposit aluminum
19. Photo 5 – Metal

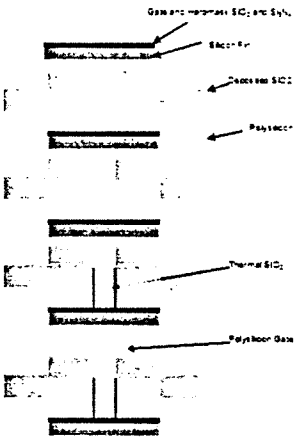

Figure 2. Process flow for the poly S/D FinFET fabrication

Figure 2 illustrates the cross-sections of the major processing steps which the FinFET undergoes. First the fin is defined. Second polysilicon and silicon dioxide is deposited. Lithography is performed on the devices and the source and drain are etched. A side wall oxide is grown to insulate the gate from the source/drain structure. Finally polysilicon is deposited and patterned to form the self-aligned gate structure.

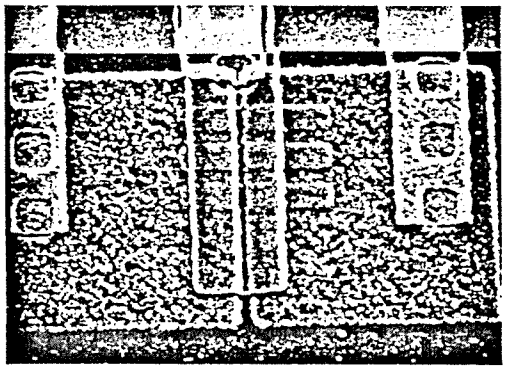

Figure 3 Scanning electron microscope image of a finished 3 micron by 3 fin device.

3. RESULTS AND DISCUSSION

Both single-crystal fin and polysilicon fin devices were fabricated through all device steps. Each device was tested using an HP-4145 Semiconductor Parameter Analyzer, however neither device produced a field effect.

The single-crystal device functionality was compromised by processing. The chemical vapor deposition oxide (LTO) that was to act as an insulating layer between the device and aluminum was not fully removed in the contact layer etch. The polysilicon devices did not exhibit any field effect. The following graph (Figure 4) was obtained from the parameter analyzer (HP-4145) and represents log I_D versus V_{DS}.

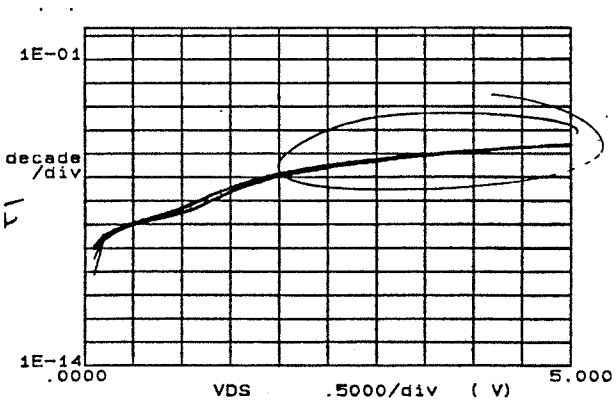

Figure 4 I_D versus V_{DS}.characteristics of a poly S/D FinFET device.

There appears to be a linear fit to the graph. This suggested Fowler-Nordheim testing. An analysis of

Fowler-Nordheim was conducted by examining the following equation.

$$J = A_F \varepsilon_{OX}^2 \exp(-B/\varepsilon_{OX}) \quad (1)$$

Equation 1 can be rewritten rearranging into current from current density and removing the exponential by examining the natural logarithm of equation 1. This gives equation 2.

$$\ln\left(\frac{I \cdot t^2}{V_{ox}^2}\right) = C - \frac{B \cdot t}{V_{ox}} \quad (2)$$

Where t is oxide thickness, V_{ox} is the voltage across the oxide and B is the activation energy.

An analysis of the data produced an activation energy, B ~48 MV/cm. Fowler-Nordheim has a B ~ 250 MV/cm. This data suggests that there are additional mechanisms to the tunneling in addition to Fowler-Nordheim tunneling. These tunneling mechanisms continue to be explored. A thicker gate and sidewall oxide should eliminate any tunneling and produce working transistors.

4. CONCLUSION

The fabrication of a novel device was completed using the Semiconductor and Microsystems Fabrication Laboratory at Rochester Institute of Technology. This process used a self-aligned double gate structure with raised polysilicon source/drain that should act to suppress short channel effects and parasitic resistance. Although a field effect was not observed, possible process improvements have been examined and will be explored in future device designs.

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Christopher Harvey, originally from Rochester, NY, received a B.S in Microelectronic Engineering from Rochester Institute of Technology in 2002. He attained co-op work at Analog Devices Inc. and Xerox Corporation. He is attending Rochester Institute of Technology for an M.S. in Microelectronic Manufacturing Engineering starting September 2002.