Design, Fabrication, and Testing of Crystalline Silicon Source/Drain FinFETs

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Abstract-- Crystalline silicon source/drain FinFET structures were designed, fabricated, and tested at the RIT Semiconductor & Microsystems Fabrication Laboratory (SMFL). Process development was completed using hand calculations, simulations, and similar processing techniques based upon mature RIT semiconductor manufacturing processes. The design under investigation is a dog-bone structure fabricated on SOI substrates. The crystalline silicon source/drain FinFETs exhibited a field effect behavior for all transistor sizes fabricated, however the smaller 1μm FinFETs were more susceptible to background noise. The smallest device, a 1x2μm FinFET yielded V_T=1.53V and a drive current of 510 μA with V_G=5V. The largest device, a 4x80μm FinFET yielded V_T=1.42V and a drive current of 4.1 mA with V_G=5V..

1. INTRODUCTION

The pace at which MOSFET (Metal-Oxide-Semiconductor Field-Effect-Transistor) scaling occurs will undoubtedly result in the introduction of new device technologies as scaling limits are met. One such emerging device is referred to as a FinFET (Fin Field Effect Transistor), in which the body of the transistor is a fin of crystalline silicon and an induced electric field creates a channel through which current flows. The FinFET structure is strictly fabricated upon Silicon-On-Insulator (SOI) substrates.

Numerous design variations of the FinFET exist, however the scope of this work consists of the design, fabrication, and electrical characterization of a crystalline silicon source/drain FinFET.

2. DEVICE THEORY

SOI wafers formed by a SIMOX process (Separation by Implanted Oxygen) utilize an oxide layer buried beneath the crystalline silicon surface of the wafer. These substrates provide an insulating barrier significantly reducing the junction capacitances between device regions and the bulk substrate, thus nearly eliminating the short-channel effects. This results in faster transistor switching times as well as reduced power consumption.

The FinFET is a completely isolated device due to its fabrication on SOI substrates in which the entire silicon surface is removed with exception for that needed to define the body and source/drain regions. A FinFET is a type of double gate MOSFET device that features a gate wrapped around a thin silicon body (fin) in which the source and drain of the transistor protrude from either side of the gate as shown in figure 1.

Figure 1: FinFET and X-section

Ideally in operation, the entire fin region would be fully depleted by the gate allowing current to flow between source and drain. The channel is defined by the width and height of the 'fin' and channel length is defined by the polysilicon gate width. This structure results in better control of the conductive channel as well as an increase in drive current.

FinFET designs can include differing transistor body (fin) structures and differing transistor source/drain structures. For example, a raised polysilicon source/drain region reduces the source/drain resistance of the device, but adds complexity to the design and fabrication.

3. DEVICE DEVELOPMENT & FABRICATION

The specific FinFET design investigated at RIT was an n-channel planar crystalline silicon source/drain FinFET due to its ease of fabrication, thus greatly improving the likelihood of achieving operational devices. Figure 2 on the following page shows a simplified example of the device processed at the RIT SMFL (not including metal connections to the device). The crystalline silicon source/drain regions are defined by the same etch process, which creates the fin of the FinFET.

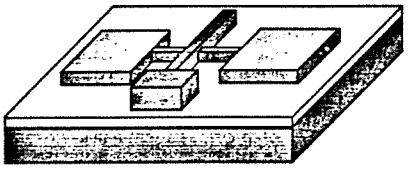

Figure 2: Planar FinFET Design

A. Device Design

The photomask of the FinFET design consisted of various polysilicon gate and fin width dimensions including 1, 2, and 4μm geometries. The number of fins between source/drain regions for which the gate controlled included 1, 2, 5, 10, and 20 fin combinations laid out similar to figure 3 below.

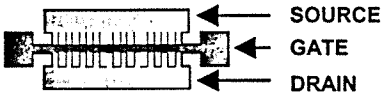

Figure 3: Fin Configuration of the FinFET

B. Device Fabrication

Starting substrates were p-type SOI with a buried oxide thickness of 3800Å and a 2000Å crystalline silicon surface layer. Pseudo SOI substrates were also fabricated with a grown oxide and deposited polysilicon surface layer with similar dimensions to that of the SOI substrates.

Process development was completed using hand calculations, simulations, and similar processing techniques based upon mature RIT SMFL semiconductor manufacturing processes. The FinFET fabrication process is briefly described in table 1.

1)	Photolithography – **Level 1: FinFET Source/Drain/Fin Definition**
2)	Silicon Etch
3)	Gate Oxide Growth - **150 Å, dry O2**
4)	Deposit Polycrystalline Silicon for Gate Material - **3000Å**
5)	Photolithography – **Level 2: FinFET Gate Definition**
6)	Polysilicon Etch
7)	Oxide Growth - **150Å, dry O2, poly oxidation**
8)	Ion Implantation - **1E15 ions/cm2, 75keV, P31**
9)	Implant Anneal
10)	LTO (Low Temperature Oxide) Deposition - **3000Å**
11)	Photolithography – **Level 3: Contact Cut Definition**
12)	Contact Cut Etch - **wet etch (BOE)**
13)	Metal Deposition - **Al, 6000Å**
14)	Photolithography – **Level 4: Metal Definition**
15)	Aluminum Etch & Sinter

Table 1: Process sequence for the FinFETfabrication

All photolithography steps were performed on a g-line (436nm) system. Silicon and polysilicon etches utilized a deep silicon reactive ion etch system.

C. Device SEM Images

Figures 4 and 5 are SEM (Scanning Electron Microscope) images taken after fabrication completion.

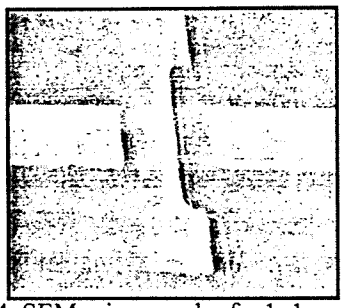

Figure 4: SEM micrograph of a 1x1μm FinFET

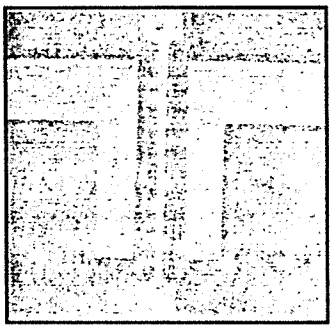

Figure 5: SEM micrograph of a 2x20μm FinFET (10 fins)

4. RESULTS & ANALYSIS

The fabricated crystalline silicon source/drain FinFETs exhibited the field effect behavior upon testing. Simple transistor characterization was done including transistor I_{DS}-V_{DS} (family-of-curves: FOC) plots and threshold voltage (V_T) extrapolation.

One of the smaller devices fabricated was a 1x2μm FinFET (μm gate width and fin width, 2 fins) shown in figure 6 exhibited a V_T=1.53V and a drive current of 510μA with V_G=5V demonstrated in figures 7 and 8 below.

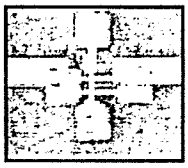

Figure 6: Micrograph of a 1x2μm FinFET

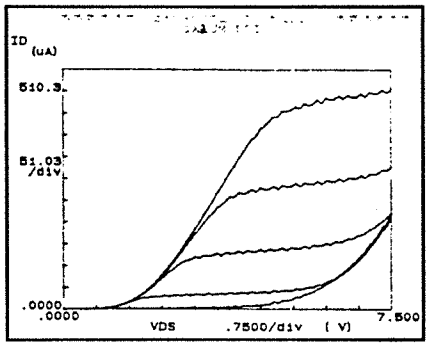

Figure 7:I_{DS} - V_{DS} characteristics for a 1x2μm FinFET

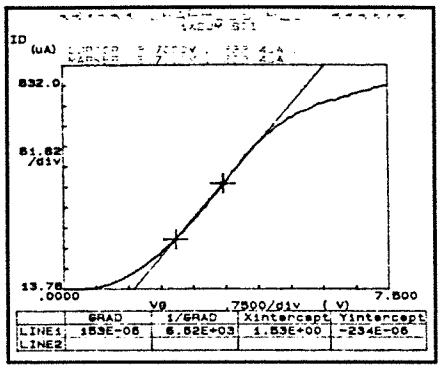

Figure 8: Transfer characteristics of a 1x2μm FinFET

Short channel effects seem to be apparent even with this design. Referring to figure 7, channel length modulation is visible in the family-of-curves as positive slopes in the saturation region. Background noise also appears as oscillations in device saturation. Junction breakdown occurs at low V_G values with increasing V_{DS} as the gate no longer has dominant control of the channel. Processing issues were determined to be the reason for the non-ohmic behavior (curvature at low V_{DS} of the output current) in the linear region of transistor operation. In figure 8, V_T is extrapolated as the x-intercept of the I_{DS}-V_{GS} plot with V_{DS}=5V. This plot also shows mobility degradation at high V_G values resulting in drive current roll-off in the plot.

The largest fabricated device tested was a 4x80μm FinFET (4μm gate width and fin width, 20 fins) shown in figure 9 exhibited a V_T=1.42V and a drive current of 4.1mA with V_G=5V demonstrated in figures 10 and 11.

Figure 9: Micrograph of a 4x80μm FinFET

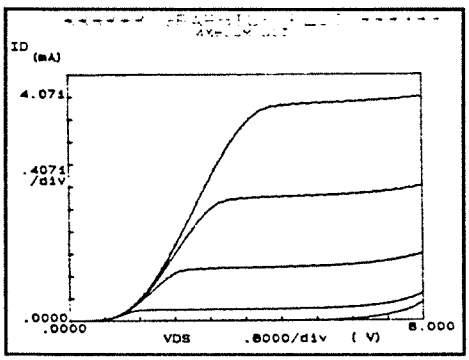

Figure 10: I_{DS} - V_{DS} characteristics for a 4x80μm FinFET

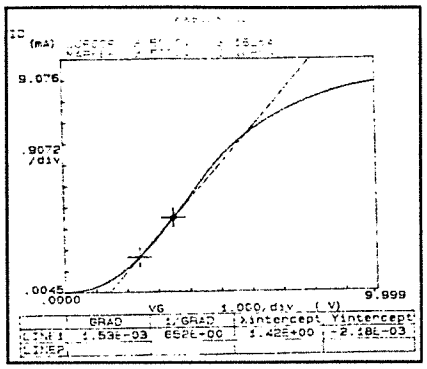

Figure 11:Transfer characteristics of a 4x80μm FinFET

Short channel effects are not quite as apparent in this larger device. Referring to figure 10, channel length modulation is minimal. Again, junction breakdown occurs at low V_G values with increasing V_{DS} as the gate no longer has dominant control of the channel. This larger device also exhibits the non-ohmic in the linear region of transistor operation. In figure 9, V_T is extrapolated as the x-intercept of the I_{DS}-V_{GS} plot with V_{DS}=5V. The larger device also shows mobility degradation at high V_G values resulting in drive current roll-off.

5. CONCLUSIONS

The successful design and fabrication of a planar crystalline silicon source/drain FinFET exhibiting transistor field effect behavior was completed at the RIT SMFL. This process used a self-aligned double gate structure with a planar crystalline source/drain structure, suppressing short channel effects and parasitic capacitance.

This work offered a proof of FinFET device concept resulting in knowledge gained from research and process development of a novel device structure. Upon completion, this project supplied the opportunity to apply Microelectronics undergraduate work at RIT to an emerging semiconductor device technology.

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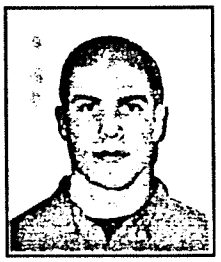
ACKNOWLEDGMENTS

The author acknowledges Dr. Kurinec as his advisor, IBIS Corporation in their donation of SOI substrates, Dr. Alan Raisanen as a silicon etch resource, Charles Gruener as a photomask resource, Jeff Peterson and Kevin Munger for their processing assistance, the RIT SMFL technicians and staff, Chris Harvey and all EMCR 2002 classmates for their support in the completion of this work.



Jesse Siman, originally from Eveleth, Minnesota, received a B.S. in Microelectronic Engineering from Rochester Institute of Technology in 2002. He attained co-op work experience at Cypress Semiconductor in Minnesota. He is joining Cypress in San Jose, California as a Product Marketing Engineer, starting July 2002.