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Investigations on Process Options Towards Improved Operation and Stability of IGZO TFTs

EMANUELLE CHOWDHRY
MAY 2024

A Thesis Submitted
In Partial Fulfillment
of the Requirements for the Degree of
Master of Science
in
Microelectronic Engineering

RIT | Kate Gleason College of Engineering

Department of Electrical and Microelectronic Engineering

Investigations on Process Options Towards Improved Operation and Stability of IGZO TFTs

Emanuelle Chowdhry

A thesis submitted in partial fulfillment of the requirements for the degree of
Master of Science in Microelectronic Engineering

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May 1, 2024

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ABSTRACT

Indium Gallium Zinc Oxide (IGZO) is an amorphous oxide semiconductor (AOS) being used in the display industry for backplane TFTs due to its superior mobility in comparison to hydrogenated amorphous silicon, as well as being compatible with the existing flat-panel manufacturing infrastructure. The ongoing research efforts primarily revolve around making the processing more robust so improved performance can be obtained and with greater consistency. The original proposed studies involved investigations on process options that promote enhanced passivation of defect states, and resistance to hydrogen plasma exposure to enable straightforward device integration schemes. However, during the beginning stages of experimentation there were problems identified that required a redirection of process development efforts.

This work specifically focuses on adhesion issues with the sputtered source/drain metal bilayer in bottom gate (BG) TFTs, which has become a more frequent observation in recent process lots, mostly in peripheral (non-device) regions. Apart from the process integration issue this challenge poses, there was also the concern that the reduced electrical performance might be linked to this phenomenon. An initial blanket wafer peeling experiment led to the hypothesis that some organic chemical residue from the positive resist lithography processing contaminated the IGZO surface causing the poor interface between the two layers. Treatment results also suggested that water adsorption may also be an issue on an exposed IGZO surface.

The proposed solution was to use an oxygen plasma treatment to remove any organic residue from the IGZO back-channel surface, immediately treat the wafer in HMDS vapor to render the surface hydrophobic, then process the wafers through the S/D lift-off lithography and sputter deposition processes within a short timeframe. The Trion Apollo ICP downstream plasma ash and oxygen RIE processes were investigated and found to promote metal adhesion on blanket

wafers, though only the ICP ash treatment was successful at preventing peripheral peeling on device wafers. Unfortunately, these treatments resulted in some compromise in the TFT operation resulting in gate leakage and lower breakdown strength. Further, the device characteristics were affected by trap states indicating some inefficacy of the passivation steps. The challenge that remains is finding an effective treatment that supports metal adhesion while being gentle enough to avoid device degradation. Possible options for further investigation to resolve the metal adhesion issues are discussed, which would enable the return to the original focus areas.

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CHAPTER 1. INTRODUCTION

1.1. Technology Background

Although silicon is the most popular choice of semiconductor for its abundance in nature, good carrier mobility, and comprehensive documentation of its characteristics, the need to investigate better-suited alternatives exists for a variety of specialized applications. Display screens are the application of interest in this research. Hydrogenated amorphous silicon (a-Si:H) has been the backbone of the display industry for the last several decades. However, due to its limited mobility, the industry has been looking for alternatives for higher performing TFTs. Figure 1.1 shows how the required channel mobility increases as the number of pixels increase, along with dependence on the refresh frequency [1]. As the demand for higher refresh rate and higher pixel count increases, the switching speed needs to increase which requires higher mobility.

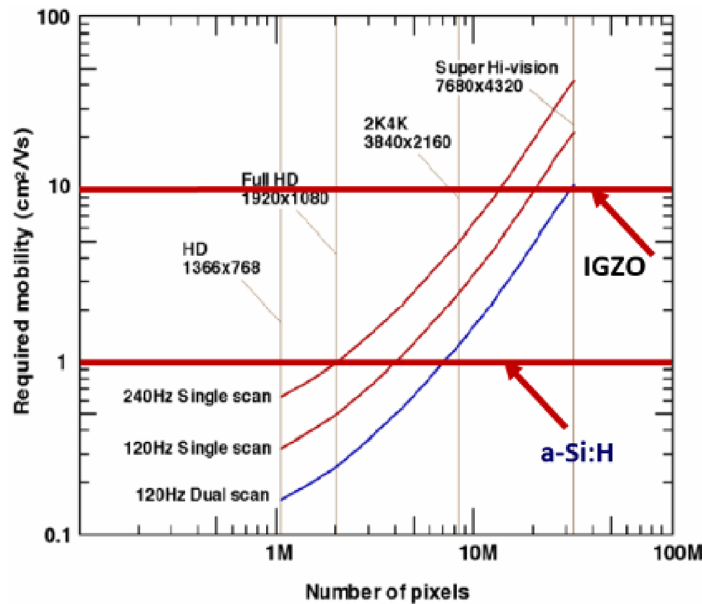


Fig. 1.1. Trend plot showing the required mobility for given number of pixels and refresh frequency. After [1].

One such alternative is the oxide-based semiconductor, Indium Gallium Zinc Oxide, or IGZO [2]. It is transparent (light stable) due to its wide band gap. It can utilize the installed base of a-Si fabs, which makes it attractive from a cost point of view. Sputter deposition without laser annealing makes it large-panel manufacturable. IGZO has approximately 10X the mobility of a-Si making it an attractive replacement candidate. As shown in Table 1.1, IGZO has a higher mobility than a-Si but doesn't not have as high mobility as Low Temperature Polycrystalline Silicon (LTPS). In addition, it cannot realize CMOS because the material supports free electrons only. However, the amorphous structure of IGZO supports excellent large-scale uniformity which is important for large panel manufacturing.

Table 1.1. Comparison of Basic Parameters of Major Semiconductor Material Options for Display Applications

Semiconductor	μ_{FE} (cm^2/Vs)	Large Scale Uniformity	Transistor Type
a-Si:H	<1	Good	NMOS
LTPS	>100	Poor	CMOS
a-IGZO	10-20	Good	NMOS

With regards to the TFT backplane configuration/design, the active-matrix coupled with a liquid crystal display (AMLCD) has been the most popular choice for flat panel displays (FPD) for its faster response rate, higher resolution and superior quality. The active-matrix mechanism has each pixel addressed to its own thin-film switching transistor, to increase refresh frequency, and storage capacitor to retain charge between refresh cycles to increase response time. Having a unique TFT addressing each individual liquid crystal improves speed of the on-off electrical signal. Passive matrixes use only wires in a grid configuration that uses integrated circuits to send voltage to the desired column and ground the desired row. This results in slower response time and poorer

voltage control, the latter effect often means the pixels adjacent to the addressed one also turn on partially (also known as Mura effect). A simple schematic representation of both passive and active matrix designs are shown in Fig. 1.2.

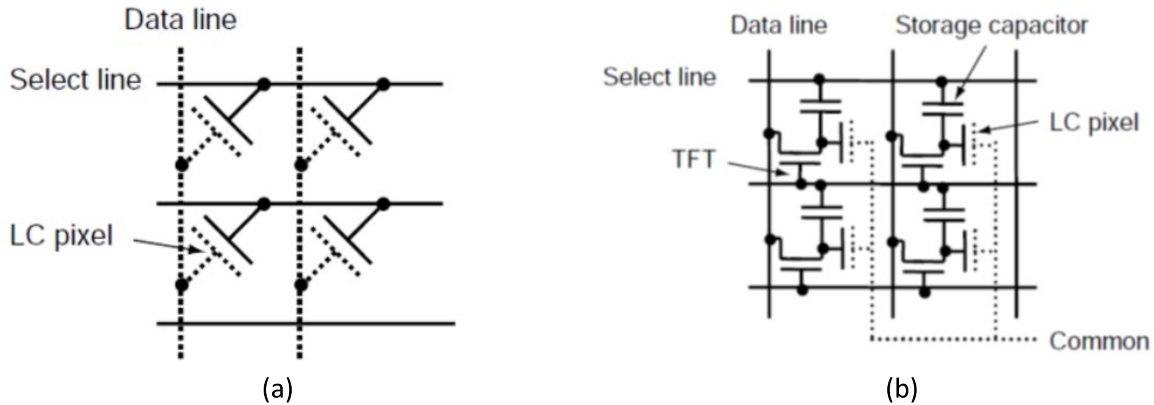


Fig. 1.2. LCD pixel addressing schematic designs: a) passive matrix and b) active matrix.

The display itself has a backlight, which used to be generated by Cold-Cathode Fluorescent Lamps (CCFLs) but is now generated by Light-Emitting Diodes (LEDs) for higher efficiency, illuminates the glass panel which consists of several layers over a diffuser which homogenizes the light. The critical layers consist of the liquid crystal sandwiched between two polarization filters perpendicularly oriented to each other. Unpolarized incident light from the source is polarized by the first of these filters. The second filter blocks out this polarized light when it is rotated by 90° with respect to the first polarizer. The liquid crystal rotates the light polarized by the first filter by 90° so it can pass through the second polarization filter by using a twisted-nematic liquid crystal structure which twists. See Figure 1.3 for general breakdown of the LCD layers.

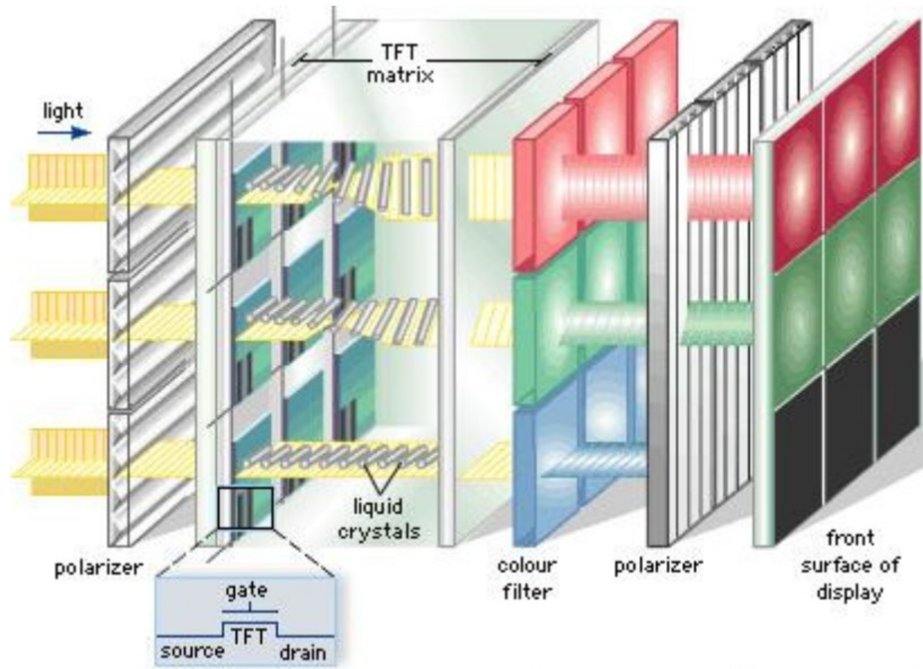


Fig. 1.3. Structure of LCD panel with TFT. From [3].

1.2. Advancements in IGZO Thin-Film Devices

Over this last decade there have been several advancements in the performance and stability of IGZO TFTs. There have been significant efforts toward improving stability and resistance to degradation due to aging, exposure to water, and process integration schemes that involve elevated temperature, i.e. $T \geq 200$ °C. Many of these investigations have been performed by members of the Thin-Film Electronics Group at the Rochester Institute of Technology, under the direction of Prof. K.D. Hirschman, with results reported in several reports. Early work was focused on the challenge of proper defect passivation of the IGZO channel and associated interfaces [4,5]. While there are different device electrode configuration options [5], the bottom-gate (BG) staggered contact configuration illustrated in Fig. 1.4 remains the industry standard due to performance and manufacturability. The baseline process has been largely unchanged for most

of the investigations, however key modifications led to improvements in device performance and stability [6,7]. Details and findings from these works will be referenced in the following sections.

1.3. Bottom-Gate IGZO TFT Process and Device Structure

The baseline process is started with ~650 nm of thick thermally grown SiO_2 to isolate the TFTs from the silicon substrate. While these devices would be normally fabricated on display glass, silicon substrates are typically used for a more robust substrate that is less susceptible to breakage and is more compatible with tooling and wafer handling sensors. The gate electrode consisting of 50 nm molybdenum was then sputter deposited and patterned using a reactive-ion etch (RIE) process, followed by a 50 nm PECVD SiO_2 gate oxide (TEOS precursor, 390 °C). The gate oxide is densified in the furnace for 2 hours in N_2 at 600 °C to improve chemical resistance and the dielectric properties.

The semiconducting body of IGZO (50 nm) was then sputtered deposited using an $InGaZnO_4$ (1:1:1:4) target in an argon ambient with 7% oxygen. This was done on an AMAT Centura system at the thin-films cleanroom facility at Corning Incorporated. The IGZO was patterned into mesas and etched using an HCl solution diluted with deionized water at a H_2O:HCl ratio of 10:1. A Mo-Al metal bilayer (50 nm + 50 nm, 100 nm total thickness) was then sputtered and defined into the S/D contacts by lift-off technique using Futurrex NR9g-1500PY negative photoresist which gives high contrast for sharp well defined shapes. The bilayer was chosen since Mo makes excellent electrical contacts with IGZO, and Al prevents oxidation during subsequent annealing in O_2 ambient. The devices were passivated with a second layer of 50 nm PECVD SiO_2, followed by a 3 hour anneal in O_2 at 400 °C plus a controlled ramp-down in O_2 for 2 hours. A 10 nm film of ALD (atomic layer deposition) Al_2O_3 was then deposited at 200 °C, serving as a capping layer to avoid the influence of H_2O [6,8]. The S/D and gate passivation-open windows

were patterned and etched using 10:1 buffered HF solution. Figure 1.4 shows the cross-section schematic and top-down view of the BG staggered device [7].

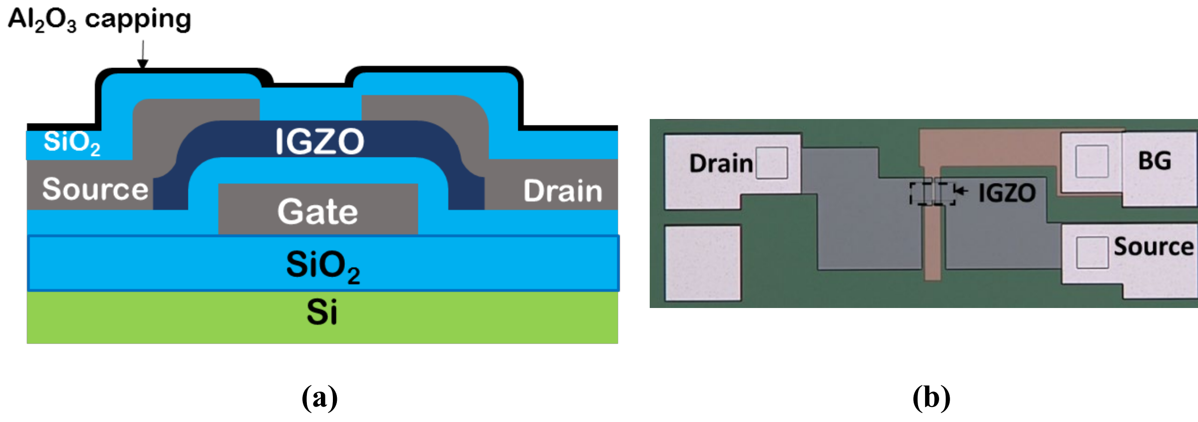


Fig. 1.4. (a) Cross-section schematic and (b) Labeled top-down view of BG staggered TFT. [7]

1.4. Key Process Modifications

Passivation and Annealing Adjustments

The use of a SiO_2 passivation layer at the IGZO back-channel (opposite the gate electrode) is preferable over other materials due to the compatibility of the PECVD process with large panel manufacturing. However, it was found that the parameters for the passivation dielectric and subsequent annealing processes were strongly coupled. Incomplete passivation resulted in degraded electrical characteristics, with typical results shown in Fig. 1.5 [5].

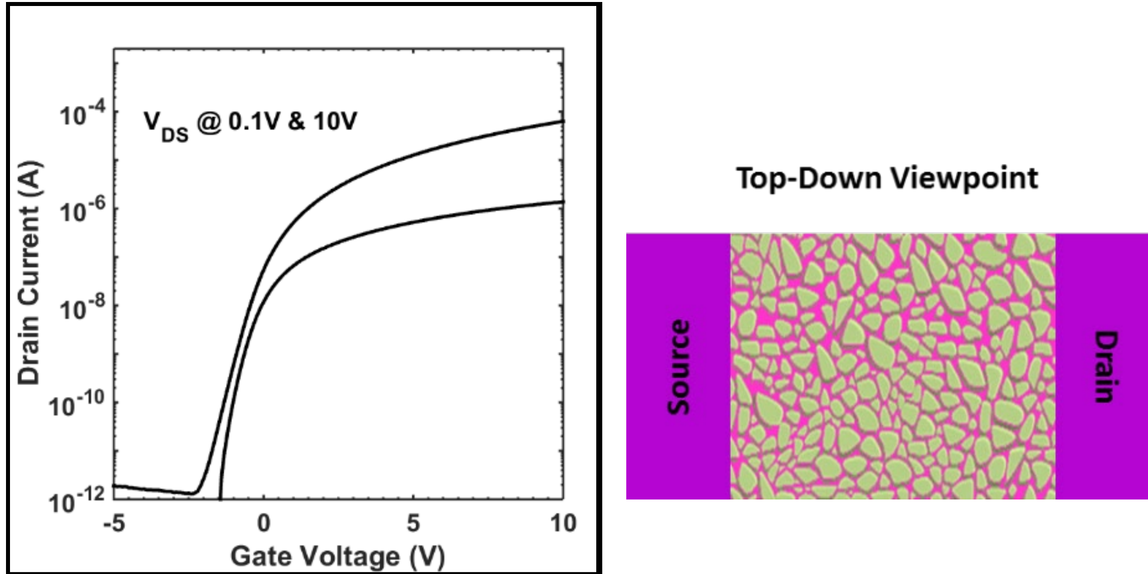


Fig. 1.5. (a) Transfer characteristics of BG long-channel (L=24 µm) device with 100 nm SiO_2 as the passivation layer, showing shallow subthreshold and DIBL-like separation between low and high drain bias curves. (b) Schematic model for the DIBL-like effect origin, since referred to as Trap-Associated Barrier Lowering (TABL). After [5].

The characteristics shown in Fig. 1.5 show a behavior qualitatively similar to Drain Induced Barrier Lowering (DIBL), however it appears on long-channel devices that should not experience DIBL. The passivation oxide on this device had a thickness of 100 nm, with an O_2 anneal for 4 hours at 400 °C followed by an extended O_2 ramp-down. The working hypothesis on this effect is inhomogeneity of trap states at the backchannel that presents regions with distinctly different effective interface charge levels. This results in a series/parallel network of channel regions to complete the electron pathway from source to drain, which was simulated in TCAD and shown to exhibit characteristics similar to that shown in Fig. 1.5(a) [5]. Given that this DIBL-like behavior was associated with interface traps, it was termed Trap-Associated Barrier Lowering (TABL). Adjustments were made to the passivation layer thickness and anneal processes in order to properly passivate the IGZO back-channel and suppress TABL [7]. The PECVD TEOS passivation oxide thickness was reduced to 50 nm, followed by a passivation anneal at 400ºC for 3 hours in O_2

ambient & 2-hour O_2 ramp-down. These adjustments resulted in a near-perfect overlay in the subthreshold region at different drain bias conditions.

ALD Al_2O_3 Capping Layer

To integrate TFTs into actual display products, elevated temperatures as high as 200 °C or higher may be required for bonding or packaging operations. Passivated BG devices demonstrated poor thermal stability when subjected to a 200°C hotplate bake, after which the I-V characteristics were noted to be markedly left shifted by several volts. The working hypothesis on the mechanism of this instability was based on water that was absorbed by the PECVD SiO_2 passivation layer [6]. Water molecules may participate directly as a donor [8], and/or react with underlying metal surfaces and release hydrogen which can act as a donor state in IGZO [9]. The solution that proved effective in promoting thermal stability was the incorporation of a 10 nm thick Al_2O_3 capping layer to serve as a barrier to H_2O atop the passivation oxide, deposited by atomic layer deposition (ALD) at 200 °C.

1.5. IGZO TFT Device Characteristics

The combination of the optimized passivation process and the ALD Al_2O_3 capping layer produced device characteristics among the best reported in the literature. Representative devices are shown in Fig. 1.6. The device shown in Fig. 1.6(b) is a “Golden Sample” which is used for experimental device comparisons as a reference of highest quality. In addition, Negative-Bias Stress (NBS) and Positive-Bias Stress (PBS) testing at +/- 10 V for 10k seconds or longer demonstrates excellent stability (not shown).

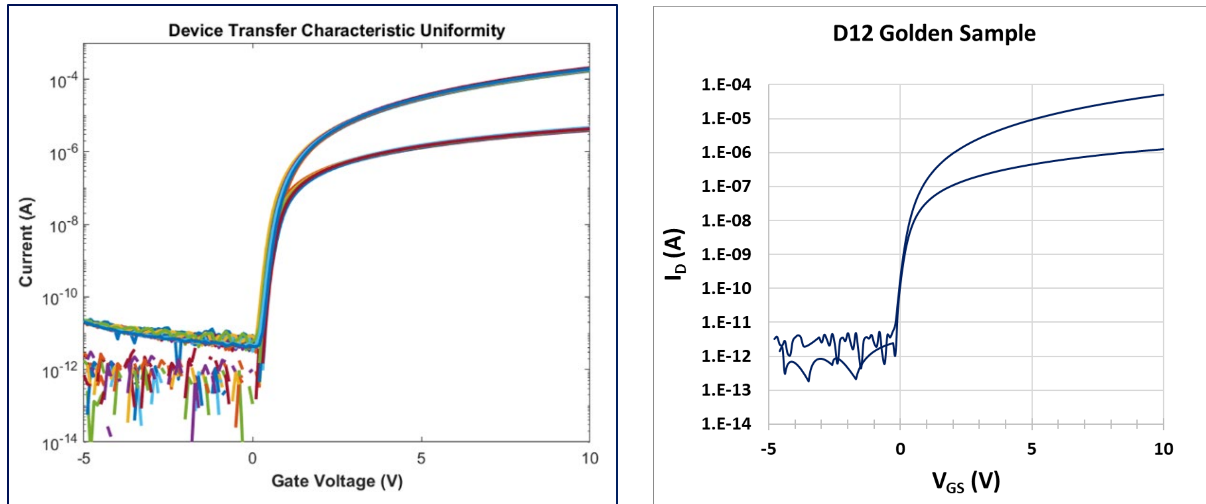


Fig. 1.6. (a) 25 device transfer characteristic overlay (L=4 µm, W=24 µm) demonstrating excellent consistency. (b) Golden Sample device (L=12 µm, W=24 µm) for comparison, with SS = 150 mV/dec. Drain bias conditions: V_{DS}=0.1 V, 10 V. Unpublished device characteristics, courtesy of E. Powell, RIT.

Along with advancements in device performance, there has been an increase in the understanding of the device physics involved in the transport properties of IGZO TFTs. Table 1.2 lists the material and device parameters that have been established for TCAD simulation [10,11]. Fundamental semiconductor parameters have been provided by various sources [12,13]. The parameters related to defect state distributions are adjusted to fit reference characteristics tested over a wide temperature range and verified accurate from 150 K to room temperature. A key contribution of this work was the validation of a thermally-activated diffusive mobility described by Wager [13].

Table 1.2. IGZO TFT Material & Device Parameters [10,11]

Parameter	Value
Band Gap (E_G)	3.05 eV
Electron Affinity (χ)	4.16 eV
Relative Permittivity (ε_r)	10
DOS Effective Mass (m_e^*)	$0.34 \cdot m_0$
RT Conduction Band DOS (N_C)	5×10^{18} cm^{-3}
Intrinsic Fermi Energy (E_i)	$E_{CME} - 0.37$ eV
RT Intrinsic Channel Mobility (μ_0)	19 cm^2/V·s
Band-Tail Acceptor States (Exponential)	
Peak @ $E = E_{CME}$: N_{TA}	3.25×10^{20} cm^{-3}eV^{-1}
Urbach energy: W_{TA}	0.02 eV
Integrated BTS: N_{BTS}	6.5×10^{18} cm^{-3}
Back-Channel Interface Trap Acceptor States (Exponential)	
Peak @ $E = E_{CME}$: N_{TA_IT}	5×10^{13} cm^{-2}eV^{-1}
Exponential decay: W_{TA_IT}	0.07 eV
Integrated IT: N_{IT}	3.5×10^{11} cm^{-2}
Oxygen Vacancy Donors V_O (Gaussian)	
Peak @ $E = E_{VO}$: N_{VO}	2×10^{16} cm^{-3}eV^{-1}
Mean energy: E_{VO}	2.9 eV
Standard deviation: W_{VO}	0.1 eV
Integrated Donor Concentration: $[V_O^+]$	4.7×10^{15} cm^{-3}

The passivation and capping layer modifications also enabled the scaling of devices to short-channel dimensions. Figure 1.7 shows a representative device with channel length L=2 μm showing excellent electrical characteristics and high thermal stability.

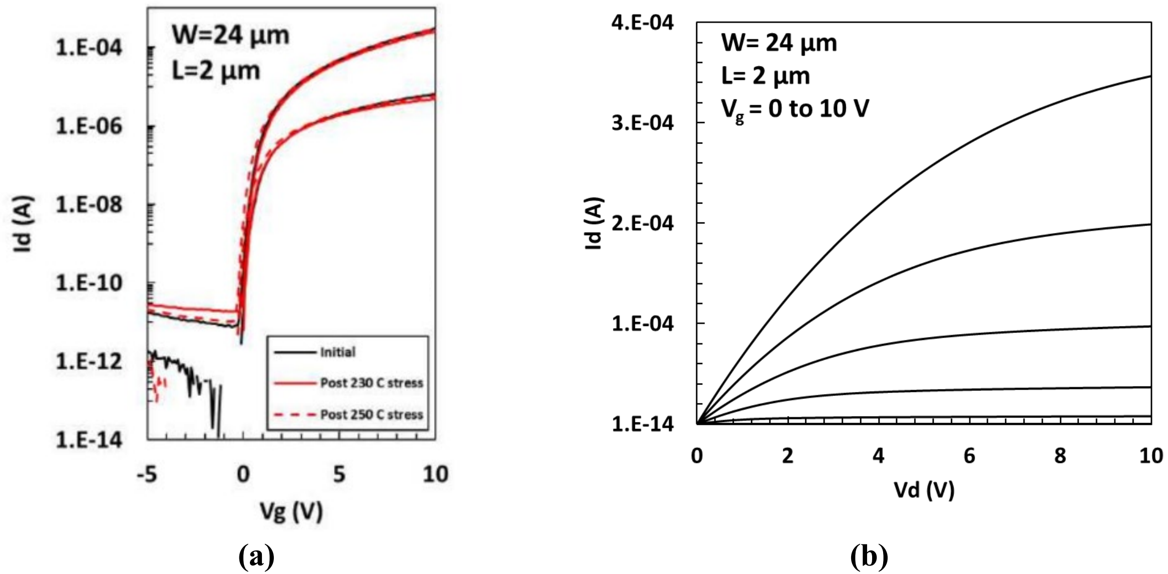


Fig. 1.7. Transfer characteristics (a) and output characteristics (b) of a representative bottom-gate TFT with 2 µm channel length. The device exhibits excellent thermal stability up to 1 hour at 250 °C [7].

Despite the reported progress in IGZO TFT performance and stability, room for improvement remains. There is a need to incorporate methods to fortify the devices through process options that will enable the integration into functional systems and preserve the improvements attained. This includes enhanced passivation of back-channel interface traps, and decreased sensitivity to hydrogen which is a common byproduct in plasma processing. Techniques to potentially address these issues are the focus of the next chapter.

CHAPTER 2. SUPPORTING RESEARCH AND PROPOSED STUDIES

2.1 Motivation for Proposed Studies

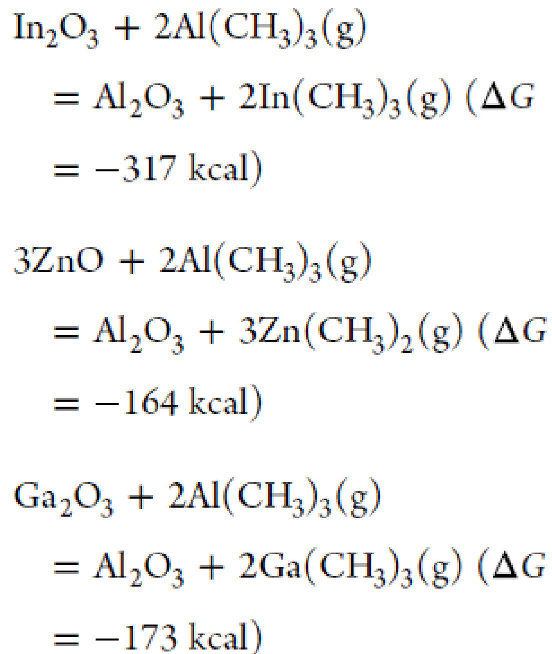
Although IGZO devices show very promising I-V characteristics, there are challenges associated with process integration with other devices, interconnects, etc. so that they can be incorporated in actual applications. The suspected presence of oxygen vacancies (V_o) is thought to make it difficult to passivate trap states at the IGZO interfaces and utilize alternative materials at the backchannel. The ability to use common plasma processes is limited due to exposure to hydrogen which behaves as a donor in IGZO, making it conductive. Process modifications have been investigated to address these issues, which was supposed to be the primary focus of this work.

Further improvements implemented by other research groups include the use of N_2O plasma treatment to suppress ALD Al_2O_3 aluminum precursor (TMA) reaction with IGZO metal cations [Li *et al*] and the use of O_3 oxidant for ALD Al_2O_3 instead of water [Lee *et al*]. The nitrous oxide plasma treatment of the a-IGZO channel surface prior to ozone alumina deposition seems to prevent Vo generation, –OH doping and interface traps. Using ozone creates an alumina that is a more effective hydrogen barrier to improve stability of the devices over time since it can getter the hydrogen in the more plentiful C-O bonds incorporated in the structure.

2.2. Improved Defect Passivation: Nitrous Oxide Plasma Treatment

In the reference titled, "*Near-Ideal Top-Gate Controllability of InGaZnO Thin-Film Transistors by Suppressing Interface Defects with an Ultrathin Atomic Layer Deposited Gate Insulator,"* by Li *et al* [14], nitrous oxide plasma was shown to suppress the interaction of the TMA (tri-methyl aluminum) precursor with the IGZO metal cations. According to the authors, the equations in Fig. 2.1 show the possible chemical reactions that may occur between the metal

cations and the tri-methyl aluminum precursor. These reactions are significantly enhanced by the presence of oxygen vacancy defects. The Hall measurement results in Fig. 2.2 show that the sheet resistance drops drastically without the nitrous plasma treatment, indicating that the introduction of oxygen during the N_2O plasma treatment reduces the number of donors like oxygen vacancies and hydroxyl groups which along with interface traps formed during ALD increase conductivity of IGZO. This is just like a porous surface and is more chemically reactive; oxygen vacancy gaps between the metal-oxide "molecules" allow for the TMA to react with those dangling bonds.



$$In_2O_3 + 2Al(CH_3)_3(g) = Al_2O_3 + 2In(CH_3)_3(g)\ (\Delta G = -317\ \text{kcal})$$

$$3ZnO + 2Al(CH_3)_3(g) = Al_2O_3 + 3Zn(CH_3)_2(g)\ (\Delta G = -164\ \text{kcal})$$

$$Ga_2O_3 + 2Al(CH_3)_3(g) = Al_2O_3 + 2Ga(CH_3)_3(g)\ (\Delta G = -173\ \text{kcal})$$

Fig. 2.1. Possible metal-oxide / TMA precursor reactions according to Li *et al.* [14]

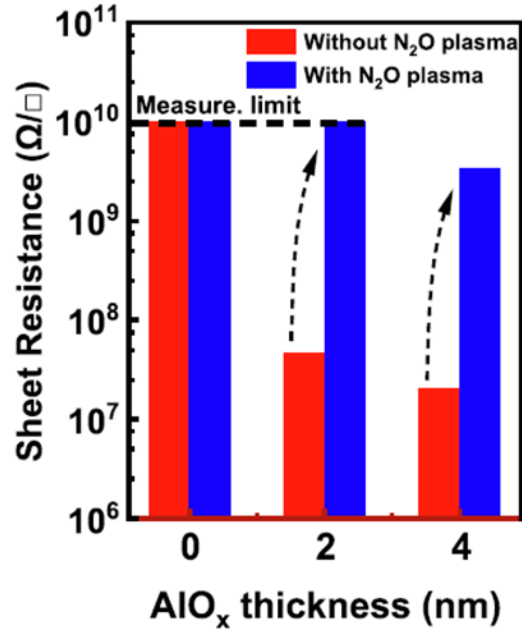


Fig. 2.2. Hall measurement results for AlOx-covered a-IGZO films w/wo N_2O plasma pretreatment. [14]

The authors looked at XPS plots of O1s peak for samples with and without N_2O plasma to verify V_o reduction (Fig. 2.3). The sample with N_2O plasma showed a decrease in the contribution of oxygen vacancy defects to the overall signal. While the difference in percentage appears relatively low, it is typical when comparing highly conductive and semiconducting IGZO samples.

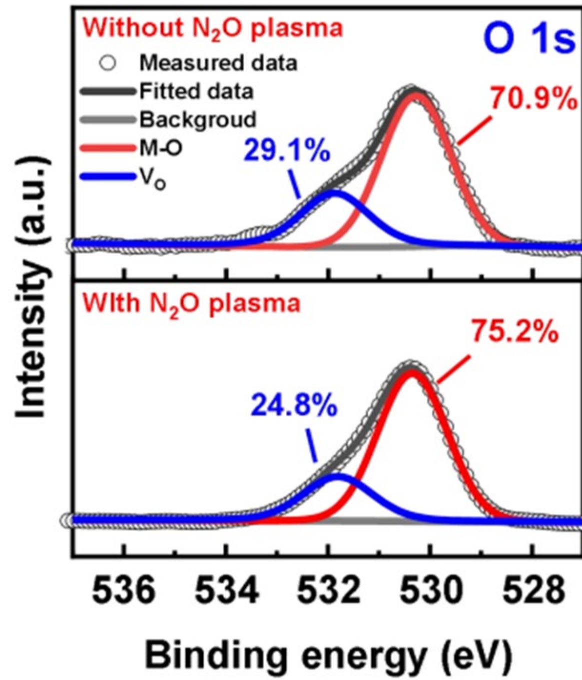


Fig. 2.3. XPS O1s signals for bare a-IGZO films without and with N_2O plasma treatment. [14]

Further reported benefits of the nitrous oxide plasma treatment were decreased subthreshold swing, hysteresis, and density of interface trap states, with the number of interface traps (N_{it}) seeing a 10x improvement with N_2O treatment (Table 2.1). While our process uses a PECVD SiO_2 passivation layer, the oxygen vacancy reduction benefit of the N_2O plasma treatment should translate and support a more effective passivation anneal to set the semiconductor properties of the IGZO.

Table 2.1: Performance Comparison w/wo N_2O Plasma Treatment

Dielectric	w/ N_2O	w/o N_2O
channel width/length (*W*/*L*)	20/9	20/9
SS (mV/dec)	60.8 ± 0.9	72.9 ± 0.3
N_{it} (eV^{-1} cm^{-2})	~ 1.40 × 10^{11}	~ 1.96 × 10^{12}
I_{on}/I_{off}	> 10^9	> 10^8
μ_{FE} (cm^2/V·s)	13.3 ± 0.6	9.8 ± 0.5
V_{th} (V)	0.20 ± 0.01	0.07 ± 0.01
Hysteresis (mV)	~ 4 mV	~ 25 mV

Secondly, post-passivation results, the same as the initial devices or better may be obtained without the need for such an aggressive passivation anneal thus saving time and potentially avoiding other process integration issues (discussed in chapter 3). The anneal may only fix V_o to a certain minimal level, regardless of time. A pre-anneal N_2O treatment may lower this plateau.

2.3. Resistance to H_2 Plasma Exposure: O_3 ALD Precursor

The reference, "*Hydrogen Barriers Based on Chemical Trapping Using Chemically Modulated Al2O3 Grown by Atomic Layer Deposition for InGaZnO Thin-Film Transistors,"* by Lee *et al* [15], is focused on the hydrogen resistance of ozone-ALD alumina which offers benefits in device stability and process integration. This work shows a significant improvement in using ozone as the oxidant in comparison to water. The authors showed that O_3-ALD Al_2O_3 back-channel passivation significantly promoted stability upon exposure to a H_2 plasma compared to H_2O-Al_2O_3 (Fig. 2.4), via its hydrogen getter mechanism.

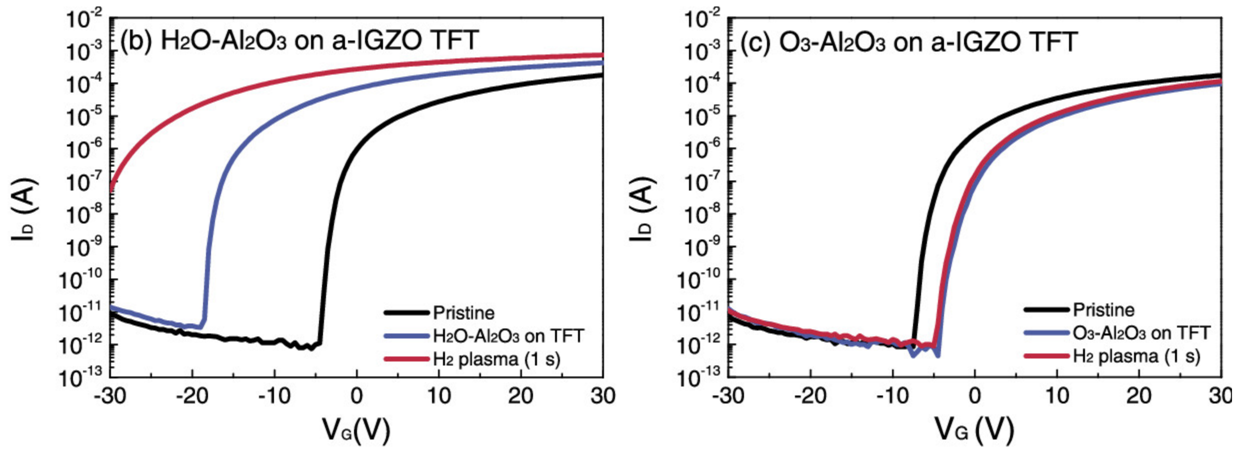


Fig. 2.4. Transfer characteristics of a-IGZO TFT after the deposition of the $H_2O-Al_2O_3$ (left) and $O_3-Al_2O_3$ (right) followed by hydrogen plasma treatment [Lee *et al*]. [15]

The left transfer characteristics show a significant left-shift upon water based alumina deposition (attributed to the formation of –OH donors) and a further shift upon hydrogen plasma exposure of 1 second. The ozone oxidant on the right results in a right-shift, with excellent stability when exposed to H_2 plasma. The authors have proposed that the H_2O-Al_2O_3 promotes adsorption and decomposition of H_2O leading to –OH donors, hence offering no resistance to H_2 plasma while O_3-Al_2O_3 demonstrates excellent resistance to H_2 plasma exposure due to the hydrogen gettering mechanism within the O_3-Al_2O_3 layer as described in Fig. 2.5.

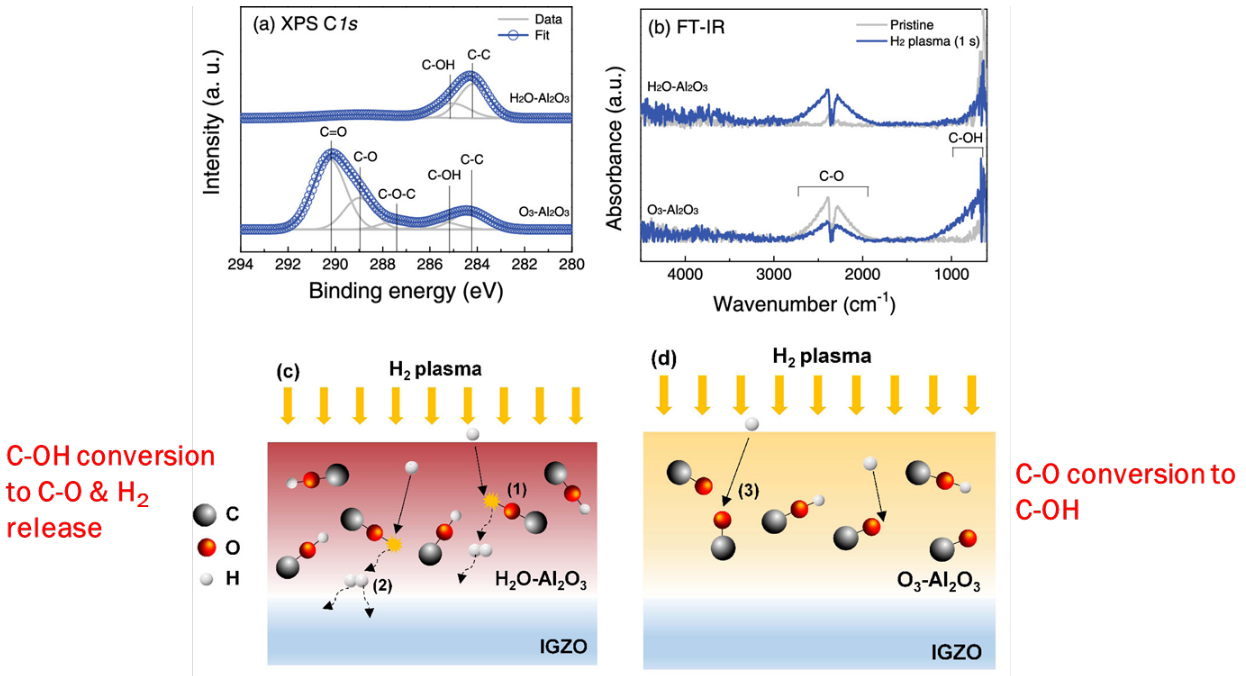


Fig. 2.5. (a) XPS spectra of the C1s core level: $H_2O–Al_2O_3$ (upper) and $O_3–Al_2O_3$ (lower). (b) FT-IR spectra of the $H_2O–Al_2O_3$ (upper) and $O_3–Al_2O_3$ (lower) before and after hydrogen plasma treatment. Schematic of possible reaction mechanisms in (c) $H_2O–Al_2O_3$ and (d) $O_3–Al_2O_3$. [15]

The XPS at the top left and the FT-IR at the top right of Fig. 2.5 provide evidence that backs up their hypothesis that in ozone-alumina there are enough C-O bonds available to getter hydrogen forming C-OH bonds, as represented in Fig. 2.5(d), which presents as an increase in both XPS and FT-IR signals. In the water-alumina there are significantly more C-OH bonds initially present, which decompose when exposed to excess hydrogen into C-O, as represented in Fig. 2.5(c), which results in the effusion of H_2. Whether the mechanism on the left or the right is operative seems to depend on the original concentration of C-O.

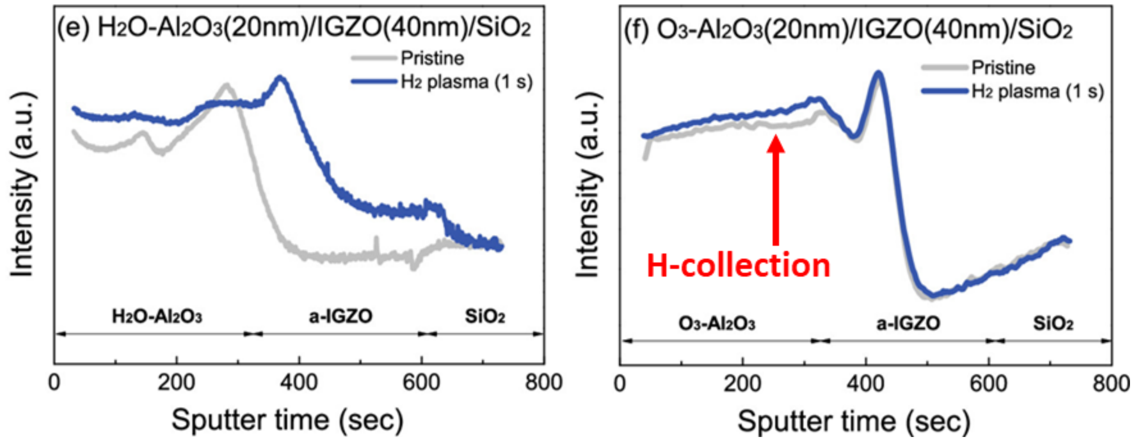


Fig. 2.6. Hydrogen SIMS depth profiles in a-IGZO (left) with H_2O-Al_2O_3 and (right) O_3-Al_2O_3 before and after hydrogen plasma treatment. [15]

There are also the SIMS depth profiles of both samples before and after exposure to hydrogen plasma in Fig. 2.6, showing a significant bump in the intensity of hydrogen detected in the body of the IGZO capped with water-alumina whereas there is no change in the IGZO capped with ozone-alumina. However, the passivation layer itself shows increased hydrogen content. This provides evidence of the benefits of the ozone oxidant in creating an effective hydrogen barrier. Based on the author's findings avoiding H_2O may offer some improvement in the initial device operation by reducing oxygen vacancies and avoiding –OH donor formation. It may also improve hydrogen plasma stability as a capping layer and might also be compatible as passivation layer directly on IGZO which may be of interest in future investigations.

2.4. Proposed Studies

Based on this preliminary research, it was decided to pursue two lines of investigation. The first study investigates the influence of a nitrous oxide plasma treatment to improve the quality of the IGZO surface (decrease defects) with a possible benefit of decreasing dependence on the aggressive passivation anneal. The N_2O plasma treatment would be performed on the Trion phantom III PECVD system, either just prior to S/D metal lift-off lithography or prior to the passivation oxide deposition. The second study investigates ozone as the oxidant for the ALD alumina capping layer, with the aim of increased resistance to hydrogen exposure in plasma processing. The ozone-alumina capping layer would potentially replace the water-alumina ALD process. The ozone-alumina process should offer excellent thermal stability as the presence of water is completely avoided, and improved resistance to H_2 plasma exposure is well supported. [15]

CHAPTER 3. EXPERIMENTS AND ANALYSIS

3.1. Process Challenges to Address

Before these improvements could be addressed in this research sudden issues that recently arose as part of the standard process needed to be investigated and fixed (before proceeding). The first problem was seen in the I-V characteristics in Fig. 3.1 which shows a shallow sub-threshold and notable separation between low& high drain bias curves. A shallow subthreshold is typically due to interface traps at the backchannel and separation is typically due to inhomogeneity i.e. variation in the trap state's physical distribution. The observation of both shallowness and separation is evidence of both issues. These issues became apparent in the summer of 2022 and have influenced several process lots.

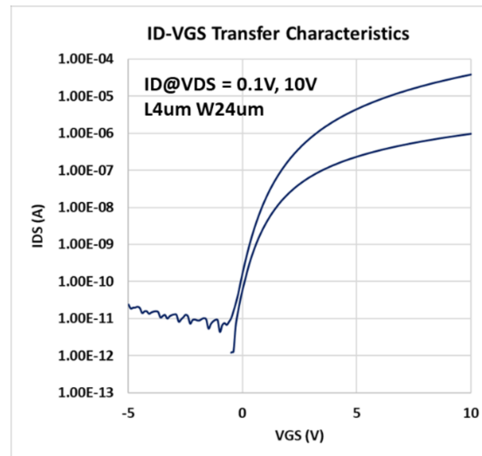


Fig. 3.1. Representative transfer characteristics measured on a recent device with compromised operation, exhibiting spreading and distortion with slight TABL.

The second issue observed was molybdenum/aluminum metal bilayer peeling off of the IGZO in the periphery of the wafers. This could be a potential factor in the compromised operation of the TFTs if the root cause interferes with backchannel passivation. To investigate this a peeling experiment was done and scotch tape was used to test adhesion which pulled of quite a bit of metal

on the IGZO monitor wafer (figure 5) on which the standard process flow that affects the source - drain(S/D) regions was followed.

Fig. 3.2. Peripheral metal peeling of the S/D Mo/Al bilayer on IGZO.

3.2. Peripheral Metal Peeling Investigation

Table 3.1. Peeling Experiment Summary

W#	Treatment prior to Mo/Al bilayer sputter (overnight pumpdown)	Mo/Al Peel?
1	Control – bare IGZO, no treatment	No*
2#	701 coat/dev/post-bake, NMP strip, HMDS + Futurrex/develop	Yes
3#	701 coat/dev/post-bake, Acetone/IPA strip, HMDS + Futurrex/develop	Yes
4	701 coat/dev/post-bake, Ash (180sec)	Yes
5	701 coat/dev/post-bake, Ash (180sec), HMDS + Futurrex/develop	No
6	504 coat/dev/post-bake, solvent strip, HMDS + Futurrex/develop	Yes

• Futurrex is negative-tone photoresist for metal lift-off process
* Control had minor localized peeling at one edge region
  - Note previous control had no peeling
Process of record (previous PRS2000 stripper)

The full peeling experiment listed in Table 3.1 consisted of one control wafer that was left untreated between the IGZO and sputter of metals, two wafers which followed the process of record since the NMP and acetone + IPA treatments were used interchangeably to strip resist, a fourth to isolate the effect of ashing, along with a fifth to see how ashing interacted with the rest of the usual process (Futurrex negative lift-off resist coat & develop), and a sixth using the earlier version of the process steps to see if the current positive resist was a possible cause of trouble or

if the old method of using solvent strip would provide any insight. The result had only wafer #5 with no peeling; even the control wafer saw some peeling.

These results lead to the interpretation that there is chemical residue remaining on IGZO surface related to positive resist processing. All wet-chemistry strip processes failed – these included acetone followed by IPA, NMP and the solvent strip – in all cases, followed by the Futurrex negative resist process which included HMDS vapor prime. Also, the ash alone did not solve the problem –this may be because the surface turns hydrophilic adsorbing water and causing the metal adhesion failure. The ash followed by Futurrex lift-off resist process, however, saw zero peeling which is believed to be a result of the HMDS following the ash rendering the surface moisture-adverse. Therefore, the inclusion of oxygen plasma prior to lift-off resist should improve metal adhesion and potentially improve the IGZO back-channel by removing surface contaminants.

This hypothesis is supported by a study recently reported which investigated the origin of instability in oxide TFTs [16]. The origin of device instability was found to be CO-related impurities, with results of their investigation represented in Fig. 3.3. The thermal desorption spectra shows the presence of CO and CO_2 after a photolithographic process after resist removal. The results indicated that the CO-related impurities were not physisorbed species because the desorption temperature was high (~350 °C). Thus, the CO-related impurities were formed as a result of the chemical reaction between the oxide surface and alkali photoresist. XPS analysis (specifically hard x-ray photoemission spectroscopy, or HAXPES) identified CO-related species following photolithography patterning that was not present prior to photolithography. The C1s peak is shown in figures labeled c (before) and d (after), with shifted peaks indicating the presence of both C-O and C=O bonds. The change in the O1s peak also indicated the presence of a CO-

related species. It was also confirmed that the chemical reaction is not limited to a specific PR; PRs of different companies yielded the same results. It is therefore necessary to ensure the removal of any organic contaminants that may exist on the IGZO following the mesa pattern and etch processes. Note that the metal adhesion result suggests there is no indication that Futurrex lift-off resist chemically reacts with the IGZO.

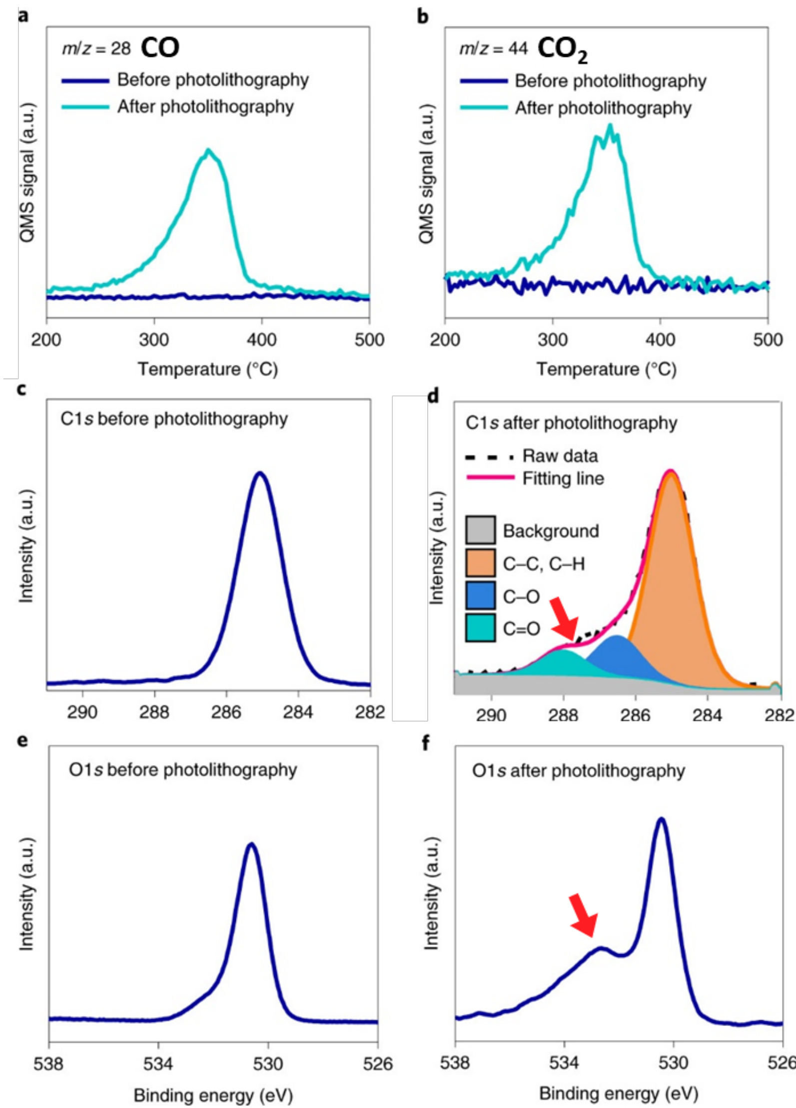


Fig. 3.3. CO-related impurities introduced by photolithography Thermal desorption spectra of (a) mass number 28 for CO and (b) mass number 44 for CO_2. Surface HAXPES data of ITZO thin films for C1*s* peaks (c) before and (d) after photolithography. O1*s* peaks (e) before and (f) after photolithography. Note: QMS and m/z denote quadrupole mass spectrometry and mass to charge ratio, respectively. After [16].

A Trion Apollo resist stripper with ICP source was investigated to remove these chemically reacted organic contaminants. The etching occurs downstream of the plasma source and is designed to reduce the damage caused by the plasma. The system provides a high removal rate and uniform strip, and is claimed to be gentle on sensitive devices. Studies have shown that the downstream configuration subjects the devices to reduced charge levels and associated degradation in comparison to a plasma immersion (conventional O_2 plasma RIE) system [17].

Table 3.2. O_2 Plasma System Recipe Settings

Item	**Hard Ash**	**RIE**
Machine	Trion Apollo Asher	Trion Phantom RIE
Chuck Temperature	200°C	Room temperature
Pressure	1 Torr	200 mTorr
ICP RF Power	900 W	NA
Electrode RF Power	0 W	100 W
Gas Flows	N_2 = 10 sccm O_2 = 300 sccm	O_2 = 20 sccm
Time	180 seconds	60 or 90 seconds

Verification of this hypothesis then followed in the form of an oxygen plasma extension to the peeling experiment on a blanket layer of IGZO, with details listed in Table 3.2. The oxygen plasma treatment experiment consisted of one wafer that went through the hard-ash recipe for 180 seconds, and two wafers that went through the RIE for 60 and 90 seconds. The RIE process was investigated for comparison as an alternative process that may offer an advantage in process integration while still avoiding device degradation. The power and time for the RIE treatment were reduced to reduce the possibility of device degradation due to direct plasma exposure. The hard-ash treatment was a replicate of the peeling investigation described previously, and resulted in no metal peeling. On the other wafers, the 60 seconds RIE treatment was found to be too short, whereas 90 seconds was found to be long enough to prevent metal peeling. Another important adjustment made here was to ensure that the HMDS was applied as soon as the wafers left the

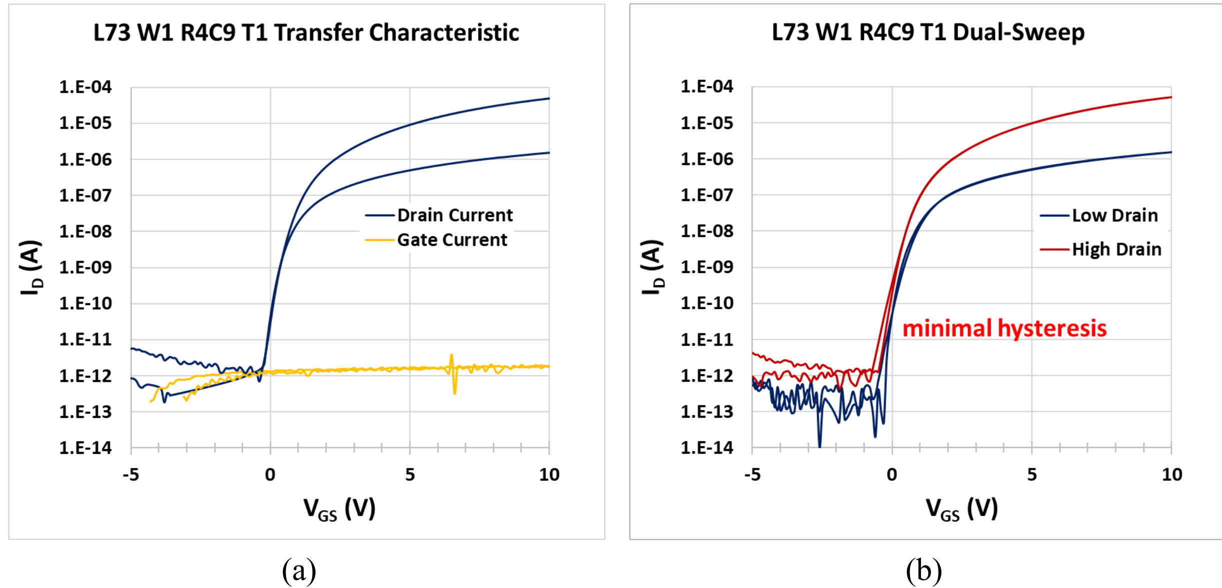
plasma, thus to seal in the benefits of the plasma, i.e. avoid water adsorption. In addition, the wafers were put into the metal sputter machine vacuum system within an hour of this process.

3.3. TFT Fabrication and Electrical Results

The purpose of Lot 73 was to confirm that the results of the blanket verification translated to device wafers. Treatments included a 180 second hard-ash (W5), and the conventional RIE process for 90 seconds (W1 & W2) and 180 seconds (W3 & W4). The hard-ash treatment saw no peeling, however the RIE treatments both exhibited metal peeling in the peripheral regions. While this is a concern, there appeared to be no issues in the metallized device regions. The RIE treatment produced functional devices, whereas the hard-ash treatment yielded short circuits indicating gate dielectric failure; the exact reason for this result was unknown but thought to be related to electrical stress induced by the hard-ash process. The following discussion is focused on the 90sec O_2 RIE treatment (W1), as that produced the best electrical characteristics. There was significant variation within the sample, thus characteristics have been selected to represent best-case device operation shown in Fig. 3.4, as well as non-ideal behavior shown in Fig. 3.5 and Fig. 3.6. Note that the drain bias was limited to V_{DS} = 5 V due to pronounced leakage and dielectric failure observed at the usual V_{DS} = 10 V application.

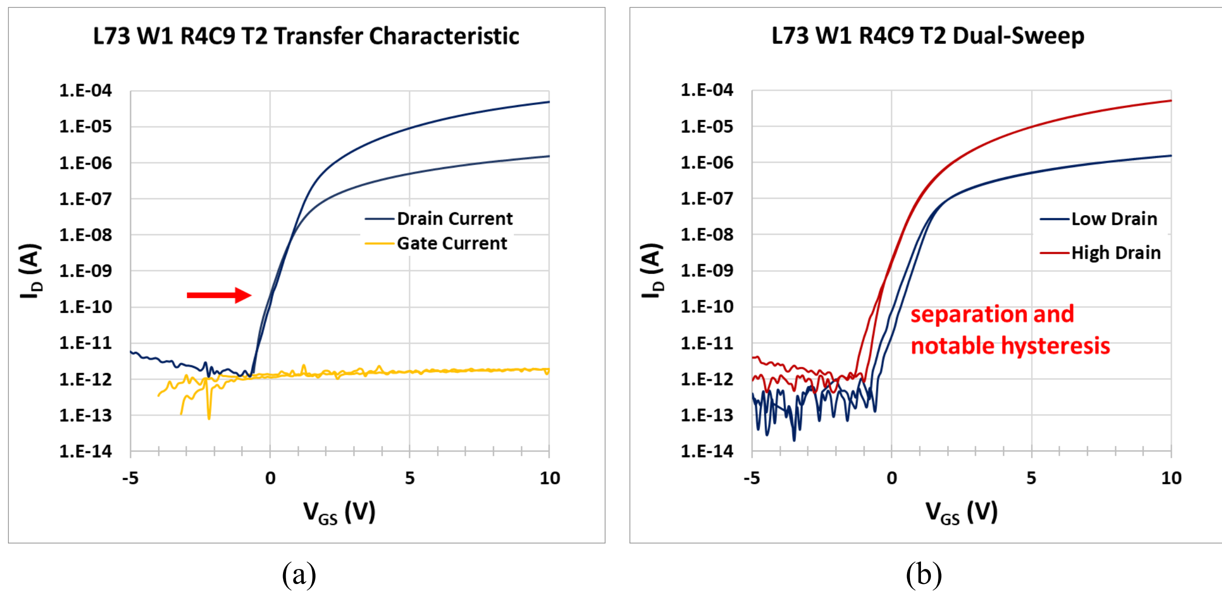
The “T1” device shown in Fig. 3.4 has a SS = 178mV/dec, low gate leakage, and is positioned to have enhancement-mode operation (i.e. positive V_T). There were several similar characteristics, however most were not as steep, and exhibited some separation and/or hysteresis. The dual-sweep characteristic in Fig. 3.4(b) does shows that hysteresis is low but present. This indicates interface trap states are operative and that some state changes are not keeping up with the gate voltage sweep rate used, which was approximately 0.5V/s. The characteristics in Fig. 3.5 are measured on a “T2” device to the immediate right of the “T1” device. Note the cross-over of

characteristics indicated by the arrow, which is a clear influence of trap states. The dual-sweep test demonstrates significant separation and notable hysteresis which is further evidence of trap-state effects.



(a) (b)

Fig. 3.4. Best-case IGZO TFT ID-V_{GS} transfer characteristics measured on Lot#73 W1 R4C9 T1, with L = 12 µm and W = 24 µm. The low and high drain bias conditions are V_{DS} = 0.1 V and 5V, respectively. Gate current measurements are also provided as an indication of gate dielectric integrity. (a) single-sweep V_{GS} from -5 V to 10 V. (b) dual-sweep (up/down) measurement demonstrating minimal hysteresis.



(a) (b)

Fig. 3.5. Transfer characteristics measured on Lot#73 W1 R4C9 T2. (a) single-sweep V_{GS} from -5 V to 10 V, showing slight cross-over in the low and high drain bias characteristics. (b) dual-sweep (up/down) measurement demonstrating separation and hysteresis.

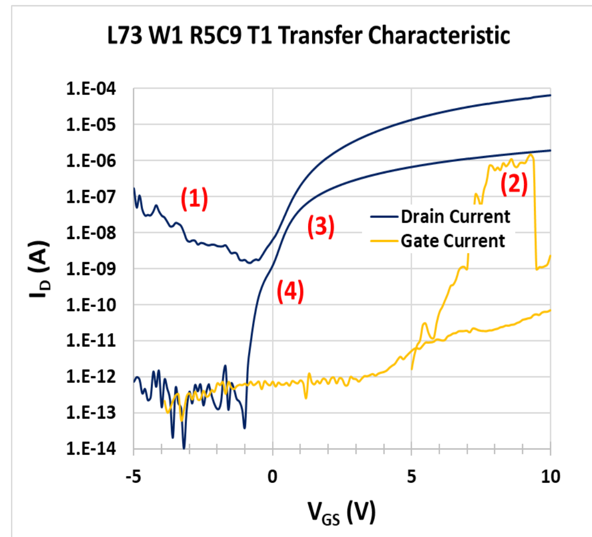


Fig. 3.6. Transfer characteristics measured on Lot#73 W1 R5C9 T1. The numbered labels identify non-ideal device behavior referred to in the associated narrative.

As a final representation of the O_2 RIE treatment, several non-ideal device behaviors were observed in the inferior transfer characteristic shown in Fig. 3.6, as identified by the numbered labels. Item #1 is pronounced gate dielectric leakage between the gate and drain electrodes at the high drain bias in the off state. This measures as a negative gate current; electrons flow from the gate to the drain which appears as a component of positive drain current on the log-scale plot. In this region, the drain current is equal in magnitude to the gate leakage. Item #2 shows the direct measurement of gate dielectric leakage as the gate voltage exceeds the drain voltage at $V_{GS} \geq 5$ V and the gate leakage current becomes positive (electrons flow from drain to gate). Item #3 shows the DIBL-like separation, previously referred to as TABL or trap associated barrier lowering, which is related to inadequate passivation of back-channel defects. Item #4 identifies a kink in the subthreshold region indicating involvement of a discrete energy trap state. Considering the point at which the gate voltage goes below 0 V, there is a distinct left-shift in the characteristic which can be interpreted as the ionization of donor-like interface traps which lose their electron and

become positively charged. This voltage offset (ΔV) corresponds to the interface density (N_{IT}) using equation (1):

$$\Delta V = \frac{qN_{it}}{C_{ox}} \tag{1}$$

where C_{ox} is the oxide capacitance per area. Using a gate oxide thickness of 50 nm, the measured offset ΔV = 0.33 V corresponds to an effective $N_{it} = 1.4\text{x}10^{11}\text{cm}^{-2}$.

The results of Lot#73 were not as hoped regarding both metal peeling and device operation. The RIE treatment samples had a low dielectric breakdown strength which limited the drain bias to 5 V for device testing. Gate leakage was still pronounced on several devices. While the select best-case results demonstrated good performance, many devices showed the influence of interface traps (i.e. poor passivation). There were still metal adhesion issues in the periphery which were not observed on the hard-ash treatment sample, however devices demonstrated dead shorts for reasons unknown. This was further investigated in the Lot#74 experiment. All samples received a hard-ash treatment following the mesa pattern and etch processes. An experimental split involved an additional O_2 plasma treatment following the source/drain metal liftoff process, immediately prior to the passivation oxide deposition. However, results indicated no difference in electrical behavior. There was no observed metal peeling on these samples, however there was significant compromise in the device operation which was more pronounced than on Lot#73.

The device shown in Fig. 3.7 is the best-case characteristics found, with a good overlay and SS ~ 500 mV/dec. There were several similar characteristics, however many were shallower and had significant separation (TABL). As in Lot#73, the drain bias was limited to 5V to avoid gate dielectric failure, which was pronounced at the usual V_{DS} = 10V measurement. In addition, the gate leakage was more elevated in this lot in comparison to Lot#73. The elevated value of SS

corresponds to fast surface states, or interface traps. The dual-sweep measurement on the right shows that hysteresis is minimal, meaning that the trap states are keeping up with the applied sweep rate. The interface trap density distribution can be estimated using following equation for a bulk semiconductor device [18]:

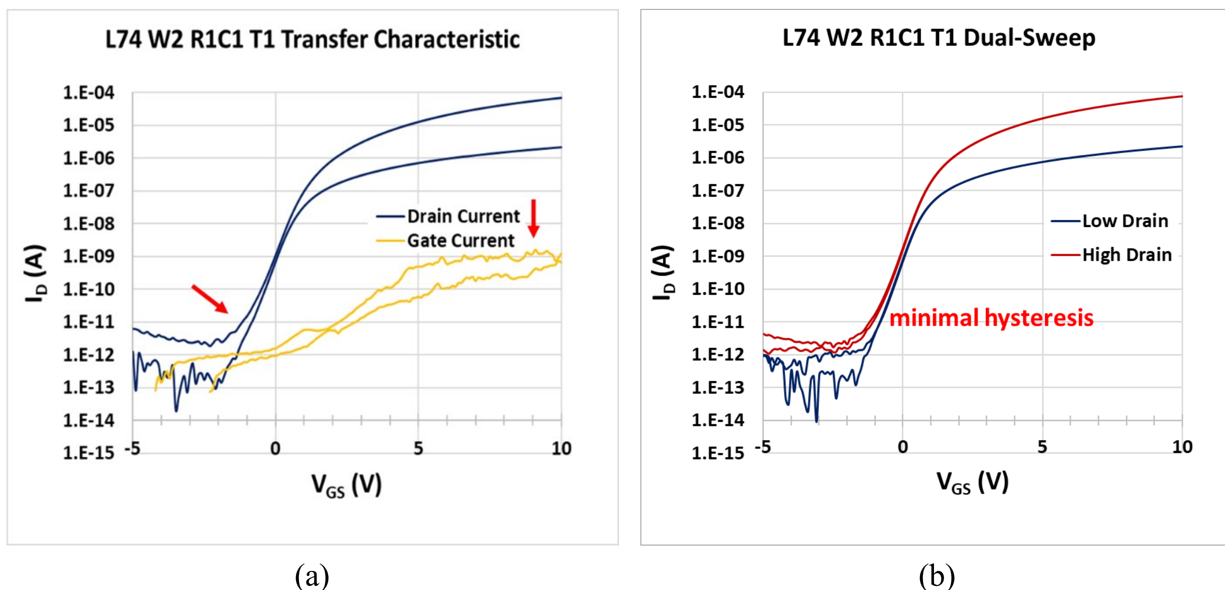
$$SS = \left(\frac{2.3kT}{q}\right)\left[1 + \frac{C_d + qD_{it}}{C_{ox}}\right] \tag{2}$$

where C_d is the capacitance of the depleted semiconductor, C_{ox} is the gate oxide capacitance, qD_{it} is the interface state capacitance and D_{it} (cm^{-2}/eV) represents the interface trap density. Note that this equation is for bulk semiconductors, with the case of a fully depleted semiconductor layer being more complex. However, it can be used for a first-order approximation with some assumptions. If the zero-trap SS value is taken to be 140 mV/dec, then the effective depletion capacitance is calculated as $C_d = 9.3\text{x}10^{-8}$ F/cm^2. This corresponds to an effective IGZO thickness of 96 nm, which is ~ 2x the actual thickness; however, when the IGZO film is electron depleted, its capacitance nearly vanishes.

The following results from the measured SS = 500 mV/dec:

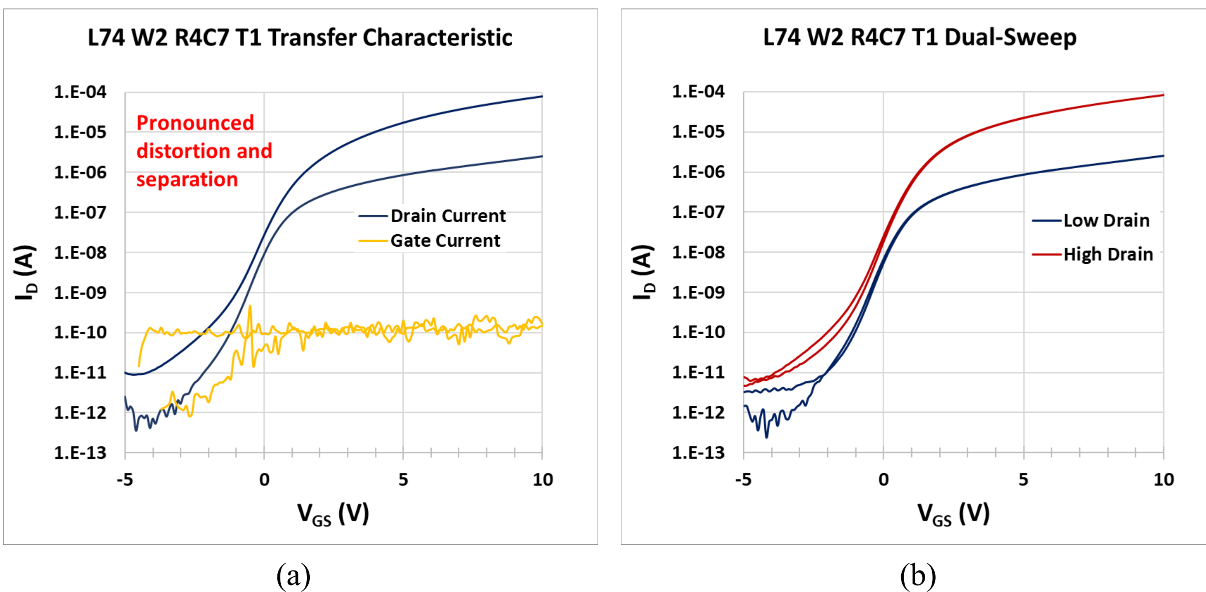
$$0.5\, V/dec = \left(\frac{2.3kT}{q}\right)\left[1 + \frac{9.3 \times 10^{-8}\, {}^{F}/_{cm^2} + qD_{it}}{6.9 \times 10^{-8}\, {}^{F}/_{cm^2}}\right]$$

resulting in $D_{it} = 2.6\text{x}10^{12}$ cm^{-2}/eV. Note that this is almost an order of magnitude higher than the same D_{it} approximation for the Lot#73 best-case result, considering that the SS = 178 mV/dec was significantly lower.



(a) (b)

Fig. 3.7. Best-case IGZO TFT ID-V_{GS} transfer characteristics measured on Lot#74 W2 R1C1 T1, with L = 12 µm and W = 24 µm. The low and high drain bias conditions are V_{DS} = 0.1 V and 5V, respectively. Gate current measurements are also provided which indicate compromised dielectric integrity. (a) single-sweep V_{GS} from -5 V to 10 V. (b) dual-sweep (up/down) measurement with sweep rate ~ 0.5 V/s, demonstrating minimal hysteresis.



(a) (b)

Fig. 3.8. Transfer characteristics measured on Lot#74 W2 R4C7 T1. (a) single-sweep V_{GS} from -5 V to 10 V, showing slight cross-over in the low and high drain bias characteristics. (b) dual-sweep (up/down) measurement demonstrating separation and hysteresis.

The spreading in the off-state of the V_{DS} = 5V characteristic indicates the role of back-channel donor-like traps thus requiring additional negative gate voltage to fully deplete the IGZO semiconductor layer. Figure 3.8 shows a final representative device with the initial characteristics showing separation and pronounced distortion. The background gate dielectric leakage (~ 100pA) is well above the noise floor (~ 1pA) achieved by best-case devices on Lot#73. Hysteresis on this device is relatively low.

3.4. Summary of Device Operation

The hard-ash and RIE treatments both resulted in degraded device performance, however the associated characteristics were distinct. The best-case characteristics from the O_2 RIE treated sample in Lot#73 shown in Fig. 3.4 demonstrate a minimal influence of interface traps, however the typical device operation is compromised. The cross-over of transfer characteristics and the observed TABL and hysteresis observed in Fig. 3.5 on O_2 RIE treated devices demonstrates the influence of trap states. These states were presumably either created at the gate-oxide / IGZO interface during the O_2 RIE process, or back-channel states at the IGZO / passivation-oxide interface resulting from damage induced on the exposed IGZO surface that were not successfully passivated during the 400°C O_2 anneal process. The device shown in Fig. 3.6 exhibited a pronounced kink in the transfer characteristics at a gate voltage V_{GS} ~ 0 V, indicating the presence of a discrete trap state with an energy level consistent with the associated surface potential (i.e. Fermi energy, E_F). The negative voltage shift related to this donor-like trap corresponds to an effective interface trap density $N_{it} = 1.4\text{x}10^{11}$ cm^{-2}.

The hard-ash treated samples from Lot#74 shown in figures 3.7 and 3.8 exhibit much more spreading and distortion, also due to unpassivated trap states but with a broadened energy distribution. The fact that Lot#74 experienced more issues with gate leakage and dielectric failure

indicates that compromised device operation was as least in part due to degradation on the gate side of (below) the IGZO. The high subthreshold swing SS ~ 500 mV/dec corresponds to an estimated $D_{it} \sim 2.6\text{x}10^{12}$ cm^{-2}/eV in the subthreshold region, which compares to $D_{it} \sim 2.7\text{x}10^{11}$ cm^{-2}/eV for the best-case O_2 RIE device from Lot#73 which had a steep subthreshold SS = 178 mV/dec. Note that the best-case result is consistent with the calculated $D_{it} = 2.53\text{x}10^{11}$ cm^{-2}/eV arrived at by taking E_F at the intrinsic level using $E_i = E_C - 0.37$ eV along with the peak and exponential decay parameters associated with back-channel interface trap states defined in table 1.2.

CHAPTER 4. CONCLUSIONS & FUTURE WORK

4.1. Summary and Conclusions

The original proposed studies involved investigations on process options that promote enhanced passivation of defect states, and resistance to hydrogen plasma exposure. However during the beginning stages of experimentation the problems identified took precedence and required a redirection of process development efforts.

Both the ICP hard-ash and O_2 RIE treatments were successful in promoting metal adhesion on blanket wafers following the relevant photolithographic processes, though only the hard-ash treatment was successful at preventing peripheral peeling on device wafers. An immediate application of HMDS treatment followed by a short space of time before metal deposition was necessary to avoid water adsorption. Both plasma treatments were observed to compromise the IGZO TFT operation. Reduced gate dielectric integrity resulted in lower breakdown strength and higher leakage. The influence of trap states was clearly seen in device characteristics, indicating inferior passivation following oxide deposition and annealing processes. Thus neither process appears to offer a promising solution for the back-channel contaminant issue.

4.2. Future Work

Future work will need continued investigation on removal of back-channel organic contaminants. For this there are several possible avenues of interest. One might be to use a barrel asher which may reduce plasma-induced damage to the IGZO surface and gate dielectric. Another would be looking at alternatives for chemical stripping, for instance possibly revisiting PRS2000 which had been used previously on devices that exhibited good characteristics as seen in the introduction. Based on the thermal desorption spectra obtained by Shiah *et al* (see Fig. 3.3),

thermal desorption in an oxygen chamber where O_2 can flow in a PECVD chamber stabilized at 400°C would also be a viable option. Upon resolution of this issue the original study focus areas outlined in chapter 2 could be revisited; specifically the nitrous oxide plasma treatment for reduced back-channel defects and reactivity, and the ozone ALD alumina capping for improved resistance to hydrogen plasma.

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