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A Comprehensive Study of Gain Characterization in MOSFETs

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A Comprehensive Study of Gain Characterization in MOSFETs

by

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Dedication

I would like to dedicate this work to my mother Sue Ellen McCall, my step-father Scott McCall, my father Anthony Greenfield III, my step-mother Heather Greenfield, and my advisor Mark Indovina for their unwavering support and kindness during my academic journey.

Elaine Greenfield

Declaration

I hereby declare that except where specific reference is made to the work of others, that all content of this Graduate Paper are original and have not been submitted in whole or in part for consideration for any other degree or qualification in this, or any other University. This Graduate Project is the result of my own work and includes nothing which is the outcome of work done in collaboration, except where specifically indicated in the text.

Elaine Greenfield

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Elaine Greenfield

Abstract

The functionality of MOSFETs makes them a crucial component in modern electrical engineering. These devices play a fundamental role in a wide range of applications. Understanding the behavior and characteristics of MOSFETs is essential for their effective utilization in circuit design. One crucial parameter that significantly impacts MOSFET performance is voltage gain. It represents the ratio of output voltage to input voltage and varies depending on the circuit configuration employed. When selecting a MOSFET for a specific circuit, understanding the parameters and characteristics that influence voltage gain becomes crucial. This research project aims to delve into the realm of MOSFETs, investigating, simulating, and testing various parameters that influence their performance. The study will encompass a broad spectrum of factors.

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Chapter 1

Introduction

The functionality of MOSFETs makes them a crucial component in modern electrical engineering. These devices play a fundamental role in a wide range of applications. Understanding the behavior and characteristics of MOSFETs is essential for their effective utilization in circuit design.

One crucial parameter that significantly impacts MOSFET performance is voltage gain. It represents the ratio of output voltage to input voltage and varies depending on the circuit configuration employed. When selecting a MOSFET for a specific circuit, understanding the parameters and characteristics that influence voltage gain becomes crucial.

Gain primarily has an effect in amplifier circuits. In circuits where amplification is the primary goal, accurate control of gain is crucial for proper operation. Functional examples where gain is a critical component would be audio amplifiers.

This research project aims to delve into the realm of MOSFETs, investigating, simulating, and testing various parameters that influence their performance in regard to gain. The study will encompass a broad spectrum of factors.

1.1 Research Goals

The primary intent of this research is to understand the parameterization of MOSFETs to generate high gain. This research aims to contribute valuable insights and methodologies to enhance performance in scenarios requiring high gain in analog designs. This research is Shown below is a summary of the leading research goals:

- To understand the impact of a variety of parameters on MOSFET gain.
- To formulate the most optimal transistor for maximum gain.
- Provide insights for analog circuit design where high gain is required.

1.2 Contribution

1. 1 V Supply NMOS and PMOS parameterization
2. Systematic variation methods.
3. Gain optimization methods.

1.3 Organization

The structure of the thesis is as follows:

- Chapter 2: This chapter discusses the background information referencing journals and articles. This chapter also discusses previously completed research and information on MOSFET parameter effects.
- Chapter 3: This chapter explains the selected research parameters and their significance.

- Chapter 4: The chapter details the design process for the testbench created for analyzing the selected MOSFETs.
- Chapter 5: This chapter goes over the initial benchmarking for gain result comparisons.
- Chapter 6: This chapter discusses about the obtained results in detail and the drawn observations from the recorded results.
- Chapter 7: This chapter outlines the conclusion of the study and possible ways of extending it.

Chapter 2

Bibliographical Research

2.1 A Brief Overview of MOSFETs

The MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) stands as a monumental cornerstone within modern technology, emerging as one of the most prolific and influential electronic devices in history. There are billions of MOSFETs existing within every piece of modern electronic technology. Its distinctive architecture features a gate, drain, and source, as seen in Figure 2.1. There are two different types of MOSFETs, PMOS and NMOS. NMOS devices are n-type, which means the channel is created with the flow of electrons. Whereas with PMOS devices, the channel is created with the flow of holes. Electrons and holes are oppositely charged, therefore they flow in opposing directions. In their most basic form, MOSFETs effectively perform as switches. When a sufficient voltage is applied to the gate, an electric field is generated that changes the width of the channel region, allowing for more current to flow. This is the "on" state of the MOSFET.

There are multiple uses for MOSFETs. As individual devices, they serve multiple purposes; such an example is of a switch as mentioned above. The MOSFET seen in Figure 2.1 is

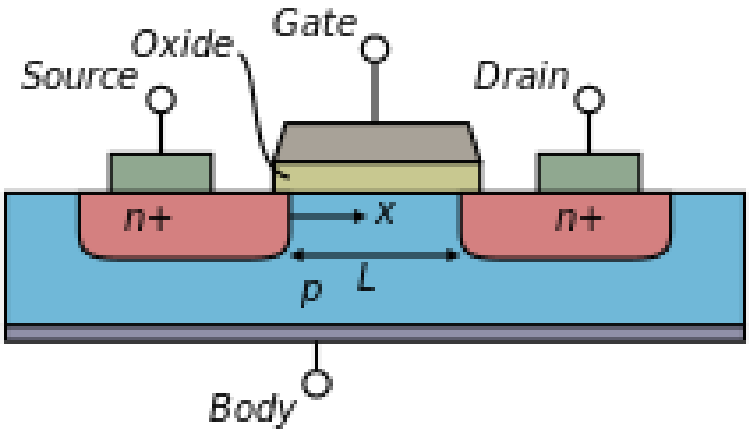

Figure 2.1: MOSFET Structure [1]

the most basic structure of a MOSFET. However, there are several variations of this design for specialized purposes, such as multigate devices, lightly-doped drain-source devices (LDDs), and silicon on insulator (SOI) MOSFETs, to name a few. These devices are described in more detail in the following sections of this chapter.

2.1.1 Multigate Devices

The swift progress in semiconductor technology has been a driving force behind the downsizing of electronic devices, leading to heightened device density and performance. Nonetheless, scaling down conventional planar MOSFETs has become progressively difficult due to challenges related to short channel effects and power dissipation. To address these hurdles, alternative device structures with multiple gates have been proposed, offering a number of beneficial properties, including enhanced electrostatic control and reduced leakage currents.

These multi-gate devices are characterized by the presence of several gates encircling the conducting channel, contributing to better electrostatic control and alleviation of short channel effects. Essentially, the operational principle of multi-gate devices mirrors that of planar

devices, where the device is activated when the gate voltage surpasses the threshold voltage. Diverse topologies for multi-gate devices exist, as illustrated in Figure 2.2.

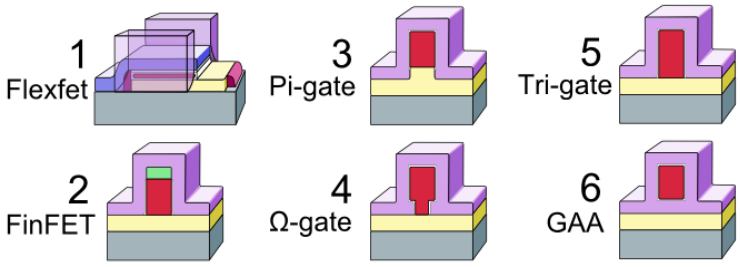

Figure 2.2: Various Multi-Gate Device Topologies [2]

One such structure, the FinFET, entails a slender silicon fin serving as the conducting channel. The fin is enveloped by a gate dielectric and a gate electrode, enabling superior electrostatic control compared to planar MOSFETs.

Another type, the tri-gate transistor, encompasses three gates strategically positioned on the sides of a vertical fin. This arrangement facilitates better regulation of electrical current flow through the transistor, leading to heightened efficiency and improved electrostatic control.

Furthermore, there are gate-all-around FETs, characterized by a gate electrode that entirely surrounds the channel, resulting in superior electrostatic control. These FETs can manifest with either nanowire or nanosheet channels.

2.1.2 LDD MOSFETs

Lightly doped source-drain MOSFETs primary difference from a traditional MOSFET is the inclusion of n^-regions inserted between the channel and the source-drain n^+ diffusion regions [8]. The structure of the LDD MOSFET can be seen in Figure 2.3. The primary advantages of an LDD device are an ability to increase power supply voltage, and decrease the channel length. These abilities are because the structure of the LDD device allows for an increased

breakdown voltage and reduced impact ionization, which creates a strong electric field.

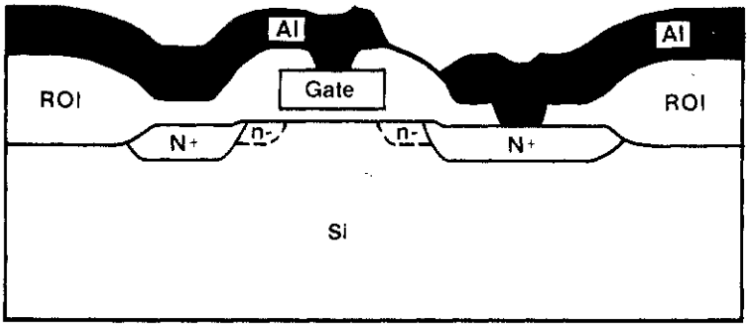

Figure 2.3: LDD MOSFET Structure [3]

2.1.3 SOI MOSFETs

Silicon on insulator (SOI) MOSFETs have an additional layer of silicon and SiO_2on the insulator. This differs from the conventional MOSFET, which is just a layer of bulk silicon. The structure of an SOI MOSFET can be seen in Figure 2.4. The main advantages of the SOI MOSFET are low capacitances, which leads to high speed performance. These devices also have zero body-effect [9].

2.2 Gain in MOSFETs

Gain is a quantity that represents the ability to amplify an input signal to have a different amplitude at the output [10]. In MOSFETs, gain is represented as the ratio of output voltage to input voltage. The measurement for gain is typically in the units of decibels. Primarily, gain is taken to be a function of transconductance, load resistance, and drain resistance. This is a crucial parameter in circuit design, as it directly impacts the performance of devices.

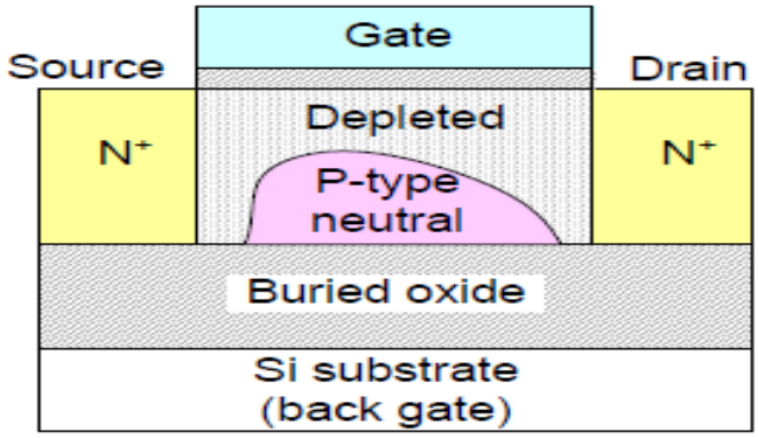

Figure 2.4: SOI MOSFET Structure [4]

2.3 Previous Studies on MOSFET Gain

Many circuits are optimized for high gain, as this is a critical specification in things like amplifiers. However, little documentation is present on the parametric effects on gain. Likely, this is because MOSFETs are not considered in comparison to bipolar junction transistors (BJTs) for high gain applications [11]. The gain of the MOSFET is a function of the transconductance, which varies with the bias point [12]. The studies discussed below provide the closest relevant documentation to gain analysis.

2.3.1 Gain Design Research

The primary approach for gain optimization in amplifier circuits is the increase of the output resistance of the system, or the device. This is typically either done through cascoding, or adding additional resistors on the load [13–15]. There is a well known relationship between gain and frequency, and research has been conducted on the optimization of that relationship [16]. Substantial research has also been conducted on the use of double gate, or multi gate

transistors and their relationship with gain. This research also brings relevant information to gate area and gain relationships [17].

2.4 Applications of MOSFET Gain Analysis

Gain plays a crucial role in numerous practical applications. Gain is a prominent specification for a well-known, and universally used circuit, the operational amplifier.

2.4.1 Practical Applications of MOSFET Gain

Gain is necessary specification for a breadth of applications. Automatic gain control systems are a frequently used example for where gain is a critical specification [18]. The most obvious example of this is for the use of audio amplifiers [19]. Additionally, biomedical applications frequently need high gain for accurate measurements. High gain is a necessary specification for blood pressure monitoring and echocardiograms to name a few [20].

2.5 Conclusions

Accurate measurements and understanding of gain is critical. Gain is a keystone specification in medical, military, and civilian equipment. Having a thorough understanding of how all parameters impact gain will be beneficial for future circuit design.

Chapter 3

MOSFET Parameters and Devices of Interest

3.1 Parameters of Interest

The gain of a MOSFET is influenced by several parameters. These parameters will be varied individually and systematically. A foundational transistor model will be established with base values assigned to all parameters to ensure consistency in testing procedures. Furthermore, we will conduct analysis on various devices from the library. These parameters and devices will be discussed in further detail in the remainder of this chapter.

3.1.1 Transistor Area

As mentioned in Chapter 2, the gain of a MOSFET has a known relationship with the output resistance of the device. The area of a transistor has a direct impact on device resistance. Therefore, it is likely that transistor area will have a significant impact on the gain.

3.1.1.1 Transistor Length

The length of the transistor is the distance between source and the drain. This region is also known as the channel. The length of a standard MOSFET is depicted in Figure 3.1.

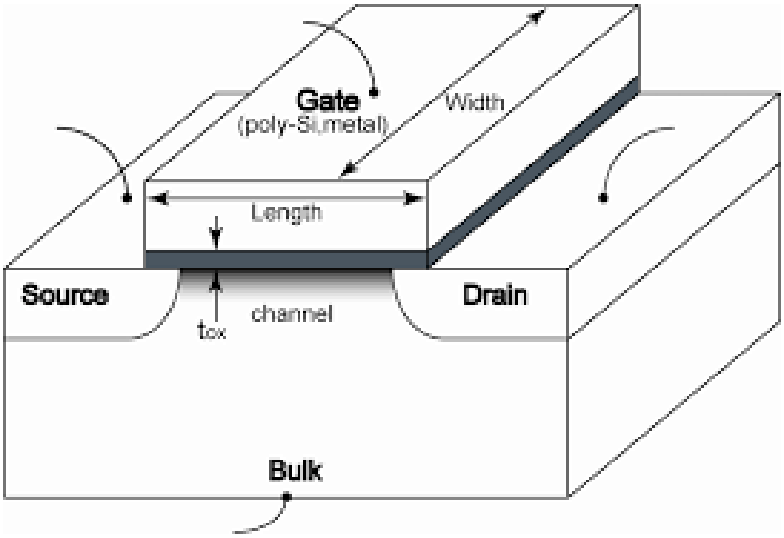

Figure 3.1: MOSFET Length and Width Depiction [5]

3.1.1.2 Transistor Width

The width of a typical transistor is also depicted in Figure 3.1. This is the total width of the gate, which stretches in a perpendicular axis to the length. Typically, this is the value that is varied when designing transistors for specific inversion levels.

3.1.2 Temperature

It is well known that as temperature goes up, the effective resistance of the device also goes up. This is because higher temperature excites electrons, causing more collisions and a lower mobility [21].

3.1.3 On-State Resistance

The on-state resistance represents the effective resistance between the drain and the source of a MOSFET when the device is on. This value varies with the gate-source voltage [22]. Ideally, when the transistor is off, the value of this resistance would be infinite. This value has a direct correlation to output resistance, thus will likely have an impact on gain.

3.1.4 Source and Drain Resistances

The source and drain resistances are exactly as they sound–the resistance value at the source and drain individually. The total value between the two is referred to as R_{DS}. Source and drain parasitic resistances have been shown to decrease the transconductance of a MOSFET [23]. Thus, it is likely these values will have a significant impact on the gain of a MOSFET.

3.1.5 Mobility

Mobility is a relationship between drift velocity and an applied electric field [21]. This quantity can be represented for either holes or electrons. Mobility has relationships with a few crucial parameters; mobility is strongly impacted by temperature, and by the associative property, as is resistance, additionally, mobility is a parameter in the function for the transconductance parameter.

3.1.5.1 Transconductance Parameter

The transconductance parameter is a function of mobility and oxide capacitance. The transconductance parameter is represented by the letter K. Along with width, length, and operational voltages, this parameter can be used in a function for the transconductance. Thus, as implied by the name, this parameter would be greatly influential in gain results.

3.1.6 Threshold Voltage

The threshold voltage is the value at which a MOSFET transitions into strong inversion [24]. This value directly relates to the drain current and gate-source voltage. It is likely that the threshold voltage will have an impact on the gain of a MOSFET.

3.1.6.1 Zero-Bias Threshold Voltage

The zero-bias threshold voltage is the threshold voltage, when there is no voltage present across the drain and source [25]. It is unknown whether this quantity will impact the gain of a MOSFET.

3.1.7 Oxide Thickness

The oxide thickness is a relationship between the oxide capacitance and the device permittivity. The higher the permittivity, the more charge can be stored in an electric field. A thicker oxide would correspond to a lower permittivity, and thus would likely correlate to a smaller gain.

3.1.8 Capacitance

Capacitance is the ability to store charge in a component. This exists between two metal layers. Since MOSFETs are built consisting of layers of metals and insulators, capacitance is inherently formed. The main parasitic capacitances that are formed are the gate, drain, and source capacitances. These are depicted for both a NMOS and PMOS device in 3.2. These values are unlikely to have an impact on gain, as they primarily impact device qualities such as speed.

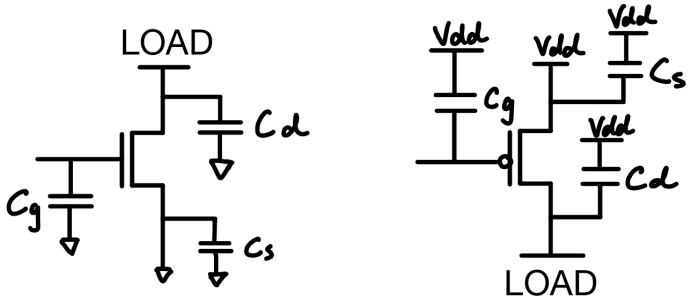

Figure 3.2: MOSFET Capacitance Diagram

3.1.8.1 Oxide Capacitance

The oxide capacitance is the capacitance value between the gate and the substrate of a MOSFET, as illustrated in 3.3. This value has significant effects on the mobility of a device, and thus is likely to impact the gain. This value is also directly related to the oxide thickness.

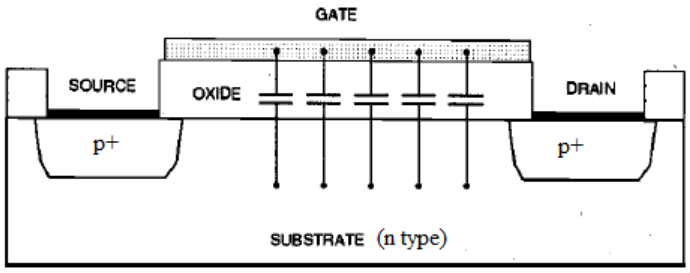

Figure 3.3: Oxide Capacitance Illustration [6]

3.1.9 Gate Charge

The gate charge, Q_G is the amount of charge needed to turn on a MOSFET. This quantity has a direct relationship with the on-state resistance [26]. Additionally, this quantity relates to the power and switching capabilities of a MOSFET. It is likely that this quantity will impact gain,

Table 3.1: Selected Devices within the Library

Device	Description
nmos1v	1 V Supply NMOS
pmos1v	1 V Supply PMOS

even if it is minimally.

3.1.10 Channel Length Modulation

Channel length modulation, λ, is a parameter that quantifies the effects of changes within the drain-to-source voltage [27]. This quantity is directly related to the output resistance, and thus will likely have a strong effect on the gain.

3.2 Devices of Interest

The devices of interest in the process design kit (PDK) used can be seen below in Table 3.1. This allows comparisons and contrasts of PMOS and NMOS devices.

Chapter 4

Transistor Configuration and Design Methodology Selection

Testing a single transistor at a time is the most accurate way to eliminate variables. This allows for control over all parameters in simulation.

4.1 Configuration Selection

When it comes to the simplest design for a gain test circuit, a single transistor design is optimal. There are three options of configuration for a single transistor gain test circuit. These are as follows: common gate, common drain, and common source. In the common gate amplifier, the input is connected to the source and the output is connected to the drain. In the common drain amplifier, the input is connected to the gate and the output is connected to the source. Lastly, in the common-source amplifier, the input is connected to the gate and the output is connected to the drain. A chart comparing the properties of the single-stage amplifiers can be seen below in Table 4.1.

Table 4.1: Summary of Transistor Configuration Details

Parameter	Common Source	Common Gate	Source Follower
Gain magnitude	High (Same value)		< 1
Gain phase	180 degrees (-)	0 degrees (+)	0 degrees (+)
Current gain	Infinite	1	Infinite
Input Impedance	High	Low	High
Output Impedance	High (Same value)		Low
BW	Low	High	Highest

Clearly, the common-drain amplifier, seen in 4.1, also known as the source follower amplifier, is immediately out of the selection process because the gain is near unity for it. The decision process between the common source and common gate amplifiers is more complicated. Both amplifiers have the potential for high gain, which is the desired outcome. The circuit diagram for a common source amplifier can be seen in Figure 4.2, whereas the circuit diagram for a common gate amplifier can be seen in Figure 4.3.

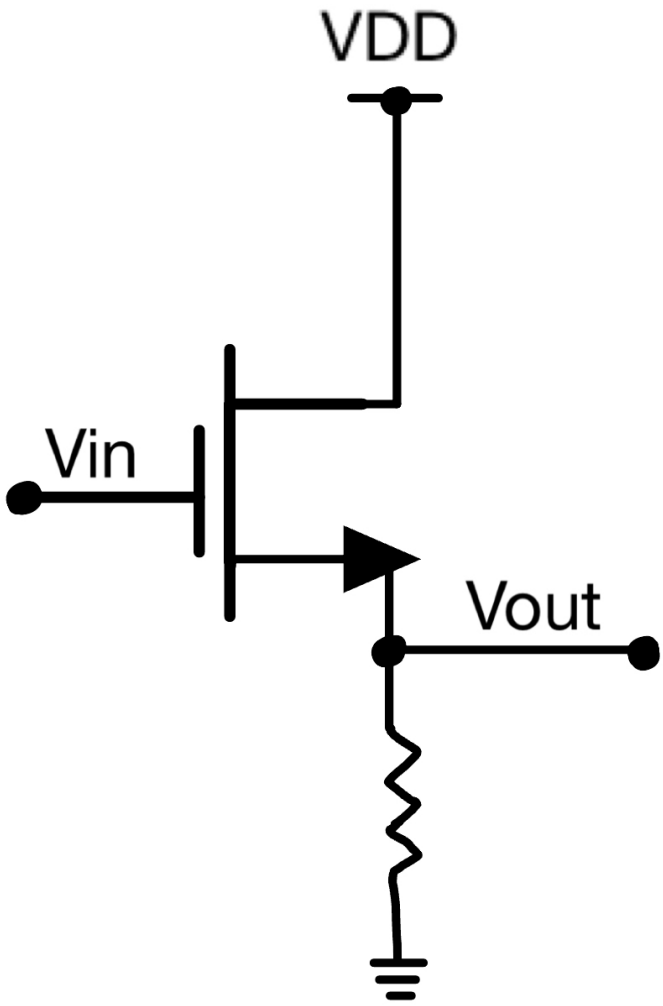

Figure 4.1: Common Drain Configuration

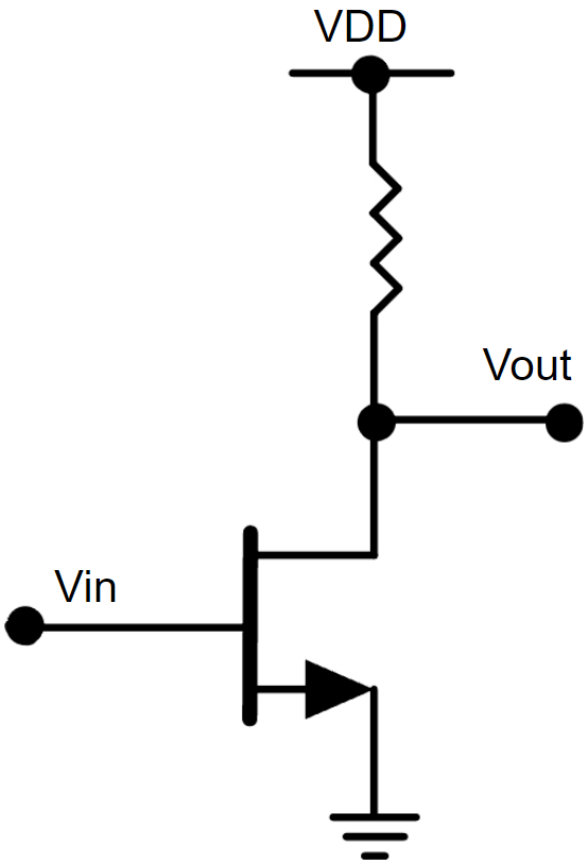

Figure 4.2: Common Source Configuration

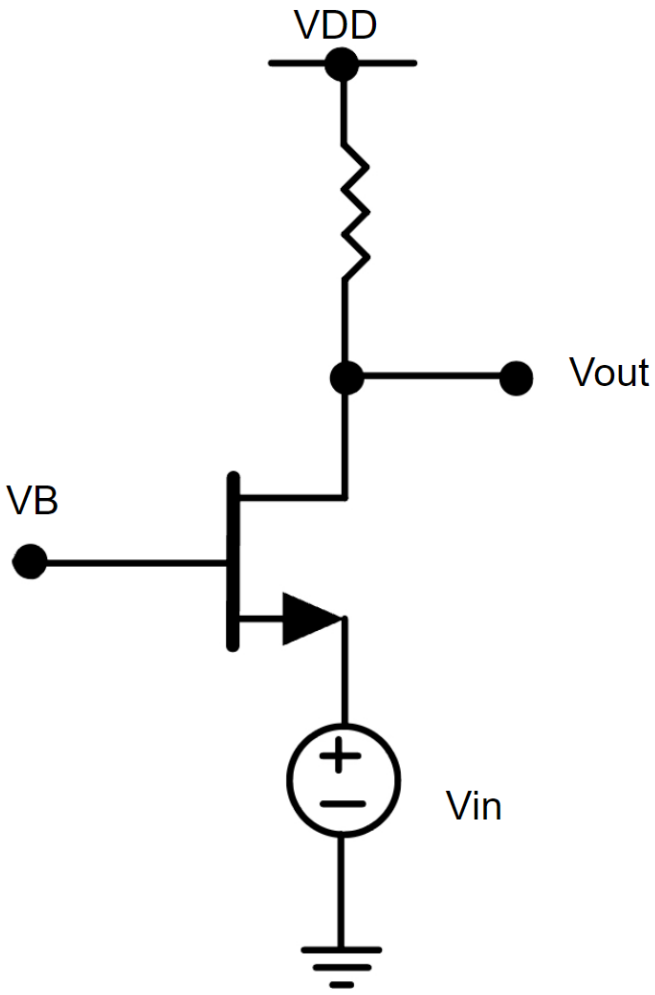

Figure 4.3: Common Gate Configuration

These are the simplest examples of common source and common gate amplifiers. Any additional components added to this would only complicate the test circuit.

4.2 Background on Design Methodologies

The intrinsic characteristics, such as intrinsic gain, are important for understanding and analyzing components. With a established understanding of the intrinsic properties of a device, this allows for enhancement of future research and device parameter quantification. Several different methodologies exist for measurement of these intrinsic values.

It is no secret that semiconductor technology continues to advance into the deep dub-micrometer range. As time goes on, devices continue to become reduced in size. With the reduction of size comes the introduction of short-channel effects. Analog designers face new challenges as devices continue to scale down in size. Many of the initial equations developed for sizing and designing transistors are based on long-channel devices. Additionally, these equations are typically based on transistors being in strong or weak inversion, since moderate inversion equations became overly complicated and difficult to develop.

Thus, since hand-calculations lose validity as devices shrink in size, new and reliable transistor design methodologies had to be developed. Three main methods are mentioned and discussed below. These are threshold voltage models, EKV models, and the gm/ID model. Each of these models utilizes different variables for analysis of transistor parameters.

4.2.1 Threshold Voltage Models

The main parameters of consideration in this model are the threshold voltage V_T, and the overdrive voltage V_{OV}. This method primarily focuses on the use of well-known expressions for the drain current I_D and the transconductance gm in both weak inversion and in strong inversion. This model relies on known, or previously measured, values for drain-source voltage V_{DS}, and early voltage V_A. The known value for the V_{DS} is used to calculated the threshold voltage. Once the threshold voltage is found, this can be compared to the gate-source voltage

V_{GS}. If the threshold voltage is found to be less than the gate-source voltage, it means the device should be in weak inversion. If the threshold voltage is found to be more than the gate-source voltage, it means the device should be in strong inversion. In this model, the ability to select inversion level is not present. From this point, the selected transconductance can be used to extract the necessary drain current. Once the drain current is known, this can be used along with a table of early voltage values to select the sizing of the transistor [28].

4.2.2 EKV Models

This model focuses on the use of the specific current, I_S. In this model, the user has the ability to select the inversion level. This is typically the first parameter that is selected in this model. Once this is selected, a value for the specific current can be extracted. From here, a transconductance value for the transistor can be calculated. Using a table consisting of early voltage values, the sizing of the transistor can be subsequently evaluated [29]. This model is substantially less complex than the threshold voltage model.

4.2.3 gm/ID Models

The gm/ID methodology focuses on inversion level as the selection point. This method relies on specifically collected data of the transistor being used. The data collected maps the density current to corresponding levels of inversion. Additionally, at least one other parameter is known in this method. Typically, the other known parameter is the value of the drain current in the transistor. Once the inversion level and the drain current are known, this can be used to find the corresponding density current and the transconductance. Knowing both the density current and the drain current allows for the extraction of transistor sizing [30, 31]. Additionally, this method can be used to directly measure intrinsic gain.

4.2.4 Previous Comparison Research

A comparison of the three methodologies was completed with a current mirror OTA design project [7]. This work covers the three discussed methods above, and compares final results in multiple parameters to the expected and designed for values. This design was completed with 45nm technology. The results can be seen in Table 4.2.

Table 4.2: Target and Simulated Values of Circuit Parameters for Varying Methodologies [7]

Parameter	***Target***	***V_{TH}-based models***	***Simplified EKV models***	***gm/ID methodology***	***Unit***
$g_{m,M1,M2}$	20	16.4	14.8	20.2	µS
$U_{GS,M1,M2}$	0.38	0.262	0.376	0.384	V
$U_{DS,M1,M2}$	0.43	0.418	0.509	0.425	V
$U_{DS,M10}$	0.12	0.238	0.124	0.116	V
$U_{GS,M3,M4}$	0.45	0.344	0.367	0.459	V
$I_{D,M1,M2}$	0.67;0.73; 0.96 [a]	0.68	0.70	0.96	µA
$I_{D,M6,M8}$	2.68;2.92; 3.84	2.95	2.96	3.94	µA
A_U	40	35.09	35.41	39.58	dB
GBW	10	7.32	9.3	12.53	MHz
Phase margin	>60	69.3	84.8	85.0	°

In regard to all parameters, the gm/ID methodology was the closest to the target results. The main parameters of importance here are gm, A_U, GBW, and Phase margin. Typically, these are parameters that are given as circuit specifications, and thus their accuracy is imperative. Given this, it is clear that the gm/ID methodology is far superior to the other models.

4.3 Conclusions

It is imperative to select the best model and configuration for transistor research. Since this work is focusing on individual parameter impact on gain, the circuit configuration with the highest gain is obvious for selection. Thus, the design circuit to measure gain variation will be in the common-source configuration. Additionally, it is important to have a deep understanding of the intrinsic characteristics for the transistors at hand. In order to have the most accurate and simple results, the gm/ID methodology will be used to analyze intrinsic behavior.

Chapter 5

Testbench Design for Gain Measurement

5.1 Testbench setups

This chapter includes a detailed description of the testbench setup. Two main testbenches were created. First, the a testbench was created to extract the intrinsic gain, which is the theoretical maximum gain of the device. Proceeding that, a common source gain testbench was established for parameterized measurements of the gain. Additionally included in this chapter is the description of SPICE parameters that were modified in the MOSFET model files. For all measurements, 1 V Supply devices were used, as described in Table 3.1.

5.1.1 Intrinsic Gain Measurement

To measure intrinsic gain, the gm/ID methodology discussed in Chapter 4 was implemented. Intrinsic gain is the maximum amount of gain a device can produce under given parameters. The intrinsic gain was measured under the conditions seen in Table 5.1. The lengths and widths were selected to match the necessary sizing of the common source gain measurement testbench.

Table 5.1: Parameter Setup

Length (m)	Width (m)	Temperature (ºC)	Corner Type
180n	480n	40	Typical Typical

The testbench setup can be seen in Figure 5.1. The intrinsic gain was determined for both NMOS and PMOS devices. For the NMOS configuration, the current was applied to the drain of the device. Meanwhile, for the PMOS configuration, the current was applied to the source. Other key differences such as body and gate connections are critical to collecting valuable data. An equation relating I_{Dense}, I_D, and the $\frac{W}{L}$ ratio can be seen in Equation 5.1. This equation was used to establish a sweep of $I_D$to adequately test the range of the device and determine the maximum intrinsic gain.

$$I_{Dense} = \frac{I_D}{(\frac{W}{L})} \tag{5.1}$$

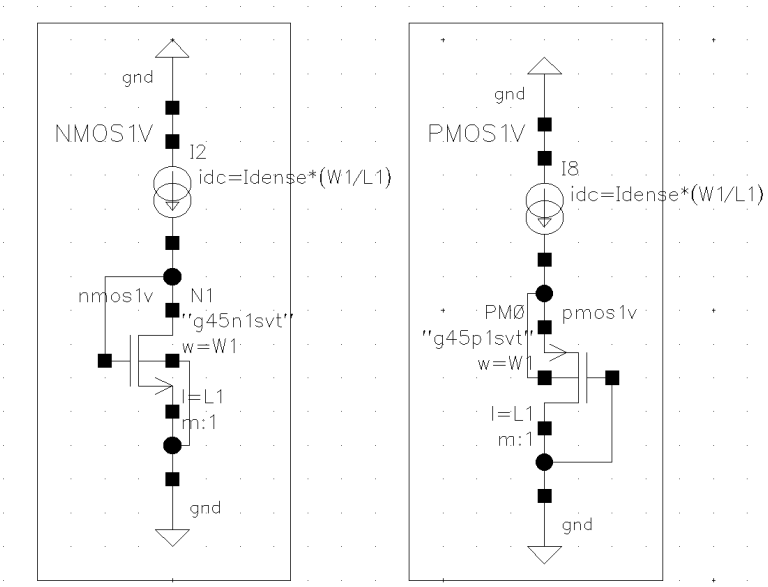

Figure 5.1: Intrinsic Gain Measurement Testbench

5.1.1.1 ADE Setup

A DC analysis was used to sweep the density current. This logarithmic sweep was completed from a density current of 1 pA to 100 uA, with 100 points per decade. The intrinsic gain was measured as a function of *gm* and *gds*, as seen in Equation 5.2. The getdata function in Cadence was used to readily measure the values of *gm* and *gds* for both the NMOS and PMOS devices. Subsequently, the ratio seen in Equation 5.2 was applied as an equation in Cadence, resulting in the expression seen in Equation 5.3. This expression produced a graph of the intrinsic gain plotted against the density current. From here, the *ymax* function was used to extract the maximum intrinsic gain, as seen in Equation 5.4. Additionally, the density current at which the maximum intrinsic gain was measured using the cross function as seen by the expression in Equation 5.5. It is to be noted that the NMOS device, N1, was used for all these measurements, but the same expressions were applied to the PMOS device as well.

$$IntrinsicGain = \frac{gm}{gds} \tag{5.2}$$

$$(getData(\text{"}N1:gm\text{"}?result\text{"}dc\text{"})/getData(\text{"}N1:gds\text{"}?result\text{"}dc\text{"})) \tag{5.3}$$

$$ymax((getData(\text{"}N1:gm\text{"}?result\text{"}dc\text{"})/getData(\text{"}N1:gds\text{"}?result\text{"}dc\text{"}))) \tag{5.4}$$

$$\frac{cross(\frac{(getData(\text{"}N1:gm\text{"}?result\text{"}dc\text{"})}{getData(\text{"}N1:gds\text{"}?result\text{"}dc\text{"})})ymax(\frac{(getData(\text{"}N1:gm\text{"}?result\text{"}dc\text{"})}{getData(\text{"}N1:gds\text{"}?result\text{"}dc\text{"}))1\text{"}either\text{"}nilnilnil)}{getData(\text{"}N1:gds\text{"}?result\text{"}dc\text{"}))1\text{"}either\text{"}nilnilnil)} \tag{5.5}$$

5.1.2 Common Source Gain Measurement

The common source configuration, as discussed in Chapter 4 was implemented to measure gain. The baseline parameters for this testbench are the same as those for the intrinsic gain measurement testbench, as seen in Table 5.1. The lengths and widths were selected to be four times the minimum sizing requirements to allow for adequate variation. The testbench schematic can be seen in Figure 5.2.

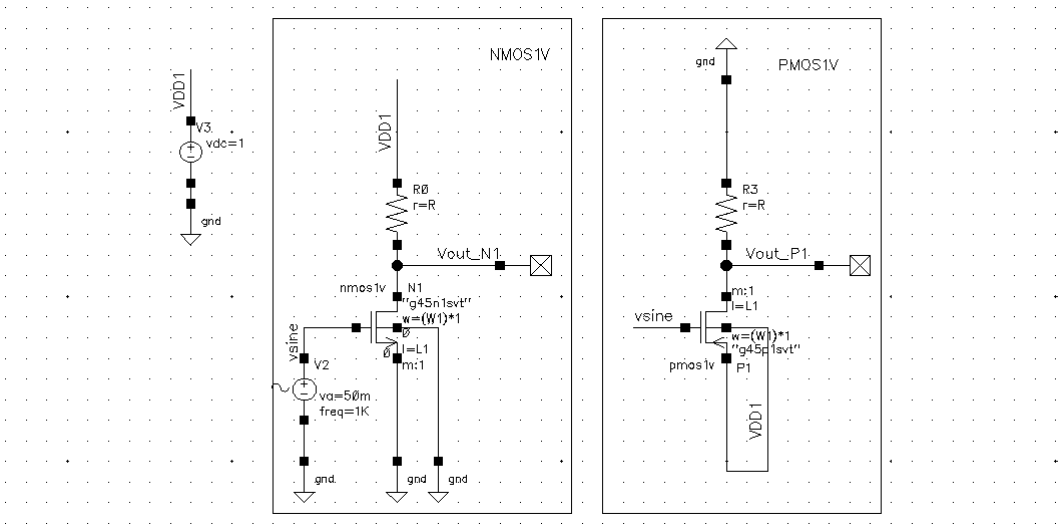

Figure 5.2: Common Source Gain Measurement Testbench

The load resistance was consistently set to 100 kΩ, this was a large enough value to be larger than the output resistance of the transistor and allow a large output voltage swing. This prevented the device from entering a condition of attenuation for most of the swept variables.

5.1.2.1 Modified Parameters for Common Source Gain Measurement

Ultimately, the parameters of interest in Chapter 3 needed to be narrowed down to feasible parameters for modification and analysis. There were four easily varied parameters through a standard Cadence ADE. The rest of the parameters of interest are embedded in the SPICE

models for the devices. The NMOS and PMOS model parameters from the PDK used were cross-referenced with the SPICE Model Parameters for BSIM4.5.0, as provided by the University of British Colombia [32]. The parameters of interest that were varied through the SPICE model were mobility, zero-bias threshold, oxide thickness, gate source capacitance per unit, gate drain capacitance per unit, and gate drain capacitance. The parameters and their descriptions can be seen below in Table 5.2.

Table 5.2: Modified Parameters in Common Source Gain Measurement

Parameter	Description
L1	Length of the transistor channel
W1	Width of the transistor channel
Area	Area of the transistor ($W1 * L1$)
T	Temperature of the transistor
du0	Mobility parameter
dvt0	Zero-bias threshold voltage
tox	Oxide thickness
cgs0	Non LDD region gate-source overlap capacitance per unit W
cgd0	Non LDD region gate-drain overlap capacitance per unit W
cgdl	Light doped gate-drain region overlap capacitance

5.1.2.2 ADE Setup

An AC analysis was applied to sweep the frequency and produce gain and phase plots. The AC logarithmic sweep was completed from 1mHz to 100 MHz with 100 points per decade. The dB20 function was used to generate the logarithmic plot for the gain, as seen in Equation 5.6. Similarly to Equation 5.4 for the intrinsic gain measurement, the *ymax* function was used

to measure the maximum gain from a the device, as seen in Equation 5.7. Again, the equations are specific to the NMOS device, but were equally applied to the PMOS device as well.

$$dB20(VF(\text{"}/Vout_N1\text{"})) \tag{5.6}$$

$$dB20(VF(\text{"}/Vout_N1\text{"})) \tag{5.7}$$

Chapter 6

Results and Discussion

The results of the simulations and analyses of the results are provided in this chapter. First, the baseline values will be established for reference. The gain results section will offer a comprehensive overview of the parameterized variations and their impact on the gain.

6.1 Baseline Values

First, the intrinsic gain was measured for both the NMOS and PMOS devices. The measurement was completed as described in Chapter 5. The results from the measurement can be seen in Table 6.1. Curiously, this is opposite to what is expected. NMOS devices typically have about twice the mobility as that of PMOS devices. Typically, higher mobility correlates to higher gain. This is likely a specific characteristic of the process design kit being used.

Table 6.1: Intrinsic Gain Baseline Results

Device	Gain (dB)
NMOS1V	26.26
PMOS1V	33.48

Next, the gain was measured for both the NMOS and PMOS devices in the common source configuration. This measurement was completed as described in Chapter 5. The results from this measurement can be seen in Table 6.2. Similarly to the results from the intrinsic gain, the PMOS device shows higher gain. Thus, the results are consistent through multiple testing methods. Additionally, it is to be noted the drastic drop between a common configuration and the intrinsic gain model. This shows there is significant amount of improvement that can be made to these devices to achieve excellent gain under specified parameters.

Table 6.2: Common Source Configuration Gain Baseline Results

Device	Gain (dB)
NMOS1V	6.478
PMOS1V	8.266

6.2 Gain Results

The results from the varied parameters in the common source configuration are detailed in the following sections. The discussion begins with the parameters easily modified in the Cadence ADE, then transitions into the parameters that can only be adjusted by modifying the SPICE models.

6.2.1 Length (m)

The first parameter varied was the length. The results can be seen in Table 6.3. Predictably, this variation had a large impact on the value of gain. This direct correlation comes from length having a relationship with the output resistance.

Table 6.3: Gain Results for Varied Length

Length (m)	NMOS1V Gain (dB)	PMOS1V Gain (dB)
45 n	4.32	3.043
90 n	6.247	7.164
135 n	6.621	8.248
180 n	6.478	8.266
225 n	6.181	7.925
270 n	5.824	7.452
315 n	5.446	6.929

The prediction would be that a smaller length would create a larger gain. Since gain is dependent on the ratio of W/L, smaller lengths would predictably correlate to higher gain. Figure 6.1 shows the graph rise and gradually fall, peaking at 135 n. Thus, it is likely that a smaller length does in fact correlate to a higher gain. Oftentimes, at very small lengths, unpredictable behavior may occur in models. Thus, there is a high probability that is the reason for the lower gain values at lower length values.

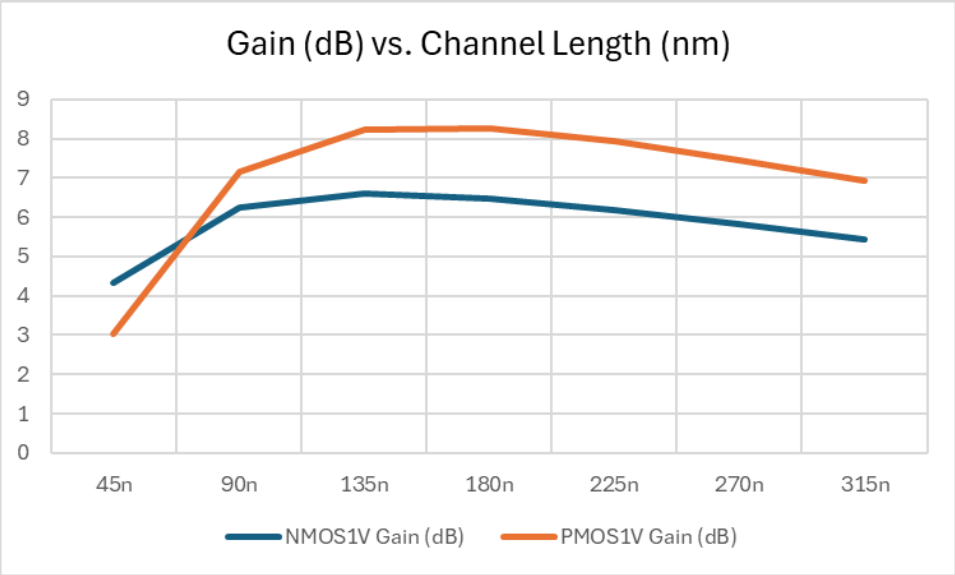

Figure 6.1: Channel Length Variation Gain Plots

6.2.2 Width (m)

The behavior of the variation of the width is exactly as expected. The results from this variation can be seen in Table 6.4. Since gain has a relationship with the W/L ratio, larger values of width are likely to correlate with higher values of gain.

Table 6.4: Gain Results for Varied Width

Width (m)	NMOS1V Gain (dB)	PMOS1V Gain (dB)
120 n	-1.207	-314.8m
240 n	2.829	3.904
360 n	4.997	6.487
480 n	6.478	8.266
600 n	7.55	9.533
720 n	8.365	10.44
840 n	8.992	11.06

Figure 6.2 shows the graph of the width compared to the gain. Clearly, a steady increase in width corresponds to a similar response in the gain. However, the graph does appear to flatten out as the width increases. A further extension of larger width values could show a flattened curve. Another point of interest is the negative values of gain seen at 120 nm. This shows that the device entered a range of attenuation, where it is no longer amplifying the circuit, but actively losing power. Therefore, at this length, which is minimum, the device goes out of its range of operation.

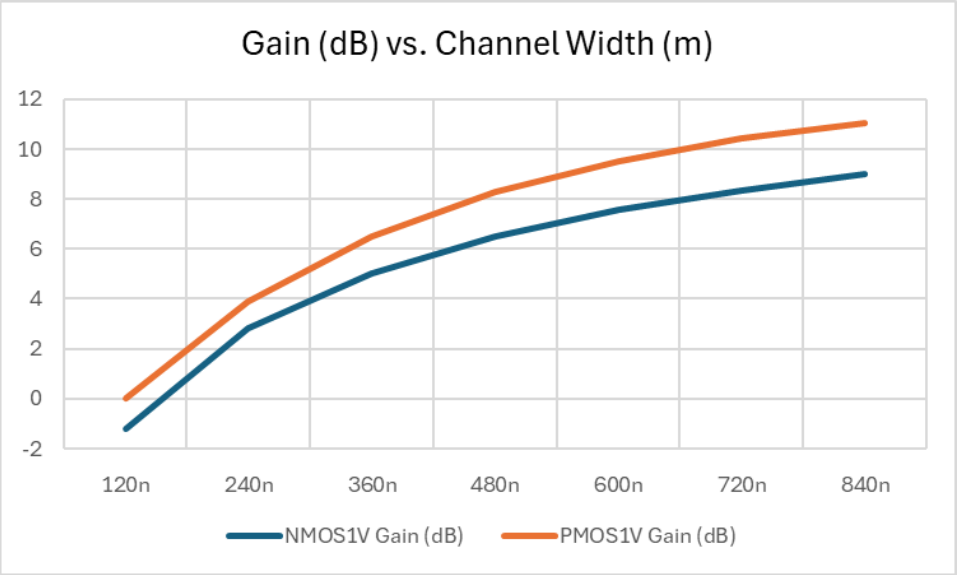

Figure 6.2: Channel Width Variation Gain Plots

6.2.3 Area

The length and width were varied simultaneously to display the impact of area on gain. The results can be seen in Table 6.5. Gain has a clear relationship with the ratio of W/L, however, area is the multiplication of W and L. Thus, the predicted results were that the highest gain would come from the devices with the largest area but smallest length.

Table 6.5: Gain Results for Varied Area

Area (nm^2)	Length (m)	Width (m)	NMOS1V Gain (dB)	PMOS1V Gain (dB)
48600	135 n	360 n	5.226	6.573
64800	135 n	480 n	6.621	8.248
81000	135 n	600 n	7.627	9.452
64800	180 n	360 n	4.997	6.487
86400	180 n	480 n	6.478	8.266
108000	180 n	600 n	7.55	9.533
81000	225 n	360 n	4.619	6.046
108000	225 n	480 n	6.181	7.925
135000	225 n	600 n	7.319	9.274

As displayed in Figure 6.3, the largest values of gain corresponded to the largest areas. However, it was predicted that the smallest lengths with the largest areas would have the highest values; this was not the case. Ultimately, the largest gain device correlated to the largest width, and an intermediate value of length; which created an area of 108000 nm^2. Interestingly, there were other combinations of width and length tested that resulted in the same area. Yet, despite having the same area, the other combinations of width and length preformed significantly worse. This sheds light on the delicate balance of optimizing lengths and widths.

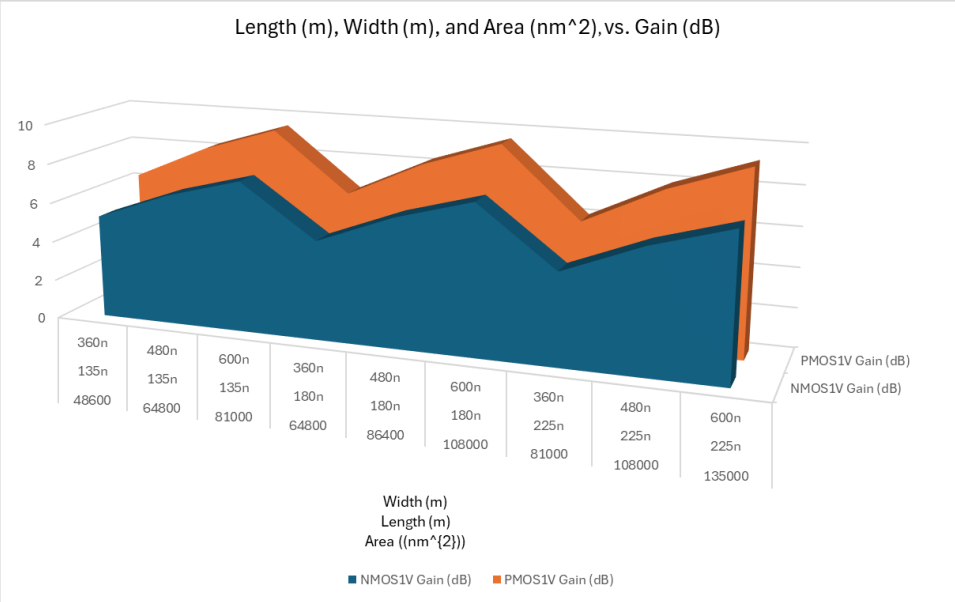

Figure 6.3: Channel Area Variation Gain Plots

6.2.4 Temperature

The temperature was varied from 10 to 70 degrees Celsius, with the midpoint being 40 degrees Celsius. The results can be seen in Table 6.6. Temperature tends to impact circuits in the opposite way as expected. It would be expected that higher temperature would cause electrons and holes to move faster, thus increasing mobility and thus increasing gain. However, higher temperatures cause electrons to interact more, bouncing off of each other, and thus creating chaos instead of a balanced stream of electrons.

Table 6.6: Gain Results for Varied Temperature

Temperature (ºC)	NMOS1V Gain (dB)	PMOS1V Gain (dB)
10	6.526	8.847
20	6.518	8.656
30	6.502	8.461
40	6.478	8.266
50	6.446	8.069
60	6.408	7.871
70	6.363	7.672

The results seen in Table 6.4 show the effects of temperature on the gain of the devices. Interestingly, the PMOS device was much more responsive to temperature variations than the NMOS device. This may indicate that holes are more sensitive to temperature variations than electrons.

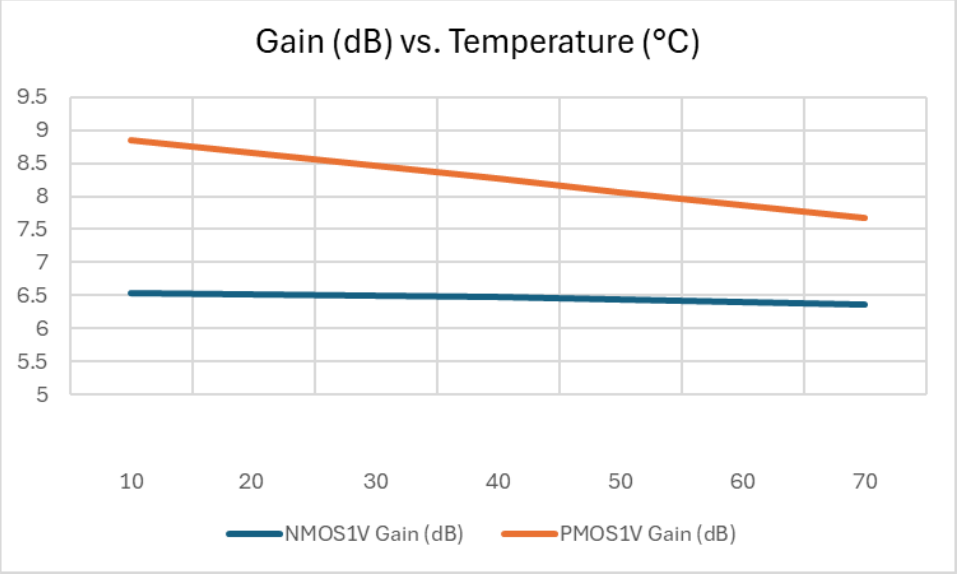

Figure 6.4: Temperature Variation Gain Plots

6.2.5 Mobility

Mobility ($\frac{cm^2}{(V*s)}$) is an extremely sensitive parameter, thus careful precaution was taken while making variations, such to not reach levels of attenuation. The results can be seen in Table 6.7. As predicted, higher values of mobility correlate to higher values of gain.

Table 6.7: Gain Results for Varied Mobility

Mobility ($\frac{cm^2}{(V*s)}$)	NMOS1V Gain (dB)	PMOS1V Gain (dB)
-5E-4	6.266	8.129
-1E-4	6.436	8.239
-1E-5	6.474	8.263
0.00	6.478	8.266
1E-5	6.482	8.268
1E-4	6.519	8.292
5E-4	6.678	8.396

Despite the small variations in the mobility, a clear trend was still present with an increasing mobility and gain, as seen in Figure 6.5.

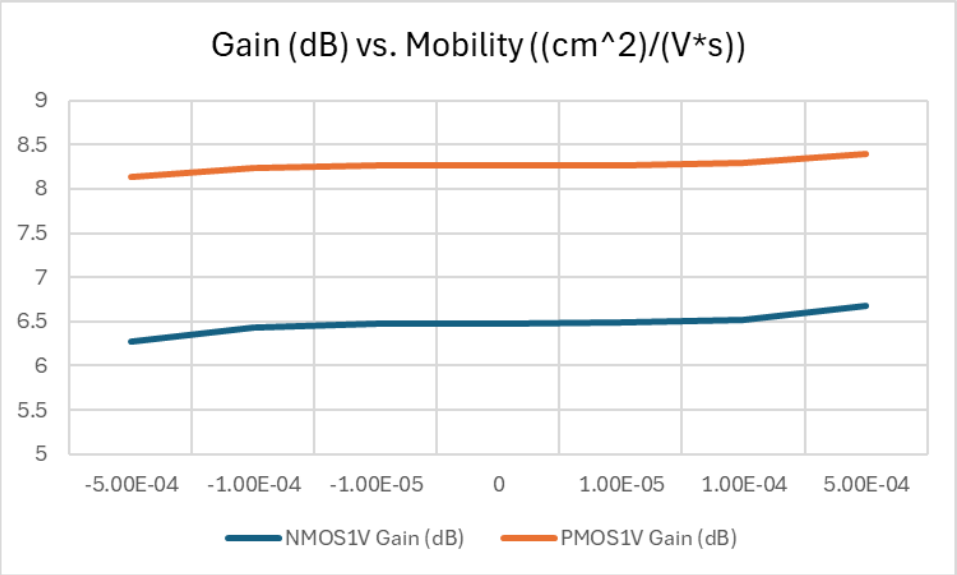

Figure 6.5: Mobility Variation Gain Plots

6.2.6 Zero-Bias Threshold Voltage

No predictions were made about the impact of the zero-bias threshold voltage on the gain of the circuit. The results can be seen in Table 6.8. Since the threshold voltage is unlikely to have an impact on the output resistance, it is likely that varying the threshold voltage impacted the transconductance of the devices. There is a known relation between threshold voltage and transconductance.

Table 6.8: Gain Results for Varied Zero-Bias Threshold Voltage

Zero-Bias Threshold Voltage (V)	NMOS1V Gain (dB)	PMOS1V Gain (dB)
-0.03	7.973	6.072
-0.02	7.581	6.923
-0.01	7.08	7.655
0.00	6.478	8.266
0.01	5.779	8.749
0.02	4.99	9.095
0.03	4.116	9.282

The results show opposite effects on the NMOS and PMOS devices in Figure 6.6. This is predictable, as PMOS devices have negative threshold values and NMOS devices have positive values. Therefore, by increasing the zero-bias threshold voltage to a positive number, the actual threshold voltage of the PMOS is decreasing. Meanwhile, the opposite applies for the NMOS device.

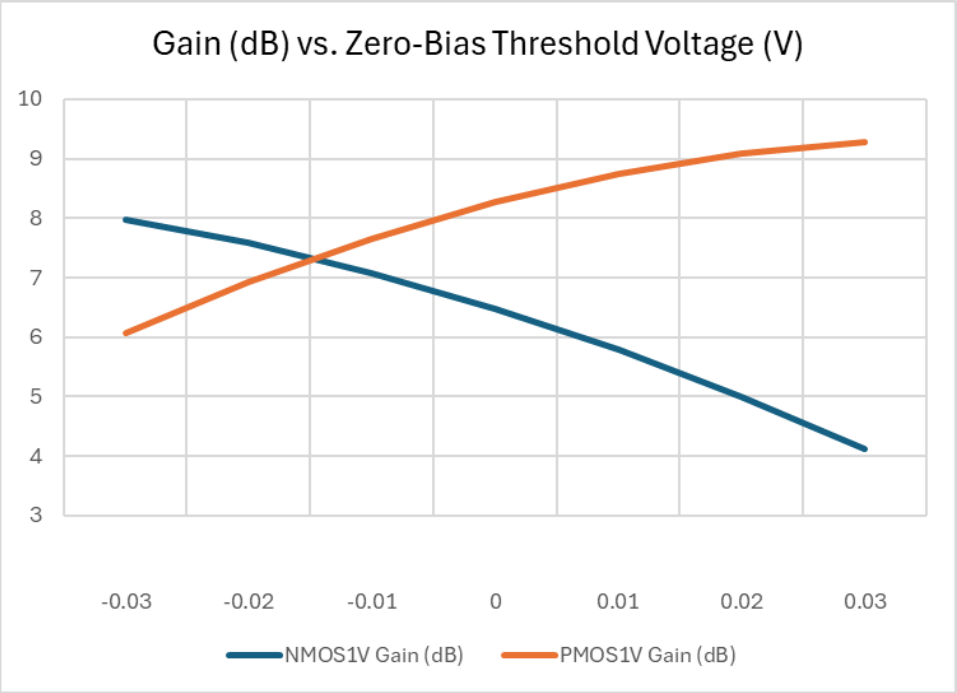

Figure 6.6: Zero-Bias Threshold Variation Gain Plots

6.2.7 Oxide Thickness

It was predicted that thicker oxides would correspond to lower gain, as less charge could be stored, thus creating a lower mobility. The results can be seen in Table 6.9.

Table 6.9: Gain Results for Varied Oxide Thickness

Oxide Thickness (m)	NMOS1V Gain (dB)	PMOS1V Gain (dB)
2.2E-9	6.813	8.472
2.3E-9	6.661	8.374
2.35E-9	6.58	8.321
2.4E-9	6.478	8.266
2.45E-9	6.408	8.206
2.5E-9	6.318	8.149
2.6E-9	6.133	8.026

A negative relationship between oxide thickness and gain is observed in Figure 6.7. This is exactly as expected, and there is no anomalies to the data.

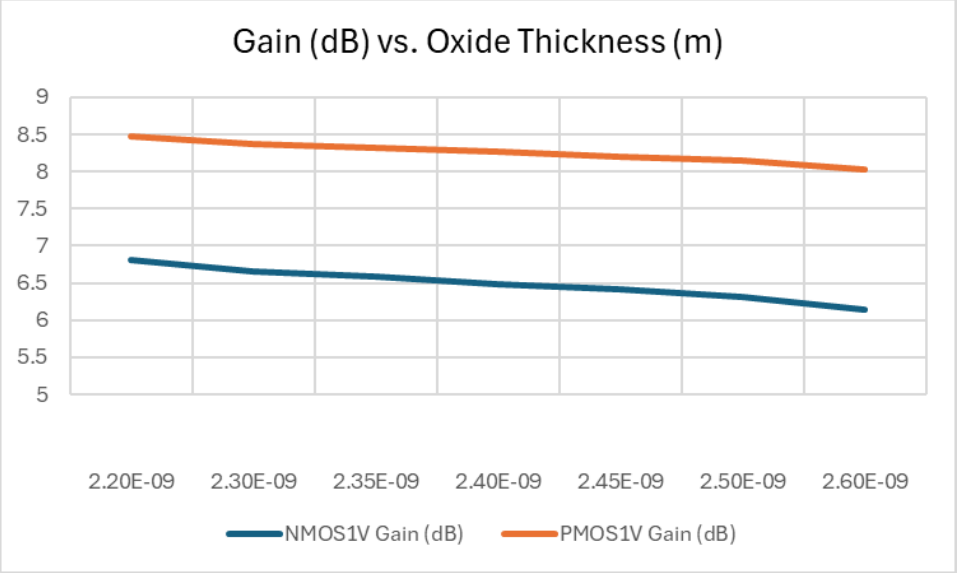

Figure 6.7: Oxide Thickness Variation Gain Results

6.2.8 Capacitance

The gate-source, gate-drain, and lightly doped gate-drain capacitance values were varied over the same set of values. The results for the gate-source capacitance can be seen in Table 6.10. The results for the gate-drain capacitance can be seen in Table 6.11. The results for the lightly doped gate drain capacitance can be seen in Table 6.12. None of these variations had any impact on gain, even at significant values of capacitance. This was as predicted.

6.2.8.1 Gate-Source Overlap Capacitance

Table 6.10: Gain Results for Varied Gate-Source Overlap Capacitance

Gate-Source Overlap Capacitance (F)	NMOS1V Gain (dB)	PMOS1V Gain (dB)
0.00	6.478	8.266
1E-12	6.478	8.266
2E-12	6.478	8.266
3E-11	6.478	8.266
4E-5	6.478	8.266

Table 6.11: Gain Results for Varied Gate-Drain Overlap Capacitance

Gate-Drain Overlap Capacitance (F)	NMOS1V Gain (dB)	PMOS1V Gain (dB)
0.00	6.478	8.266
1E-12	6.478	8.266
2E-12	6.478	8.266
3E-11	6.478	8.266
4E-5	6.478	8.266

Gate-Drain Overlap Capacitance

Table 6.12: Gain Results for Varied Light Doped Gate-Drain Overlap Capacitance

Light Doped Gate-Drain Overlap Capacitance (F)	NMOS1V Gain (dB)	PMOS1V Gain (dB)
0.00	6.478	8.266
1E-12	6.478	8.266
2E-12	6.478	8.266
3E-11	6.478	8.266
4E-5	6.478	8.266

Light Doped Gate-Drain Overlap Capacitance

6.3 Optimization Observations

The observations from these experiments indicate that the highest gain value would occur when the length is small, width is large, area is large, temperature is low, mobility is high, the zero-bias threshold voltage works to decrease the threshold voltage, and the oxide thickness is thin. A test of this was completed to achieve maximum gain based on these variations. The values used for the simulation can be seen in Table 6.13. Despite these being the optimized individual results from the simulations, there is a deeper connection between parameters that needs to be further investigated, as evidenced by these results. Though the gain is increased from the baseline value, this is not the maximum gain that has been achieved through testing. This shows the overall complexity and the intersectionality of parameters.

Table 6.13: Optimized Values for Largest Gain

Device	NMOS1V	PMOS1V
Length (m)	135 n	180 n
Width (m)	840 n	840 n
Area (nm^2)	113400	151200
Temperature (ºC)	10	10
Mobility ($cm^2/V*s$)	5E-4	5E-4
Zero-Bias Threshold Voltage (V)	-0.03	0.03
Oxide Thickness (m)	2.2E-9	2.2E-9
Gain (dB)	7.053	9.14

Chapter 7

Conclusion

This work focused on the systematic variation of parameters to analyze the effects of gain on a common source amplifier. The results were mostly as predicted, with a few anomalies marked and accounted for the in the results discussion. The primary take away from this work is the impact of mobility on gain. Many parameters directly trace back to mobility, such as temperature and oxide thickness. Therefore, mobility seemed to have the largest overall impact on the gain of the tested devices.

7.1 Future Work

Future work for this study could be extensive. First and foremost, many more parameters in the SPICE model can be varied to see their effects on gain. Additionally, an investigation of the interconnectedness of the parameters would be extremely beneficial to future work. The other main topic of study that could be investigated more thoroughly is different supply and different threshold devices. In this project, only 1 V supply devices were used. However, 2 V supply devices are present in the library and could be investigated. Additionally, the library

also supports high, low, and nominal threshold voltage devices. Another interesting avenue for gain variation would be multi-gate device investigations. This could be done through double-gate devices, FINFETs, or GAAFETs.

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