# Full-Wafer DMOS Fabrication at RIT

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**Abstract- A well understanding of basic structure of Double Diffused Metal Oxide Semiconductor (DMOS) and the concept of segmented large capacitor creates possibility to produce a full-wafer DMOS. Using the Mylar Mask Technology, the final metal layer can be patterned accordingly so that to leave out any damaged fragments. Thus, it will increase the possibility of higher yield. Most of the basic fabrication processes will be done at RIT microelectronics lab facilities, and the functionality tests will be conducted at Naval Research Lab. Therefore, this paper is intended to give a general overview of concepts involved and the fabrication processes.**

## 1. INTRODUCTION

Power MOSFET found its origin in the MOS integrated-circuit technology. Prior to the development of power MOSFET, the predominantly used high-speed power device was the power bipolar transistor. Although this type of power device provides needed characteristics, such as current handling capability of several hundred amperes and blocking voltages of several hundred volts, it has some major drawbacks.

First, the bipolar transistor has a complex and expensive base drive circuitry. Not only it needs large base drive currents to maintain the device in the on-state, but also requires even a larger base drive currents to obtain high-speed turn-off. Secondly, under the application of high current and voltage simultaneously, the bipolar transistor is prone to second breakdown failure mode. These disadvantages led to the development of power MOSFET technologies.

Unlike the bipolar device, no significant gate current is needed to operate in either the on-state or off-state condition. The control signal is done through induction process. A bias voltage is applied to the gate electrode that will effect the state of charge of the semiconductor that is separated by a thin layer of oxide. Furthermore, the power MOSFET also reduced the possibility of second breakdown failure. There are several structures of power MOSFET that have been thoroughly developed. In this project, however, only the vertical DMOS will be explored and used.

In order to obtain higher power handling capability, DMOS are usually constructed in repetitive pattern of small cells. This project will explore the possibility to construct a full-wafer of these DMOS cells. This device is expected to have current handling of several thousands amperes and blocking voltage of several thousand volts. The future application of the device will be used for mega Watt (~12 MW) Power Converters and Drivers for: utility power distribution, electric drive for ships, tanks, and locomotive, linear motors for air craft carrier launch and arrest.

## 2. BACKGROUND THEORY

### *A. Introduction to Basic DMOS Structure*

The basic structure of vertical DMOS is shown in Figure 1. N-type substrate is normally used because electrons, the majority carrier, have higher mobility, producing faster performance. The doping concentration of the substrate will determine the on-resistance of the device. In addition, the on-resistance can also be minimized by using wafer with (100) orientation because it provides the highest surface mobility.

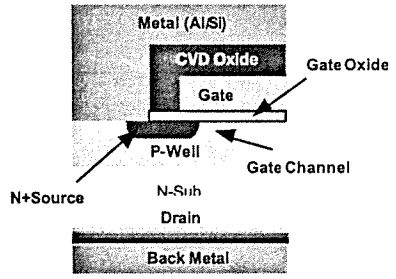


**Figure 1.** Basic Vertical DMOS Structure

As shown in Figure 1, the electrons path is vertical, from the source region that is on the top surface, to the drain region, which is the backside of the wafer. For this reason, the device is named vertical DMOS. The backside of the wafer is usually doped heavily to reduce the contact resistance thus minimizing the on-resistance.

The gate oxide quality is also of a great concern since the operation of the device is done by modulating an electric field across the gate oxide. Producing a defect-free gate oxide has been a major challenge, especially if it involves a large area, which is vulnerable to physical defects, such as pinhole and local oxide conglomeration.

The basic operation of DMOS is similar to the MOSFET technology. In order for the current to flow from drain to source, a path needs to be created in the p-well region to allow the flow of electrons from source to drain. For this to happen, a positive bias voltage is applied to the gate electrode that will repel the holes in the p-well region thus creating an n-channel that is the gate channel. If there is a potential difference between the drain and the source, current flows. In addition, the gate channel length is determined by the junction depth of p-well and n+souce.

In the on-state condition, the source is grounded, and a positive voltage is applied to the drain. Assuming the channel exists, current will flow from drain to source. Unlike in the MOS integrated circuit, conduction is done by the majority carrier in the n-type substrate in power DMOS. It is important to note that the source and the p-well is shorted at all time to establish a fixed potential to p-well region during device operation. In the off-state condition, the gate electrode is grounded by short-circuit it to the source. By doing this, the conducting channel at p-well region is shut-off.

The robustness of the fabrication process will determine the electrical characteristics of the device. The following are some device parameters that are important to understand and can be used as a quantitative measure of how well the device was fabricated.

### *1. Forward Blocking Capability*

To obtain this device parameter, the gate and the source is shorted, and a positive voltage is applied to the drain. As a result, depletion layer is formed at the p-well/n-sub junction. As the drain voltage increases, the depletion width also increases. When the depletion region reaches the n+source/p-well junction, breakdown occurs. In the DMOS structure, the doping profile and curvature are crucial in determining the forward blocking capability.

### *2. Threshold Voltage*

Threshold voltage is the minimum bias voltage applied to the gate electrode at which a strong inversion begins to occur, creating the n-channel for current to flow.

### *3. On-Resistance*

The on-resistance is the total resistance of the current path, from the drain to source. This parameter can be broken down to a series of smaller resistances: n+source, channel, junction, n-sub, and n+contact resistance. On-resistance is very important parameter because it determines the power rating of the device.

## *B. The Concept of Segmented Large Capacitor*

In order to understand the idea of full wafer DMOS, it is crucial to grasp the basic concept of segmented large MOS capacitor. The oxide layer is the primary concern in this matter. As it is understood, the dimension of the oxide will determine the capacitance. However, even more crucial than the dimension is the physical robustness of the oxide, such as defect density and pinholes. As illustrated in Figure 2(a), a single tiny pinhole will ruin the whole device because it will short-circuit the two electrodes.

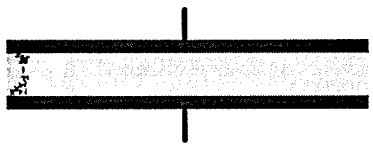

**Figure 2.** Oxide Defects in Large Capacitor

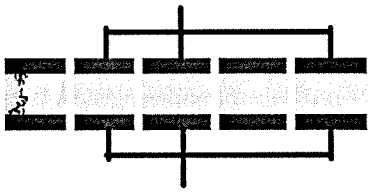

**Figure 3.** Segmented Large Capacitor

As a solution, the large capacitor is segmented into smaller capacitors; thus confining the defects to smaller areas. After testing the whole capacitors segments, good capacitors are then connected in parallel as shown in Figure 3. Therefore, the method will significantly increase the yield.

## *C. Full-Wafer DMOS*

In the same manner, the fabrication of a full-wafer DMOS is most likely to fail due to poor large gate oxide due to presence of particulates, defects, and pinholes. Adopting the idea of segmented large capacitor, this project will attempt to fabricate a full-wafer DMOS.

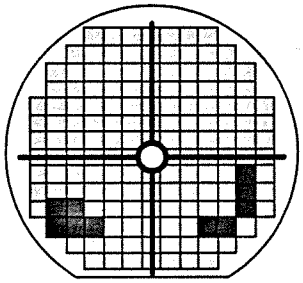

**Figure 4.** Full Wafer DMOS

The mask will be designed in such a way to repeat DMOS cells on the entire wafer. Prior to the last metal step, test will be conducted on each of the DMOS cell. The damaged cell will be marked, and using the mylar mask technology the final metal layers will be patterned in such a way to connect working devices. Figure 5 shows a wafer of the preliminary experiment with mylar mask.

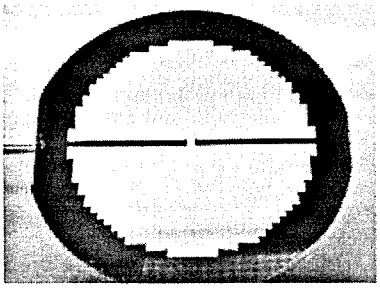

**Figure 5.** Preliminary experiment with mylar mask.

## 3. FULL-WAFER DMOS FABRICATION PROCESS

The full-wafer DMOS process was developed from an established RIT CMOS process. It involves four-level mask with the mylar mask as the last photo step. Figure 6 shows the cross sections and process flow of the fabrication process.

Four-inch N-substrate wafer with low resistivity and (100) crystal structure will be used. After proper cleaning procedure, 700 Å of gate oxide is thermally grown. A layer of 6000 Å of polysilicon is deposited on top of the oxide using LPCVD. The dopant concentration on the polysilicon then is adjusted by controlled phosphorous diffusion. The polysilicon then is patterned using standard procedure of photolithography into gate electrodes of the DMOS cells as illustrated in Figure 6(a).

Boron implant of 60 keV and dose of 4e13 $cm^{-2}$ is done at 7 degree off axis to minimize channeling effect (see Figure 6(b)). The implanted

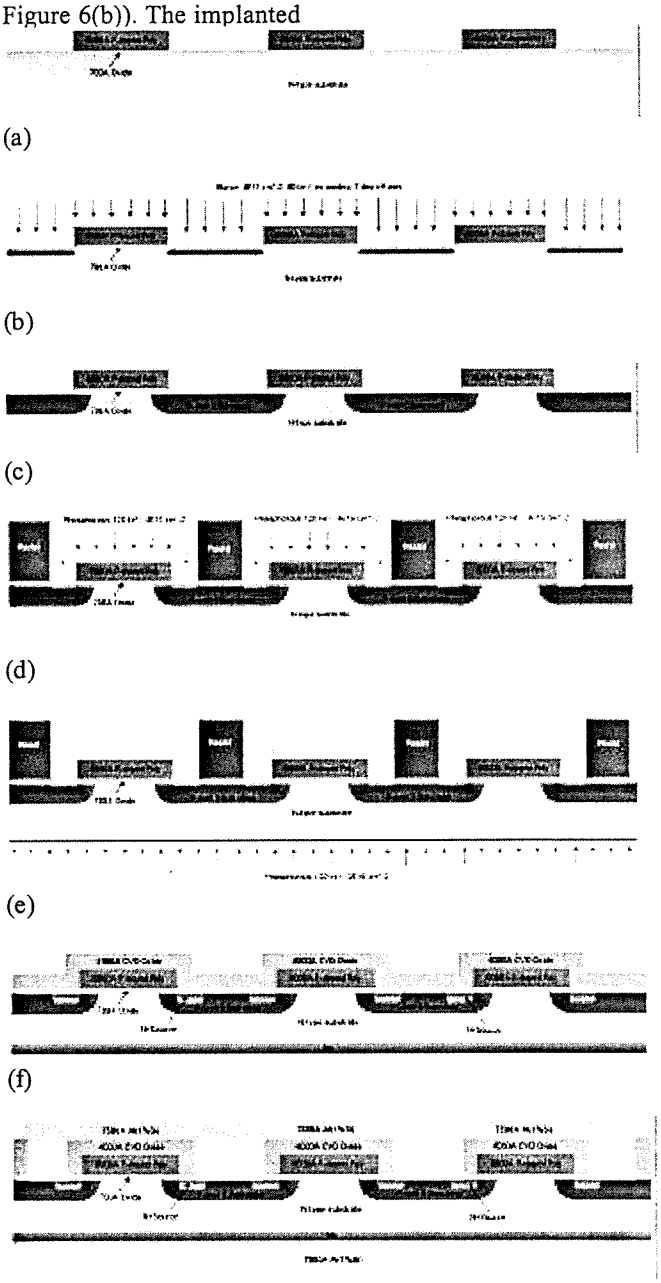


**Figure 6** Cross Sections of Full-Wafer DMOS. The drawing doesn't reflect the proper scaling.

boron then is annealed at 1100°C for 255 minutes at $N_2$ ambient, forming the p-well region as shown in Figure 6(c). After this step, a layer of photoresist is applied on the front side of the wafer. This makes possible for the stripping of polysilicon at the backside of the wafer.

The next step is to form the n+source region. The second level of photolithography defines the area for

n+source as seen in Figure 6(d). Phosphorous implant of 120 keV and dose of 4e15 $cm^{-2}$ s is done using cooling system at 7 degree off axis. Phosphorous is also implanted at the backside of the wafer at lower dose of 2e15 $cm^{-2}$. After annealing it at 1000°C for 20 minutes in $N_2$ ambient, a 1000 Å of oxide is thermally grown by wet oxidation. On top of the oxide layer, 4000 Å of CVD oxide is deposited as an insulator layer between the poly gate and metal layer. To increase the oxide performance, it was annealed at 900°C for 30 min in $O_2$ ambient (see Figure 6(e)).

As shown in Figure 6(f), the third photolithography step is to define the contact window. The next step is to deposit 7500 of aluminum with 1% of silicon using sputtering technique both at the front and back side of the wafer. The final metal layers then is patterned using the mylar mask technique. Figure 6(g) shows the final cross section of the device.

## ACKNOWLEDGMENT

Dr. Fritz Kub of Naval Research Lab is the initiator and sponsor of the project. Dr. Santosh Kurinec of RIT is a tremendous resource of knowledge, help, and motivation. Charles Gruener has been a great assistance to the project.

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