Design and Fabrication of On-Chip Inductors

Robert K. Requa
Microelectronic Engineering
Rochester Institute of Technology
Rochester, NY 14623

Abstract-- An inductor is a conductor arranged in an appropriate shape (such as a conducting wire wound as a coil) to supply a certain amount of self-inductance. This passive device stores magnetic energy.

Simple spiral planar inductors of varying geometry were designed and fabricated on a silicon substrate insolated by silicon oxide. The process chosen for fabrication of the devices was the copper damascene process. Line widths and spaces varied from 5μm to 20μm. Thickness of the copper wire was approximately 1.5μm. The inductors were isolated from the silicon substrate by 0.5μm of SiO_2 and wires were insolated with the same material. Theoretical inductance values for the designed inductors ranged from 17nH to 300nH.

1. INTRODUCTION

An inductor is a conductor arranged in an appropriate shape (such as a conducting wire wound as a coil) to supply a certain amount of self-inductance [1]. Inductance of two magnetically coupled loops is defined as:

$$L = \frac{\Lambda}{I_1}$$

Λ is the flux linkage and I_1 is the current flowing through the loop. Inductance can also be defined as:

$$\phi = \oint B \bullet ds$$

$$L = \frac{\oint B \bullet ds}{I} \text{ (Henry)}$$

Where ϕ is defined as the flux, I is current, and B is magnetic flux density. Two example of simple devices that can be modeled are a solenoid and toroidal. The inductance of a simple solenoid device is $L_{SOLENOID} = \mu_o\mu_r n^2 A$ [H]. The inductance of a toroidal device is $L_{TOROIDAL} = (\mu_o\mu_r n^2 h/2\pi) * (\ln b/a)$ [H], where a = inner radius, b = outer radius, and h = height. It is also important to define the voltage and quality factor (Q) of an inductor.

$$V_L = L\frac{dI}{dt}$$

$$Q = 2\pi \frac{\text{Time average energy stored at a resonance frequency}}{\text{Energy disipated in one peroid of this frequency}}$$

This passive device allows magnetic energy to be stored, which has many applications in circuit design.

Some applications for inductors on a chip include RF circuits, communications, passive components in microwave circuits, micropower converters, magnetic microsensors, magnetic microactuators, and magnetic MEMS systems. There are several types of inductors that have been fabricated over the years. They can be broken down into three categories; planar types, 3D micromachined planar types, and micromachined planar inductive components with closed magnetic circuits. These groups can be further divided into subcategories. They include spiral, meander, solenoid, and toroidal meander.

Requirements for an inductor on a chip (IOC):

- Must have High current carrying capacity
- High magnetic flux density
- Closed magnetic circuits
- Low product cost
- CMOS compatibility

Areas that require improvement are accurate inductance with small device area, high quality (Q-) factor, high peak -Q frequency, large inductance (L), reduction of substrate loss and metal resistance, minimize both parasitic coupling to the substrate and inductor area, and CMOS

compatibility of process. There are several different methods of reducing substrate loss. These methods include using high resistivity substrate, etching the substrate underneath, insulating the inductor from substrate with thick polyimide, or oxidized porous Silicon (OPS), or diffused shield under oxide (DUO). Ways to reduce metal resistance are thick gold metalization layer, multiple metal layers in parallel, or copper metalization.

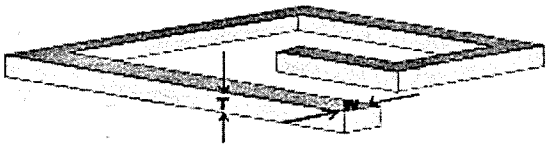
Some of the current inductor technologies are two level planar inductor using normal lithographic processes, 3D microfabrication using a novel sacrificial metallic mold (SMM), and other 3D methods involving polyimide as a mold and insulating material.

2. DESIGN

The design of inductors on a chip are dependent upon many factors. These factors include geometry, type of insulating material, number of turns, and type of conductor used.

Geometry plays an important role in the inductance. The width of the wire and spacing of wires determines the density of lines in the spiral planar inductor. Refer to Figure 1 below.

Figure 1: Define width and thickness of wire



This directly affects the number of turns (n) in the design. The inductance increases by a factor of n^2. The thickness of the wire in conjunction with the width also affects inductance. This is due to flux created by magnetic fields.

Wires must also be insulated by a good insulator such as silicon oxide, or an air gap. The addition of a magnetic material between insulated wires will increase the inductance of the design. The quality factor (Q) can be increased by choosing a conductor with low resistivity.

A total of ten inductors were designed in Mentor Graphics IC Station layout tool. All inductors were built on a 4-inch silicon substrate insulated by 5000A of silicon oxide. The theoretical inductance values were designed to range from 17nH to 300nH. The theoretical equation used to calculate inductance was from a modified Wheeler Formula [3]:

$$L_{mw} = K_1 \mu_o \frac{n^2 d_{avg}}{1 + K_2 \rho} \quad [3]$$

The values of K1 and K2 are constants, where K1 = 2.34 and K2 = 2.75. These constants are dependent upon geometry. For this model, an inductor for a given shape is completely specified by the following: number of turns n, the outer diameter d_{out}, the inner diameter din, the average diameter $d_{avg} = 0.5(d_{out} + d_{in})$, or the fill ratio, defined as $\rho = (d_{out} - d_{in})/(d_{out} + d_{in})$. The symbol μ_o is the permeability of free space equal to $4\pi \times 10^{-7}$ H/m.

Geometry and number of turns were varied to investigate the effects on inductance as stated above in the abstract. Refer to Table 1.1 below.

Table 1.1: Inductor designs

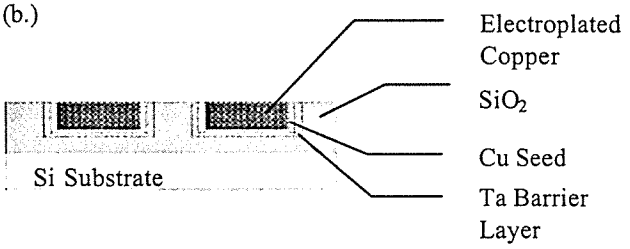
Inductor #	Line width (um)	Space Width (um)	(n) # of turns
1	5	5	15
2	10	5	15
3	10	10	15
4	10	15	15
5	10	20	15
6	15	5	15
7	20	5	15
8	10	5	5
9	10	5	10
10	10	5	20

Copper was chosen as the conductive material. Thermal Silicon oxide two microns thick was chosen as the insulating material. A square spiral planar geometry was used for ease of layout and fabrication. Refer to figure 2a.

Figure 2: 3D Design and Cross Section

(a.)

(b.)

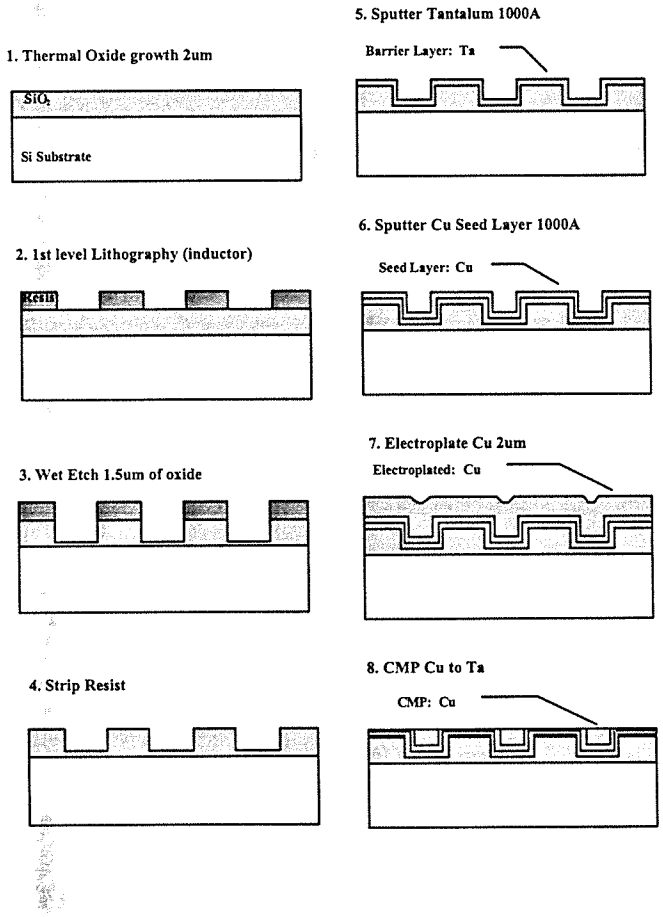


All inductors were designed with one level of metal to reduce amount of time for fabrication. The process used to fabricate the inductors designed in this project was a single copper damascene process.

2. PROCESS

The purpose of the process used in this project was to demonstrate a single copper damascene process and provide the groundwork for future research in the integration of inductors on a chip. With slight variation to the process used in this project, all designed inductors will be CMOS compatible. There are several key steps for the process used in fabrication of the designed inductors. These steps are deposition of insulating material, 1st level lithography, etching of insulator, deposition of barrier and seed layer, electroplating of copper, chemical mechanical planarization of copper, and electrical testing. The process steps will be described below. Refer to Figure 3 for process steps

Figure 3: Process Steps



A. Thermal oxide growth

Approximately two microns of thermal silicon oxide was grown on a p-type substrate. This oxide was grown in the Bruce Furnace Tube 01 with recipe #420 20,000A wet field oxide. For demonstration purposes thermal oxide was chosen because it provided the best uniformity and control of thickness for the desired insulating material. To make the process CMOS compatible, other means of deposition of silicon oxide could be used. Some examples include LTO, or a PECVD oxide. It also can be noted that other insulating materials could have been used instead of silicon oxide. Some examples could be air, polyamide, or SU8.

B. 1st level lithography

The 1st level lithography used in this process was RIT's standard one-micron resist recipe. The GCA1006 coat track was used to coat one micron of positive photoresist. All parameters were set the same as RIT's process. The GCA g-line stepper was used for exposure. A different stepper job was used to compensate for a slightly larger chip size. Development was completed on the GCA1006 development track. All parameters were identical to RIT's standard development program.

C. Etching

Wafers were wet etched in BOE for 17.5 minutes. Wet etching was chosen to reduce the amount of processing time. The ideal etch would be an anisotropic plasma etch with an ICP power source. This process would require a deep UV curing step prior to etching, or a much thicker resist. After etching, resist was ashed, and RCA clean is necessary.

D. Deposition of Barrier and Seed layer

Tantalum was chosen as the barrier layer. The thickness was 1000A. Next a 1000A copper seed layer was deposited. Both Ta and Cu were sputtered in a CVC601 sputter system. The base pressure reached in the system was 5E-6 torr. First a pre-sputter of Ta was conducted for 10 minutes followed by an 8 minute sputter. An 8-inch target was used for better uniformity across the wafers. Next, without breaking vacuum, copper was pre-sputtered for 10 minutes. This was followed by an 8 minute sputter of copper. The Cu target was also 8-inch. This process was developed by Deepa Gazula.

E. Electroplating of copper

Copper electroplating was conducted on a Reynolds Tech electroplating system. The electroplating recipe used

was 2.50A for 5 minutes at a total of 12.5 A-min. The temperature of the bath was approximately 25°C and allowed to warm up for four hours. Wafers were plated one at a time. An o-ring was placed on back of wafer to help increase contact to electrode. This process was developed by Keith Udut

F. Chemical Mechanical Planarization of Cu

CMP was conducted in the CMP lab on the tool designated for copper polishing. The CMP process used in this project was a two step process. All wafers were polished one at a time at the first step, then same procedure was followed for second step. The first step involved polishing with a fast removal rate slurry. The second step used a slower removal rate slurry. The faster slurry had a removal rate that was 10 times greater than the slower slurry. All copper except approximately 2000A was removed with first slurry. The second slurry was used to remove the remaining copper. The purpose of the second slurry was to reduce the effects of dishing. Total process time was 48 minutes. This process was developed by Jeffery Perry.

G. Electrical testing and characterization

Some electrical testing and characterization was completed for the devices. Resistance measurements were taken using analyzer 3. An LCR bridge was used to try and measure inductance with no success. Further testing on a network analyzer capable of measuring such small inductance is necessary in the future.

3. RESULTS

A single copper damascene process has been demonstrated in this project. Resistance measurements indicate that devices will work. Refer to table 2 for data.

Table 2: Resistance Measurements

Inductor #	Average Measured Resistance (ohm)	Theoretical Resistance (ohm)
1	79.67	64.200
2	76.63	37.596
3	68.77	43.080
4	74.53	48.108
5	72.53	53.304
6	69.07	28.960
7	64.13	24.462
8	21.13	9.480
9	43.57	21.960
10	120.00	57.720

Measurement of inductance still needs to be completed to verify designs. Refer to Table 3 below for theoretical inductance values. Also quality factor needs to be measured.

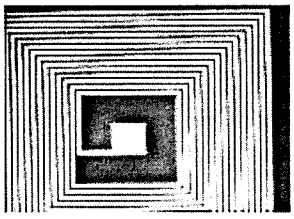
Table 3: Theoretical Inductance using Modified Wheelers Equation

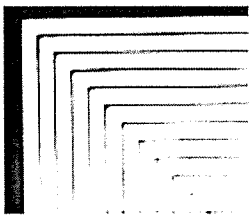
Inductor #	Line width (um)	Space width (um)	(n) # of turns	Lmw (nH)
1	5	5	15	155.34
2	10	5	15	159.65
3	10	10	15	167.15
4	10	15	15	176.34
5	10	20	15	186.52
6	15	5	15	167.74
7	20	5	15	177.69
8	10	5	5	17.74
9	10	5	10	69.06
10	10	5	20	297.67

Figure 4a – 4d are some microscope pictures of fabricated inductors. There are well-defined lines and spaces as can be seen in each figure. Refer to figures below.

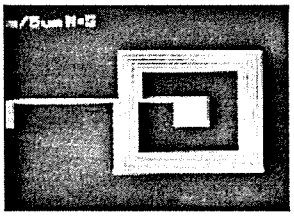
Figure 4: microscope pictures of fabricated inductors

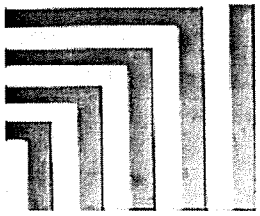
(a.) (b.)





(b.) (d.)





The next three pictures in figure 5 are SEM pictures of fabricated devices. It must be noted that samples were not prepared properly. These pictures provide a cross sectional view of a several lines, single line, and measurements of etch profile.

Figure 5: SEM pictures

(a.)

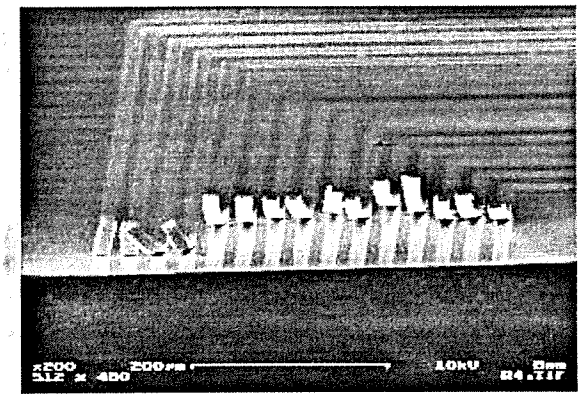
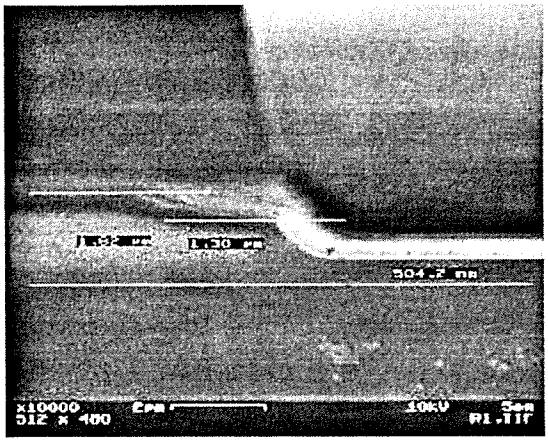
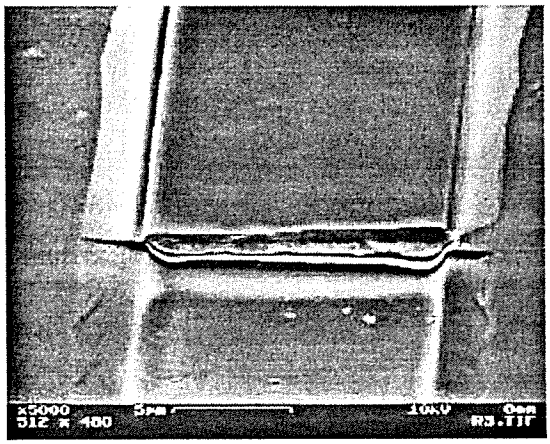


Figure 5: continued

(b.)



(c.)



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Robert K. Requa, originally from Holley, NY, received B.S. in Microelectronic Engineering from Rochester Institute of Technology in 2001. He attained co-op work experience at Eastman Kodak, Analog Devices, and Motorola SPS. He is actively looking for full time employment in the semiconductor industry as a process or device engineer.