12-2023

Investigation on Sputter Ambient Oxygen Partial Pressure and Anneal Conditions on the Operation of Indium-Tungsten-Oxide Thin-Film Transistors

Meghana Nagesha

RIT

Investigation on Sputter Ambient Oxygen Partial Pressure and Anneal Conditions on the Operation of Indium-Tungsten-Oxide Thin-Film Transistors

by

Meghana Nagesha

A Thesis Submitted in Partial Fulfilment of the Requirements for the Degree of Master of Science in Microelectronics Engineering

Department of Electrical and Microelectronics Engineering
Kate Gleason College of Engineering

Rochester Institute of Technology
Rochester, NY
December 2023

Investigation on Sputter Ambient Oxygen Partial Pressure and Anneal Conditions on the Operation of Indium-Tungsten-Oxide Thin-Film Transistors

by
Meghana Nagesha

A thesis submitted in partial fulfillment of the requirements for the degree of
Master of Science in Microelectronics Engineering

Approved by:

Dr. Karl D Hirschman Date
Thesis Advisor, Electrical and Microelectronic Engineering

Dr. Michael Jackson Date
Committee Member, Electrical and Microelectronic Engineering

Dr. Robert Pearson Date
Committee Member, Electrical and Microelectronic Engineering

ABSTRACT

Amorphous oxide semiconductors (AOS) have emerged as compelling candidates for thin film transistors due to their remarkable attributes, including high mobility(>20cm^2/Vs), low-temperature deposition, optical transparency, and electrical uniformity. However, current solutions, such as amorphous indium gallium zinc oxide (a-IGZO), exhibit sensitivity to moisture and wet etch processes, leading to suboptimal device performance and stability issues. To address these challenges, this study explores Indium Tungsten Oxide (IWO), an AOS devoid of Ga or Zn, as a potential material for fabricating high-performance and stable flexible enhancement mode thin-film transistors (TFTs).

The experiment investigates the impact of oxygen partial pressure during the film deposition, anneal temperature, time, and ambient conditions on TFT performance. Bottom-gate unpassivated TFTs were fabricated with a 30 nm IWO film on a 6" silicon wafer with 650 nm isolation and 100 nm gate dielectric. Oxygen partial pressures (P_{O2}) ranging from 2.5% to 10% were sputtered and deposited. The working metal was molybdenum for the gate electrode and Mo/Al bilayer for source/drain contacts. The unpassivated anneals were conducted across temperatures from 100°C to 300°C with varying durations and ambient conditions. Devices were tested using an HP4145 Semiconductor Parameter Analyzer connected to a probe station, with transfer characteristic measurements used to extract transconductance.

The results identified an interaction effect between oxygen partial pressure (P_{O2}), and the passivation anneal conditions on the transfer characteristics and associated parameters (i.e., V_T, g_m, SS). A 100 °C hotplate anneal for 1 hour established semiconducting behavior, with distinct differences based on P_{O2} values. All material samples experienced a transformation during a successive anneal for another hour at 200 °C, with significantly higher conductivity

(depletion-mode). Semiconducting behavior was restored during additional hotplate annealing at 250 - 275 °C, with diminished residual oxygen partial pressure dependence. A furnace anneal in O_2 at 300 °C for 30 minutes resulted in a convergence of characteristics over all oxygen partial pressure conditions, without obtaining enhancement mode operation.

ACKNOWLEDGMENTS

I would like to convey my gratitude to my advisor Prof Karl D. Hirschman. Without his constant support, encouragement, and guidance, this work would not have been possible. In addition to the technical guidance, he inspired me to become a critical thinker and independent researcher.

I would also like to thank my committee members, Dr. Robert Pearson and Dr. Michael Jackson for their valuable input and constructive feedback throughout the thesis process. A special acknowledgment goes to Team Eagle for their unwavering support, with a heartfelt thanks to Patricia Meller for her assistance in certifying me on all the tools in the RIT Cleanroom.

I would also like to acknowledge the SNL staff: Sean O'Brien, John Nash, Bruce Tollesen, Rich Battaglia and Thomas Grimsley for their tireless work, behind the scenes, in ensuring smooth operation in the cleanroom. I would like to thank the faculty members of Microelectronic Engineering program.

I am grateful to Corning Inc. for their assistance in thin film deposition, without which the completion of this thesis would not have been possible.

I extend my deepest gratitude to my parents for their unwavering support and unconditional love. Additionally, I wish to express my heartfelt appreciation to Vincent Mei for his meticulous review of numerous drafts and unwavering support throughout this journey.

TABLE OF CONTENTS

LIST OF FIGURES

CHAPTER 1: INTRODUCTION

The evolution of display technology increases the need for rigorous manufacturing and performance standards; requirements for these displays include large-area uniformity, increased mobility, compatibility with low temperatures, and transparency to visible light. The changing demands of next generation displays introduce numerous challenges, particularly in high pixel density displays and applications requiring fast switching speeds. Therefore, the demand for thin film transistors (TFTs), featuring high-mobility semiconductors, becomes crucial to enhancing current drive and minimize delay times. Thus, there is a growing significance in exploring improvement methods and investigating new material candidates for TFT fabrication. This chapter provides an overview of TFTs, delving into their brief history and operational principles.

1.1 Liquid Crystal Display

LCD (Liquid Crystal Display) is a type of flat panel display which uses liquid crystals in its primary form of operation. Prior to LCD displays, there were cathode ray tube (CRT) displays which were bulky and consumed more power. LCDs works on the principle of pixel addressing, where pixels, consisting of RBG colors, turn on and off rapidly to display a picture.

LCDs are made with either a passive matrix or an active-matrix display grid. Passive matrix LCDs have pixels arranged in a matrix consisting of rows and columns of electrodes, as shown in Figure 1.1, with two glass substrates, filled with Liquid Crystal fluid, both patterned with ITO electrodes. Pixels are formed when the rows and columns of two substrates intersect, creating a matrix. Activating a pixel typically involves sending a voltage signal to the relevant column and grounding the corresponding row to create a circuit. One drawback to this approach is that it may introduce a leakage path, which could turn on the adjacent pixel (aka

crosstalk) in the LCD matrix. Since the passive matrix has common electrodes, it requires a special matrix drive schemes to be implemented. These schemes impose significant limitations on the range of voltages that can be independently applied to individual pixels. Direct pixel addressing comes with two significant disadvantages: slow response time and inadequate voltage control [1]

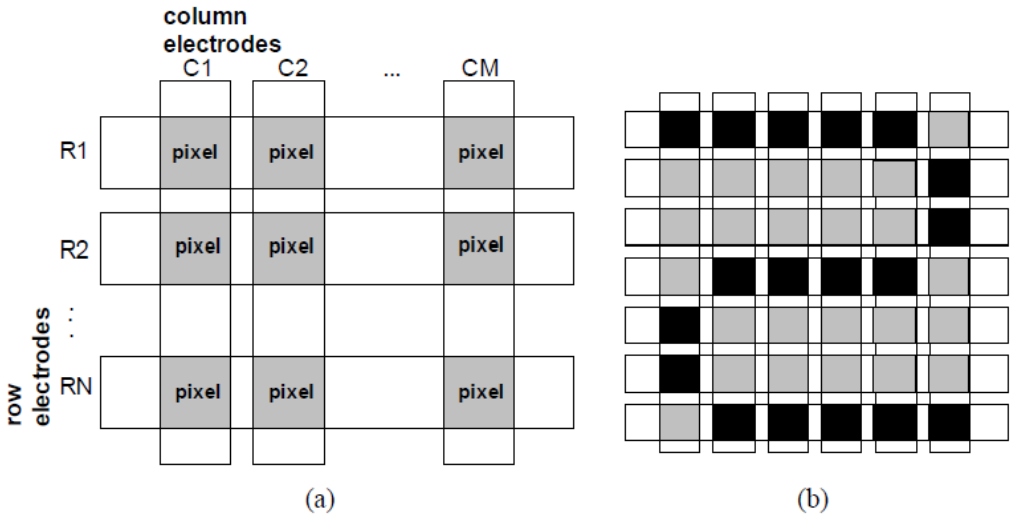

Figure 1.1 Passive matrix LCD: (a) schematic representation of the pixels made up of orthogonal rows and columns of electrodes, (b) example of a displayed numeral.

An active-matrix LCD has a device such as a transistor or diode at each pixel intersection. The active device is usually a thin film transistor (TFT) that is arranged in row and columns on a glass substrate. In an active-matrix display (as depicted in Figure 1.2), each pixel is equipped with a switch that manages the charging of its capacitor to the desired level. This charge is maintained until the next frame refresh while other pixels are being addressed. This approach effectively addresses the issue of crosstalk, which is a significant concern in passive matrix displays. In contrast to passive matrix displays, which necessitate the charging of all rows to address a single pixel, active matrix displays provide the benefit of individualized control for each pixel. This leads to a decrease in the current needed to control the brightness

of a pixel. For this reason, the current in an active-matrix display can be toggled on and off more frequently, improving the screen refresh time.

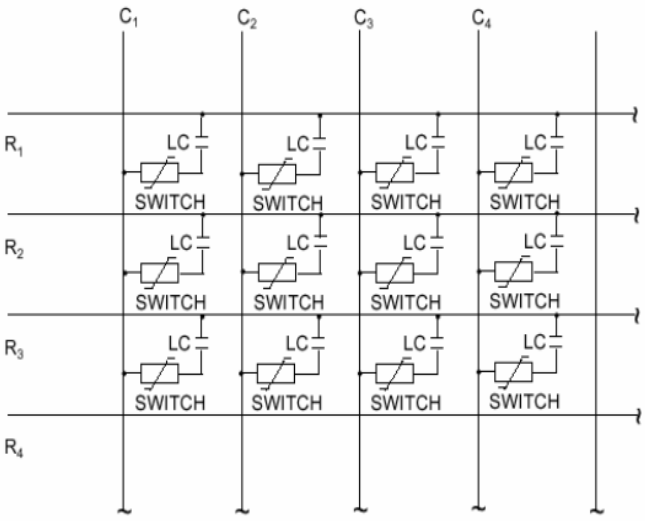

Figure 1.2: Active Matrix Addressing (Adapted from [2])

1.2 Historical overview of Thin Film Transistors

The development of Thin-Film Transistors (TFTs) has emerged as a pivotal driving force in the electronic flat panel display industry. The initial implementation attempt can be traced back to the 1940s when Bardeen and Brattain [3] introduced a thin-film field-effect device using a germanium film in 1948. However, the first active-matrix LCD (AMLCD), using CdSe (*cadmium selenide),* TFT was demonstrated in 1973[4]. Following this milestone, the introduction of TFTs utilizing amorphous silicon (a-Si) for AMLCD applications garnered substantial global attention and significantly influenced research in this field for decades to come [5,6].

1.3 Amorphous hydrogenated silicon (a-Si:H)

Polycrystalline and amorphous silicon are the two most used types of thin-film transistors in the display industry. Amorphous silicon offers the advantage of being low-

temperature compatible and can be deposited using plasma-enhanced chemical vapor deposition (PECVD) at temperatures below 350°C. a-Si:H is known to have great electrical uniformity and is a cost-effective material for TFTs. However, it is important to note that amorphous silicon TFT technology is primarily limited to n-channel devices due to its electronic properties, which do not favor the production of high-quality p-channel devices. This is attributed to the significantly lower on-current, stemming from the low mobility of holes within the active layer.

The expanding market for flexible and transparent display applications has led to increased demand for large area displays with higher resolution, lower power consumption, and lighter and faster electronic devices that are unable to be achieved with a-Si:H. To overcome the limitations of a-Si:H the research community has been actively exploring alternative materials to replace amorphous silicon (a-Si:H). Two promising candidates to address these requirements are low-temperature polycrystalline silicon (LTPS) and amorphous oxide semiconductors (AOS). The table below presents a performance comparison of these candidates with amorphous silicon (a-Si:H).

	a-Si:H	***LTPS***	***IGZO(AOS)***
Microstructure	Amorphous	Polycrystalline	Amorphous
Channel Mobility(cm^2/Vs)	~1	>100	~10
TFT Type	NMOS	CMOS	NMOS
TFT Uniformity	Good	Fair	Good
Leakage Current	Good	Fair	Excellent

Table 1: Comparison between different candidates for TFT channel materials

1.3.1 Low-temperature Polycrystalline Silicon (LTPS)

LTPS is generated by changing the properties of a-Si. Silicon molecules undergo recrystallization through laser irradiation, transforming them into a state similar to single crystal silicon. This characteristic imparts LTPS with higher electron mobility, contributing to faster switching speeds and enhanced resolution. In contrast to a-Si and Metal Oxide technology, LTPS backplanes exhibit increased off-state currents. However, this higher off-state level leads to elevated leakage current and greater power consumption. While LTPS offers advantages in resolution and mobility over a-Si:H, its fabrication is costly, thereby raising production expenses.

1.3.2 Amorphous Oxide Semiconductor Devices

AOS devices are characterized by minimal leakage current and cost-effective fabrication in comparison to LTPS. Among the AOS candidates, amorphous indium-gallium-zinc-oxide (a-IGZO) has emerged as a promising material in the display industry. The first a-IGZO document in literature was by Nomura, et al. in 2004, and since then has become the most researched AOS [7]. The performance improvement of IGZO over a-Si:H is especially evident in Fig. 1.3 where, when normalized by device width the IGZO TFT current drive is approximately 1.5 times larger than the a-Si:H TFT despite being roughly 10 times longer in channel length. This allows IGZO devices to operate at lower voltages and can result in reduced power consumption. Yet, numerous challenges linked to AOS thin-film transistors (TFTs) require addressing before gaining widespread acceptance in the flat panel display (FPD) industry. These challenges involve issues such as gate bias instability [8–10], instability under illumination stress [11], thermal instability [12], and the impact of hot carrier effects [13]. The mobility of IGZO increases with increase in the concentration of Indium and decrease with

Gallium. However, increasing Indium content and decreasing Gallium concentration also causes the problem of stability due to oxygen vacancies [14].

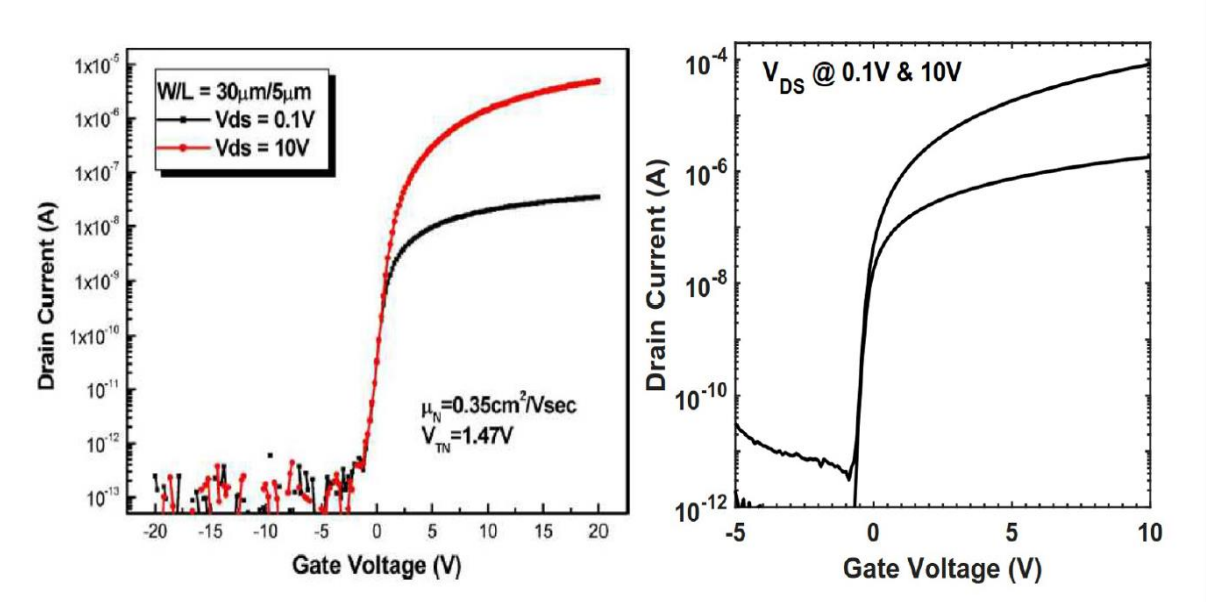

Figure 1.3: Comparison of ID-VGS transfer characteristics for a-Si:H and un-passivated IGZO TFTs with dimensions W/L = 30/5 μm and W/L = 100/48 μm, respectively [15,16]

1.3 IWO as a Candidate for Metal Oxide TFT

Transparent amorphous oxide semiconductors (TAOSs) have been gaining attention owing to their notable attributes, including high mobility, low-temperature deposition, optical transparency, and electrical uniformity. A diverse range of AOS candidates, such as InZnO, Sn-InZnO, Hf-InZnO, Si-InZnO, Zr-InZnO, and InGaO31[17], has been investigated to enhance device performance. Thin film transistors associated with Zn/Ga containing channel layers have been observed to exhibit sensitivity to moisture and wet etch processes, resulting in suboptimal performance and stability issues [18,19]. Various passivation strategies have been employed to mitigate these stability concerns [20,21].

To overcome the challenges, the exploration of amorphous oxide semiconductors devoid of Ga or Zn, such as indium tungsten oxide (IWO) is explored and investigated for

fabricating high-performance and stable flexible TFTs. In IWO, In_2O_3 showcases elevated electron mobility attributed to band conduction originating from an edge-sharing polyhedral structure [22,23]. The properties of IWO are extensively discussed in Chapter 2.

CHAPTER 2: IWO LITERATURE REVIEW

Metal oxide semiconductors based on indium oxide (InOx) have been extensively explored as potential channel materials for thin-film transistors (TFTs) due to their impressive electron mobility, attributed to their polyhedral structure with edge-sharing [14]. This enhanced electron mobility contributes to improved electrical conductivity without compromising optical transparency within the visible light spectrum. Consequently, transparent electronic devices can achieve high operational speeds [24]. One notable variant, Indium-tungsten oxide (IWO), produced by doping In_2O_3 with a minimal amount of WO_3 (<5%), has been the subject of extensive research as a channel material [25] [26].

The generation of free electrons in the n-type indium-tungsten oxide (IWO) semiconductor film is attributed to either oxygen vacancies or activated W^{6+} ions replacing In^{3+} ions at specific sites [27]. In accordance with the complex theory, in IWO, W^{6+} is expected to contribute one carrier when it forms an association with one interstitial O^{2-}, as illustrated in Equation (2.1).

$$In_{In} + WO_3 \rightarrow W_{\dot{I}n}O_i'' + \frac{1}{2}In_2O_3 + \frac{1}{2}O_2 + e' \qquad (2.1)$$

Here, $O_{i''}$ is interstitial oxygen with negative charge given by the ($'$) and A_B represents ion A substituting ion B with positive charge given by the (.). Consequently, fewer electrical neutral complexes and impurities are formed, leading to reduced neutral complexes and weakened neutral complex scattering. This effect leads to an increase in mobility as the O_2/Ar ratio rises [28]. However, as the oxygen concentration rises, oxygen vacancies can be filled and the substituted W^{6+} ions can be deactivated by forming W-O complexes [29]. Hence, optimizing the O_2/Ar ratio is crucial in producing a suitable film for the TFT channel.

Aikawa, et al. reported the first ever a-IWO TFT, demonstrating a high-performance TFT with an IWO channel deposited through DC magnetron sputtering. The TFTs demonstrated encouraging electrical characteristics, as illustrated in Figure 2.1(a) [30]. Figure 2.1(b) highlights distinct hysteresis in the transfer curves, indicating the existence of interface traps. Furthermore, the negative threshold voltage (V_{th}) attributes to a relatively high number of carriers.

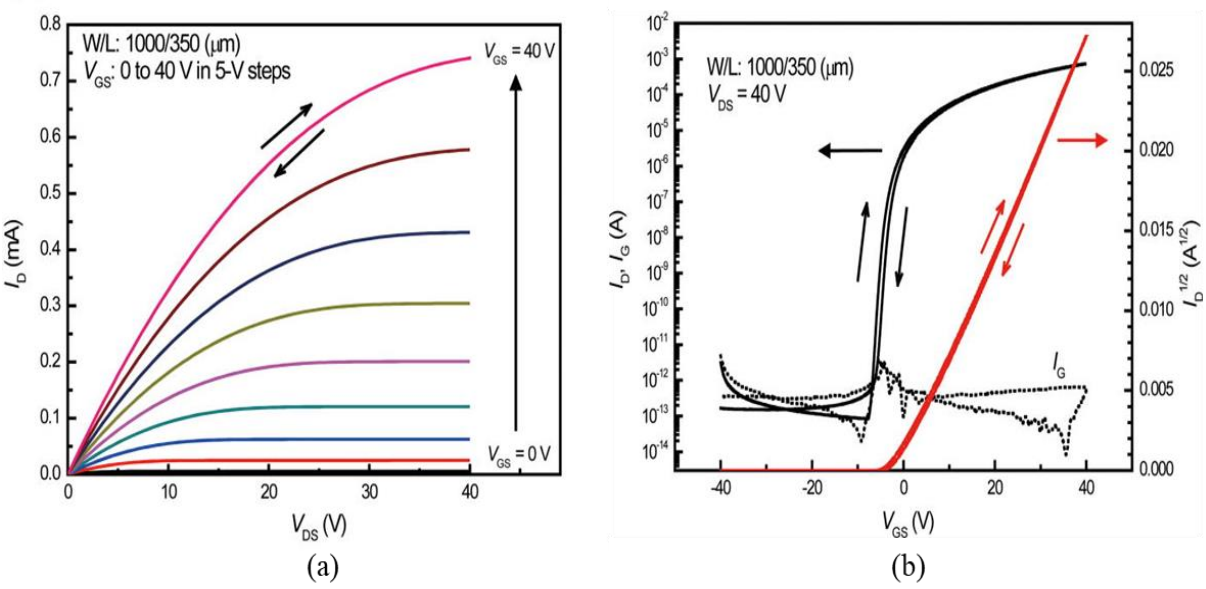

Figure 2.1 I_D-V_{DS} characterises post anneal (a) output (b) transfer characteristics.

The conductivity of oxide semiconductors is predominantly influenced by the presence of oxygen vacancies, which serve as the primary source of free electrons [31]. Controlling the oxygen vacancy concentration during the annealing process is instrumental in regulating the film's electrical properties. Notably, as illustrated by Liu, et al.'s research [27], the electrical performance of a-IWO TFTs is greatly affected by varying oxygen pressure (P_{O2}). Specifically, an increase in oxygen content within the device leads to a higher voltage threshold (ΔV_t). In the study, three TFTs were fabricated, each with different oxygen partial pressures (P_{O2}) set at

7%, 10%, and 13%, shown in Figure 2.2. Subsequently, all devices underwent a passivation annealing process at 100°C for 30 minutes in an oxygen ambient.

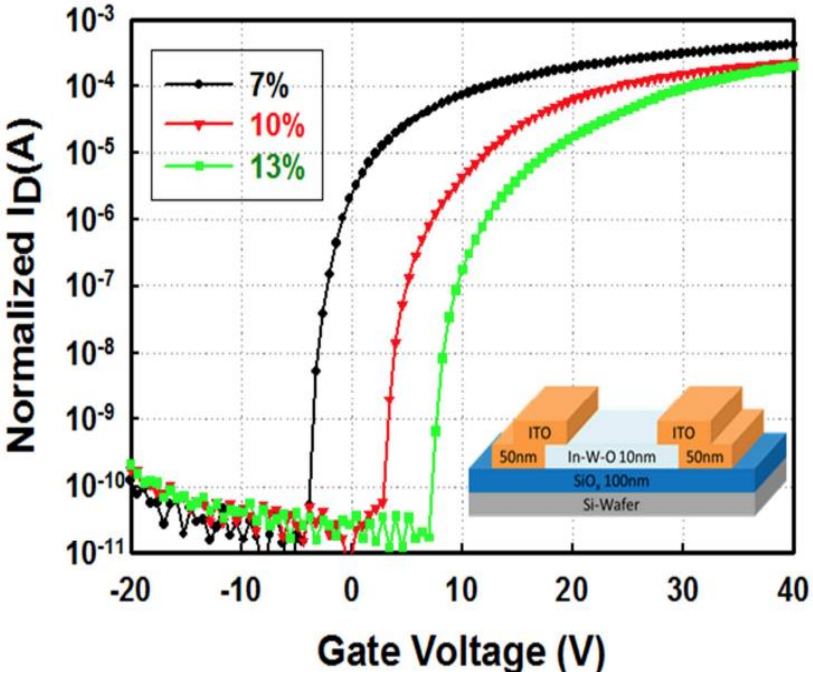

Figure 2.2: A comparison of I_D-V_{GS} characteristics for transistors of P_{O2} 7%,10% and 13%. [33]

The operational parameters, such as the V_{th}, subthreshold swing, and hysteresis, displayed a notable increase as the P_{O2} increased. Conversely, the mobility of the device exhibited a decline with the increase of P_{O2}. This observation highlights the necessity of optimizing the fabrication process for enhancement-mode TFTs to attain higher channel mobility and sharper subthreshold performance.

P_{O_2}	V_{th} (V)	*S.S* (V/ decade)	Mobility (cm^2/ V S)	Hysteresis (V)
7%	-3.4	0.39	36.7	0.06
10%	4.2	0.42	26.2	0.11
13%	8.4	0.55	22.4	0.29

Table 2: Comparison of various device parameters of IWO TFTs

In the IWO literature, it has been observed that employing low-temperature annealing processes have resulted in the development of enhancement mode devices [31],[32]. Menzel, et al [31], demonstrated that for IWO films containing a combination of c-In_2O_3 and a-IWO_x, annealing at temperatures below 300°C maintained an amorphous state, particularly with P_{O2} levels ranging between 5% and 10%, as shown in Figure 2.3. Beyond this temperature range, a tendency for crystallization was noted.

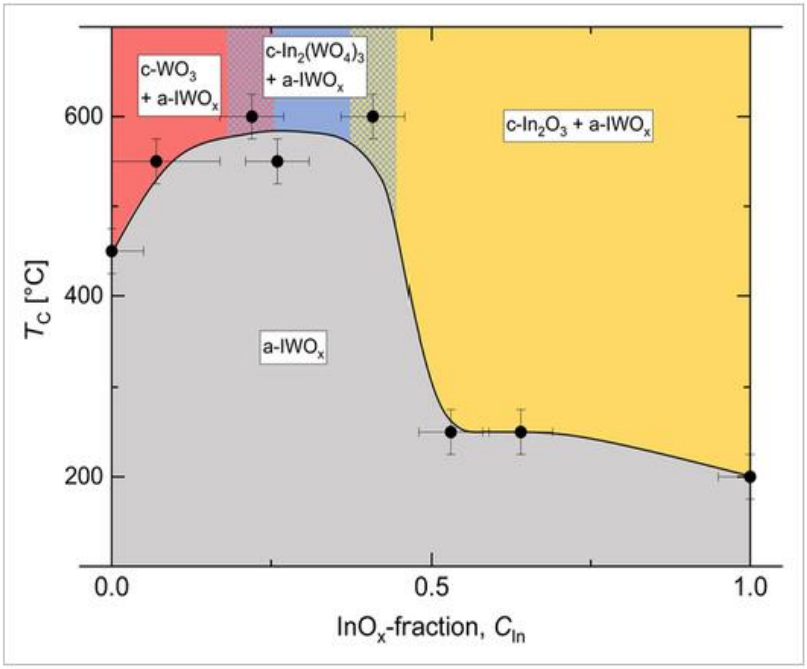

Figure 2.3: Crystallization diagram of thin-film mixtures of tungsten oxide and indium oxide, based on grazing incidence X-ray diffraction measurements (Adapted from [32])

Qu, et al., demonstrated that annealing ambient has an influence on the device performance by using N_2 and O_2 as anneal ambient [33]. Figure 2.4 illustrates that devices subjected to O_2 annealing outperformed those annealed in N_2 or air ambient. This improved performance is attributed to the presence of O_2 in the annealing ambient, which can diffuse into the amorphous IWO (a-IWO) channel layers, filling excess oxygen vacancies. The observed hysteresis in device behaviour is linked to electron capture in the channel layers, interactions

at the interface between the gate insulator and the channel [34], and the trapping of charges by water adsorbed on the semiconductor surface [35].

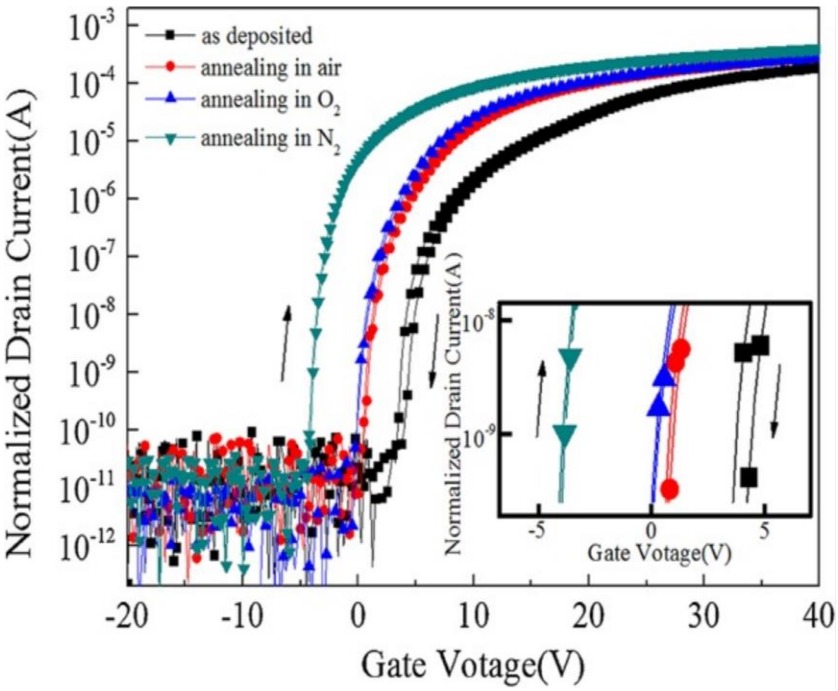

Figure 2.4: Transfer characteristic curves of a-IWO-TFTs under different annealing ambient conditions (Adapted from [33]).

The goal of this investigation was to develop an understanding of the dependence of IWO semiconductor properties and TFT operation on the initial oxygen partial pressure (P_{O2}) of the film and anneal conditions. The following criteria defines device operation of a viable candidate for advanced TFT applications.

1) Higher mobility than IGZO.
2) Near enhancement mode operation of the devices.
3) Operation consistent with low level of defect states.

CHAPTER 3: DEVICE FABRICATION AND CHARACTERISTICS

This section details the fabrication process of bottom-gate TFTs utilizing IWO thin film at the RIT Semiconductor Nanofabrication Laboratory. The chapter provides a comprehensive explanation of the extraction and calculation of operational parameters, including threshold voltage and mobility. The fabrication process and characterization methods remains consistent for both Phase I and Phase II of this thesis.

3.1 TFT Device Fabrication

The bottom gate thin film devices using IWO thin film were fabricated at RIT Semiconductor Nanofabrication Laboratory (SNL). Devices were fabricated on 6" silicon wafers with bottom gate staggered configuration on a thermally grown SiO_2 isolation layer, approximately 650nm thick. A 150nm Molybdenum gate electrode is sputtered and patterned using a CVC601 sputter tool with argon gas flow of 20sccm and pressure of 3.3mTorr. The gate electrode is patterned and then etched using a Transene Type A Aluminum etchant at room temperature. It is followed by the gate dielectric deposition of 100nm using the plasma-enhanced chemical vapor deposition (PECVD) method with TEOS precursor. The SiO_2 is densified for 2 hours at 600^{o}C in the furnace with nitrogen ambient. Following that, a 30nm IWO Film is sputtered using an AJA Sputter Tool at Corning Inc.; the sputtering system has a chamber pressure of 5mTorr, power of 200W and a combined gas flow of 40sccm comprised of Argon and Oxygen. The target composition used is 98% In_2O_3 & and 2% W. The IWO MESA is patterned and etched using a dilute HCl mixture. The source drain electrodes are defined using lift off lithography (Futurrex NR9g-1500PY-negative photoresist), with a sputtered Mo/Al bilayer (50nm Mo, 75nm Al). The wafers were divided into four quarters, each subjected to a passivation anneal process with different time, temperature, and ambient.

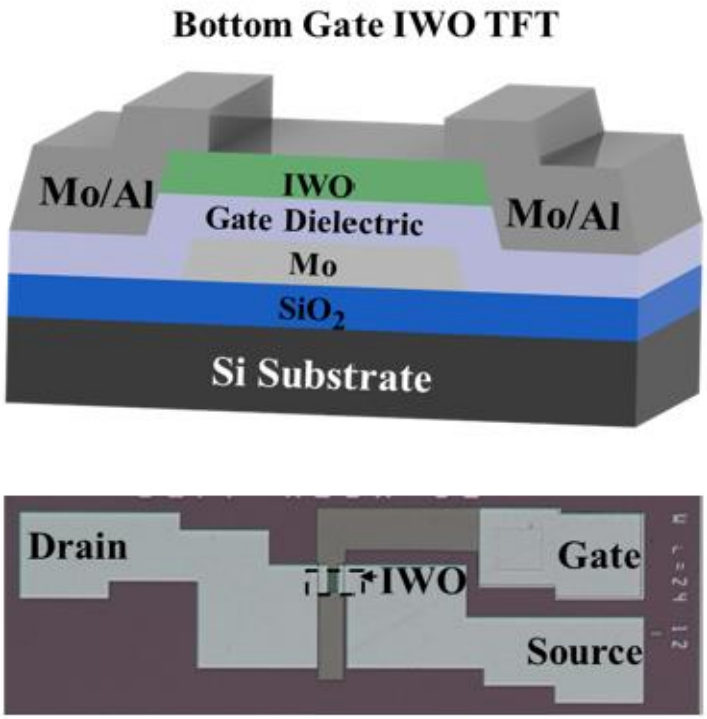

Figure 3.1 (a) Cross-section schematics of bottom-gate IWO TFT (b) Fabricated TFT

3.2 Electrical Characterization

The output transfer characteristics of the transistor were measured using the HP4145 Semiconductor Parameter Analyzer connected to a probe station. The I_D-V_{GS} characteristics were used to extract operational parameters such as the threshold voltage (V_{th}) and mobility (μ). V_{th} was determined using the intercept of the extrapolated (I_D-V_{GS}) linear relationship. The mobility of the device was calculated from the maximum transconductance using the following equation:

$$\mu = \frac{g_m L}{C_{ox} V_{DS} W} \qquad \text{Eq (3.1)}$$

where L is the channel width, W is the channel width, g_m is the transconductance, and C_{ox} is the capacitance per unit area. For the mobility calculation the C_{ox} value was taken as 3.45 x 10^{-8}F/cm^2 and V_{DS} was taken as 0.1V.

3.3 Mobility extraction

The mobility of the fabricated devices were extracted at a consistent subthreshold current of 100pA.

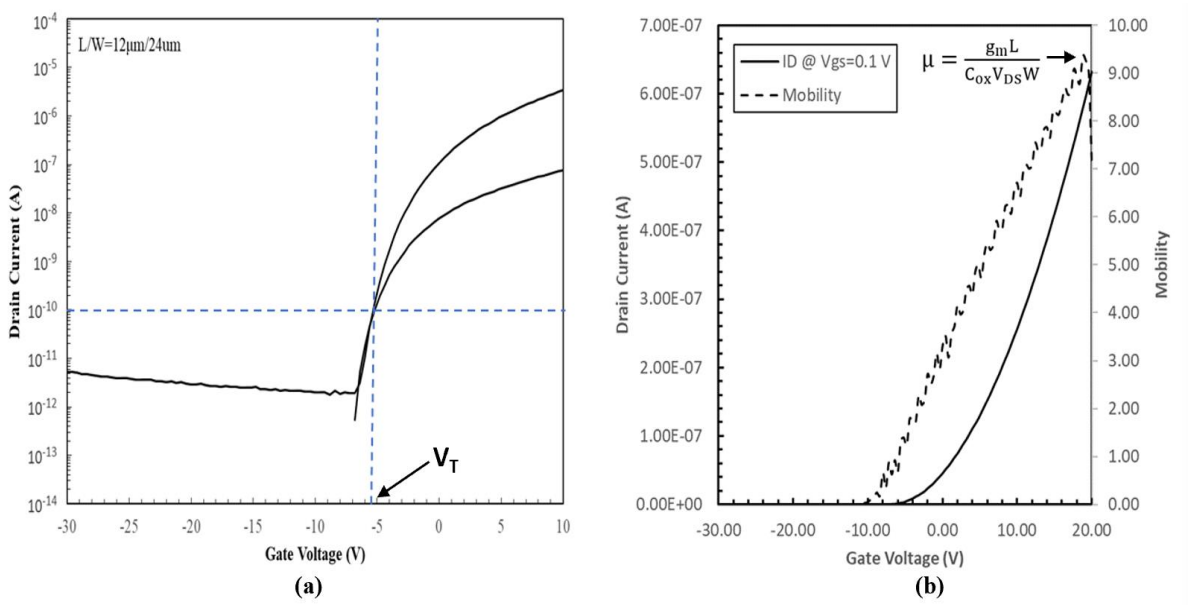

Figure 3.2(a) V_T extraction at 100pA (b) Concave-up transfer characterises at V_{GS} of 0.1V

Figure 3.2(b) illustrates the concave-up transfer characteristics of the device, indicating the inability to extract an extrapolated V_T in the conducted experiment. In comparing different parameters within this experiment, peak transconductance (g_m) and maximum gate voltage are considered due to the presence of band tail states (interface traps).

CHAPTER 4: PRELIMINARY RESULTS (PHASE I)

This section focuses on the initial research conducted on Indium Tungsten Oxide (IWO) thin-film transistors (TFT) with a bottom-gate configuration without passivation material at the back channel subsequently subjected to an annealing processes. The IWO thin-film transistors were fabricated with varying oxygen partial pressures (P_{O2}) in the sputter ambient, specifically at 2.5% and 5%. The operational parameters, such as the threshold voltage (V_{th}) and mobility, were extracted and analyzed. The following section provides a comparative analysis and discussion of the results obtained from these devices under different annealing conditions.

4.3 Anneal Conditions

4.3.1 Anneal Time

To explore the effect that anneal duration has on device performance and I_D-V_G characteristics, the IWO TFTs were subjected to different anneal durations while maintaining the P_{O2} in the IWO film and the anneal temperature constant. Two quarter samples with IWO P_{O2} of 5%, underwent a hot plate anneal in atmosphere ambient at 100˚C, for 30 minutes and 60 minutes respectively. Figure 4.1 shown below compares the data from the IWO TFT, before and after annealing, for these scenarios. There is a significant right shift in the device annealed for 60 minutes, with a reduced separation between high drain and low drain bias; this is presumably due to a decrease in the oxygen vacancy donors that are prevalent in oxide semiconductors. It is worth noting that there appears to be negligible difference in the mobility of the devices subjected to a 30-minute anneal (8.52 cm^2/Vs) compared to those subjected to an hour-long annealing process (8.77 cm^2/Vs). This indicates that the extended annealing period did not negatively impact the mobility. Subsequently, higher temperatures were explored with a minimum of an hour long anneal with the expectation of further right shift in the device operation.

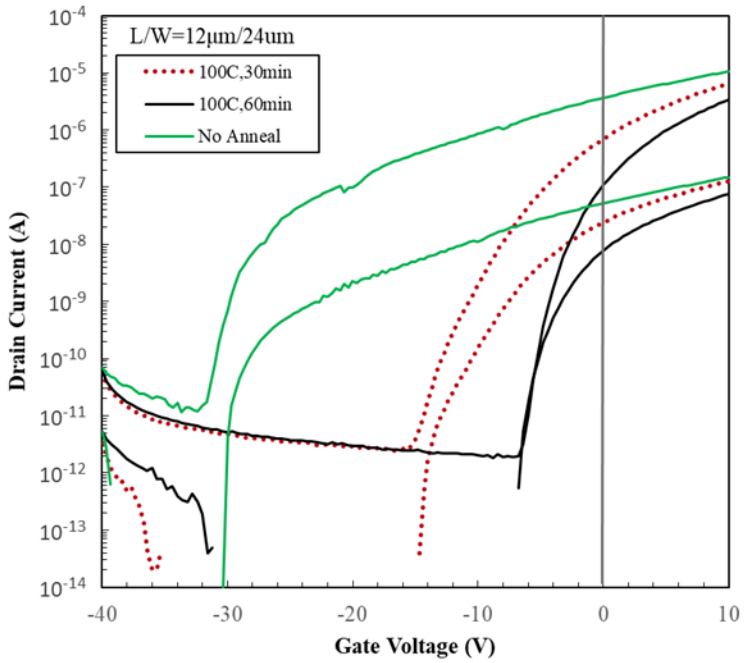

Figure 4.1: The 60min hot plate anneal at 100˚C for P_{O2} 5% shows a significant right shift with channel mobility of 8.77 cm²/Vs.

4.3.2 Anneal Temperature

To explore the impact of temperature, the IWO TFTs were subjected to different anneal temperatures while keeping the oxygen partial pressure and anneal time constant. The first two anneals for 5% P_{O2} were carried out at 100˚C and 200˚C for one hour in ambient air environment using a hot plate. The device subjected to a 200˚C anneal exhibits significant degradation compared to the 100˚C anneal device. This is seen by noticeable shifts, separation, and distortion. This result was unexpected for this treatment, suggesting the involvement of another mechanism, such as oxygen trap states. [1]

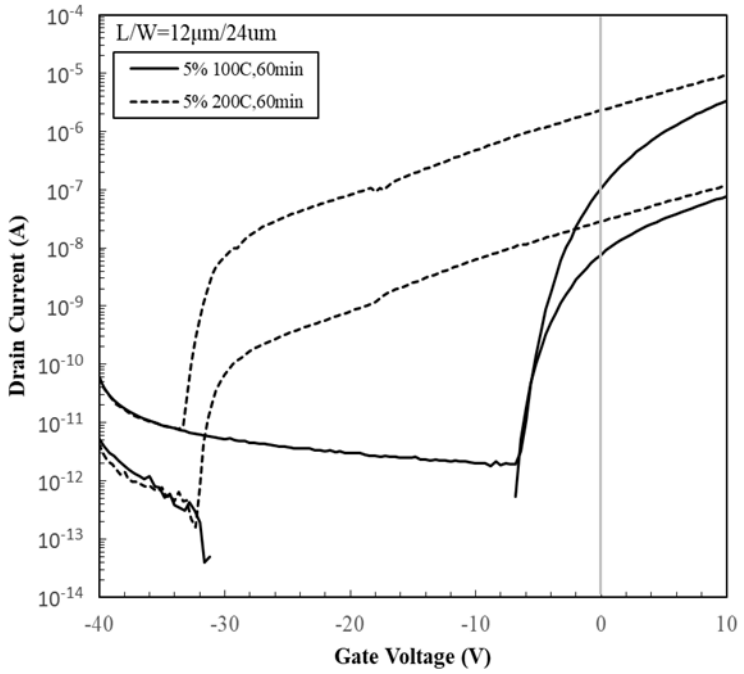

Figure 4.2: Significant degradation of I_D-V_{GS} characteristics is observed for P_{O2} =5% after an hour anneal at 200˚C on a hotplate.

4.4 Influence of Oxygen Partial Pressure on The Thin Film

The next stage of the experimental section focuses on the influence of P_{O2} on the semiconducting properties of the IWO sputtered film of the TFT.

4.4.1 Treatment 1- 200˚C hot plate atmosphere ambient anneal for one hour (60mins)

Figure 4.3 provides a comparative analysis of the I_D-V_{GS} characteristics for two different oxygen partial pressures of the IWO films of 2.5% and 5, after annealing at 200°C for one hour on a hotplate. It was seen that the IWO film with a 5% P_{O2} exhibits a more significant distinction between the low drain and high drain characteristics. The devices were seen to turn off beyond -20V, which does not contribute to good device characteristics. The devices were seen to be shallow and in depletion mode.

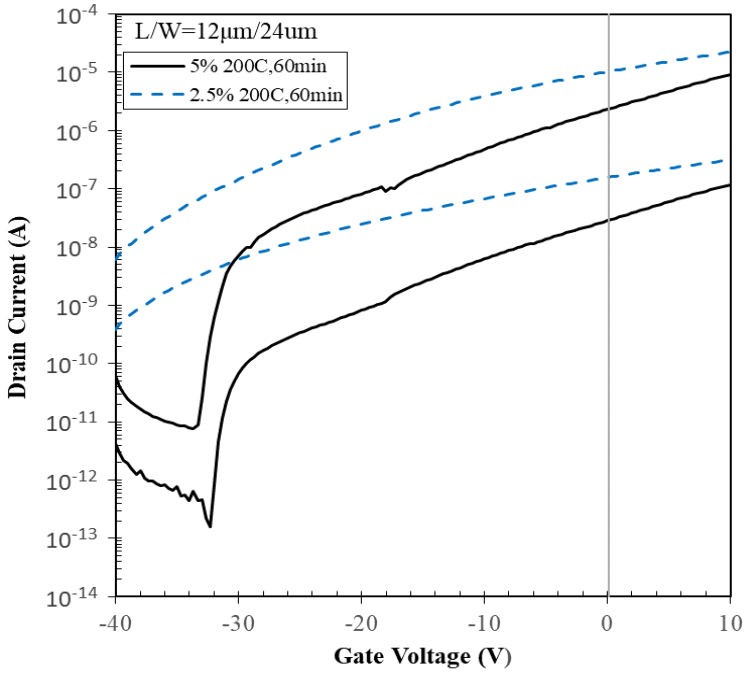

Figure 4.3 P_{O2} 2.5% and 5%, with a 200C anneal for an hour show distortion, degradation, and depletion mode devices.

4.4.2 Treatment 2: 250˚C hot plate atmosphere ambient anneal for one hour (60mins)

Figure 4.4 compares the I_D-V_{GS} characteristics for the TFT Devices of 2.5% and 5% P_{O2} after annealing at 250°C for one hour on a hot plate. It is seen that the film with 2.5% P_{O2} has better device turn-on characteristic and a lower separation between the high drain I_{D1} and low drain I_{D2} current. The V_{th} is seen to be shifted right for the device with 2.5% P_{O2} when compared to the device with 5% P_{O2}. The mobility of the transistor with 2.5% P_{O2} is 9.36

cm²/Vs, while that of the 5% P_{O2} is 8.71 cm²/Vs. It is observed that the mobility of the device declines along with the subthreshold slope, as the P_{O2} increases.

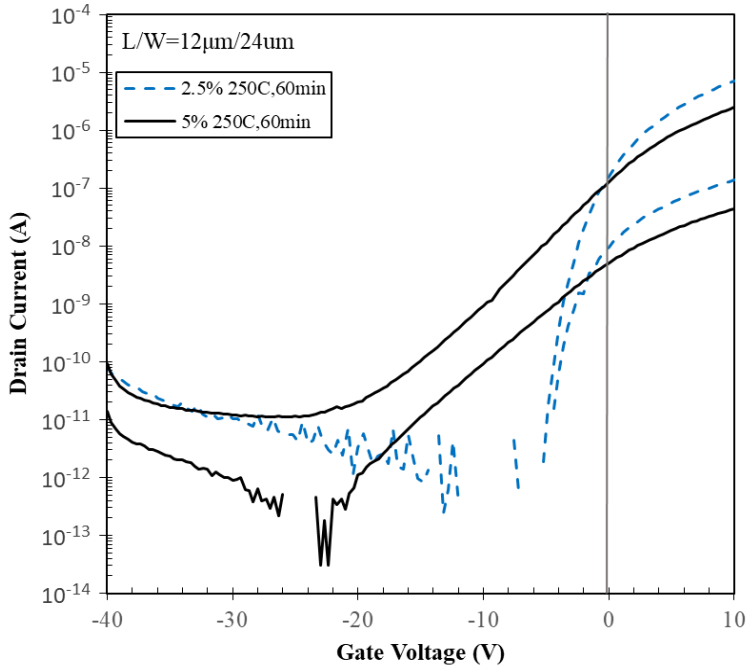

Figure 4.4: A comparison of I_D-V_{GS} characteristics for transistors of P_{O2} 2.5% and 5%, with a 250C,60 min anneal showing that the mobility of the device declines along with the subthreshold slope, as the P_{O2} increases.

In Figure 4.5, similarities between the 2.5% P_{O2} quarter annealed at 250˚C for 60 minutes and the 5% P_{O2} quarter annealed at 100˚C for 60 minutes are highlighted. The mobility of the 2.5% P_{O2} at 250˚C anneal is 9.36 cm²/Vs, and that of 5% P_{O2} at 100˚C anneal is 8.77 cm²/Vs. These similar mobility values indicate comparable material conditions [Table III]. Despite the initial hypothesis, higher temperatures did not yield the expected improvement of the right-shift in the transfer characteristics.

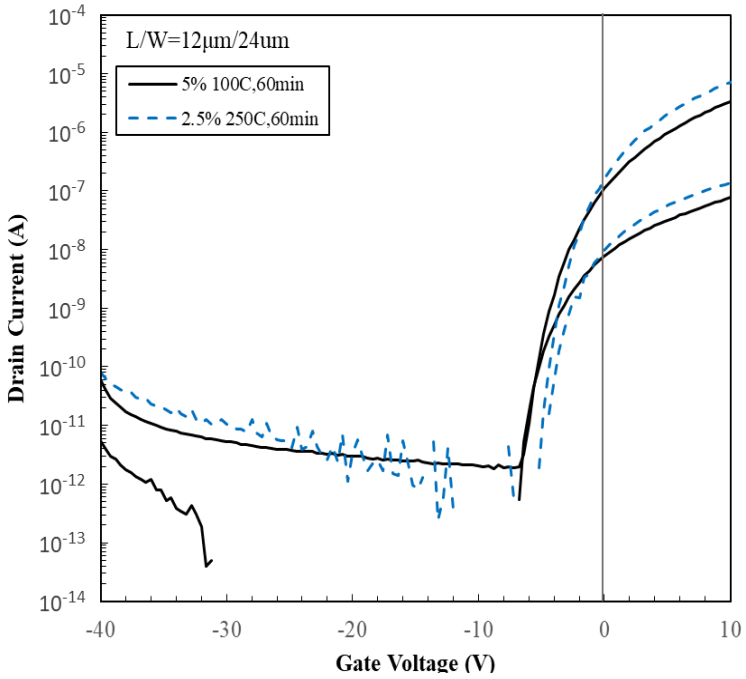

Figure 4.5: Similarity in device operation of P_{O2} 2.5% and 5%, with a 250C,1hr anneal and 100C,1hr anneal respectively.

4.3.2 Treatment 3: 300˚C furnace anneal for 30 minutes in oxygen.

In the subsequent experimental phase, devices with P_{O2} levels of 2.5% and 5% underwent annealing in an oxygen furnace ambient at 300°C for a duration of 30 minutes. As illustrated in Figure 4.6, both devices are observed to be operating in depletion mode. Following the furnace annealing process, both devices demonstrated comparable performance, indicating that the annealing process dominated the variations in oxygen partial pressure of these devices, however it is not a desirable transfer characteristics. The presence of numerous

trap states at the back channel or gate oxide interface resulted in a shallow subthreshold slope and significant separation. Therefore, it can be concluded that the furnace annealing performed in an oxygen environment did not have a positive impact on the overall device performance.

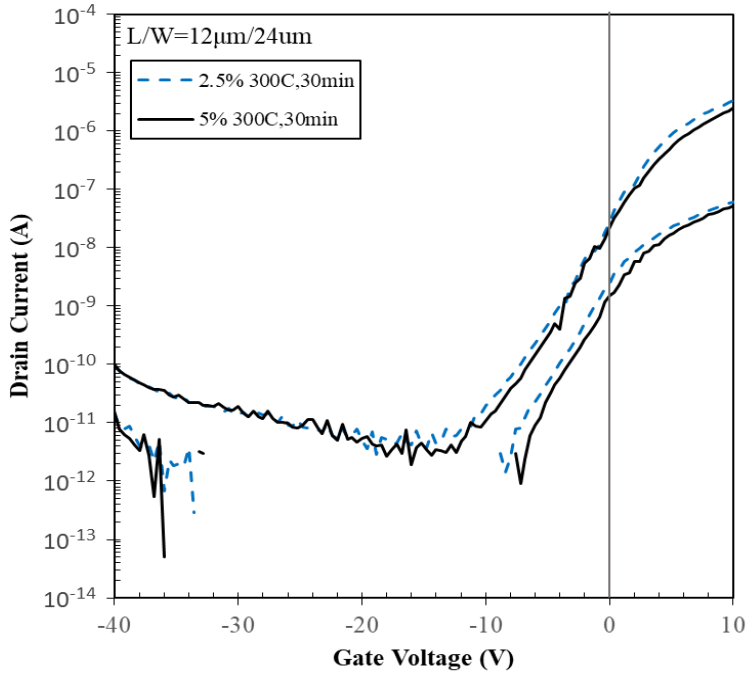

Figure 4.6: The furnace anneal in O_2 ambient overrode the variations in oxygen partial pressures of the devices.

4.4 Summary of Preliminary Result

Among the various conditions tested, the most promising device performance was observed in the IWO TFTs that underwent annealing at 100°C for one hour with a P_{O2} of 5%, and at 250°C for one hour with a P_{O2} of 2.5%. These devices transitioned towards an enhancement mode of operation with mobility approaching 10cm^2/Vs (Figure 4.5 and Table 3).

P_{O2}	Temperature, Time	Mobility (cm²/Vs)
5%	100˚C, 30 min	8.52
5%	100˚C, 60 min	8.77
5%	250˚C, 60 min	8.71
2.5%	250˚C, 60min	9.36

Table 3: Mobility values for notable PO_2 2.5% and 5% at 100˚C and 250˚C hot plate anneals.

Interestingly, when subjected to furnace annealing in an oxygen ambient at 300°C for 30 minutes, devices with P_{O2} values of 2.5% and 5% exhibited similar performance, indicating that the furnace annealing process has a dominant effect, overriding the initial influence of P_{O2}. Furthermore, it was noted that furnace annealing had a detrimental impact on both device mobility and operation; thus, the strategy of higher temperature anneals for P_{O2} of 5% did not support the improvement in the device passivation.

Although the process flow for the device fabrication shares similarities with that of Menzel, et al.[31], there is a significant difference in the device operations, potentially attributed to the thickness of the IWO film. In summary these results indicate that lower annealing temperatures are advantageous when a higher P_{O2} is employed, and conversely, higher annealing temperatures are more beneficial for lower P_{O2}. Devices with P_{O2} of 5% that were subjected to a 200˚C hotplate for an hour exhibit an interesting anomaly, where the devices were seen to exhibit degradation and were operating in depletion mode. The TFTs with a P_{O2} of 5% at higher annealing temperatures exhibited enhanced conductivity, a left-shifted behaviour, and more conducting characteristics. This observation led to the hypothesis that increasing the oxygen partial pressure in the IWO film composition could reduce conductivity and right-shift the I_D-V_G transfer characteristics, ultimately leading the device into an improved semiconducting state.

Phase I yielded promising results, demonstrating that an increase in P_{O2} in the IWO films leads to improved enhancement mode operation. This development prompted an investigation into higher P_{O2} concentrations; phase II of this research will concentrate on investigating the impact of annealing conditions on the oxygen partial pressure in the IWO films, expanding the range of oxygen partial pressure from 5% to 10%.

CHAPTER 5: PHASE II RESULTS

The goal of this investigation was to further understand the influence of the factors that lead to enhancement mode characteristics in the TFT with good mobility and optimal current drive. The study systematically examined the impact of varying P_{O2} and various annealing temperatures on the electrical characteristics of TFTs. The devices were fabricated with varying ***P_{O2} from 5% to 10%*** in the sputter ambient, with an emphasis on P_{O2} values of 5% and 10% representing lower and upper limits. The primary objective was to achieve an enhancement mode operation in device characteristics without compromising current levels, and the observed trends suggest that this objective may not be fully achieved.

5.1 Heat Treatment #1: 100˚C, 1hour hotplate anneal in air ambient

The initial annealing process was set at 100°C for one hour, guided by the Phase I results that showcased optimal device characteristics for P_{O2} 5% under these conditions. Figure 5.1(a) presents a comparative analysis of the IWO TFTs for P_{O2} 5%, 8%, and 10% subjected to a one-hour anneal at 100°C on a hotplate in an air ambient. The devices were seen to be operating in enhancement mode; there was a significant right shift in the devices with the increase in P_{O2}, with the P_{O2} 10% having a V_{th} around 4V. However, the higher P_{O2} resulted in a compromise in current levels.

Given the enhancement mode operation for P_{O2} 5% and 10%, a one-hour anneal at 100°C was extended to the P_{O2} range of 6-9%. Figure 5.1(b) illustrates the data for IWO TFTs with P_{O2} ranging from 5% to 10% during this annealing process on a hotplate in an air ambient. A noticeable right shift trend is observed as the P_{O2} increases. While the device with P_{O2} at 5% exhibits higher current levels and lower V_{th}; a progression in P_{O2} leads to an increase in V_{th}, accompanied by a compromise in current levels.

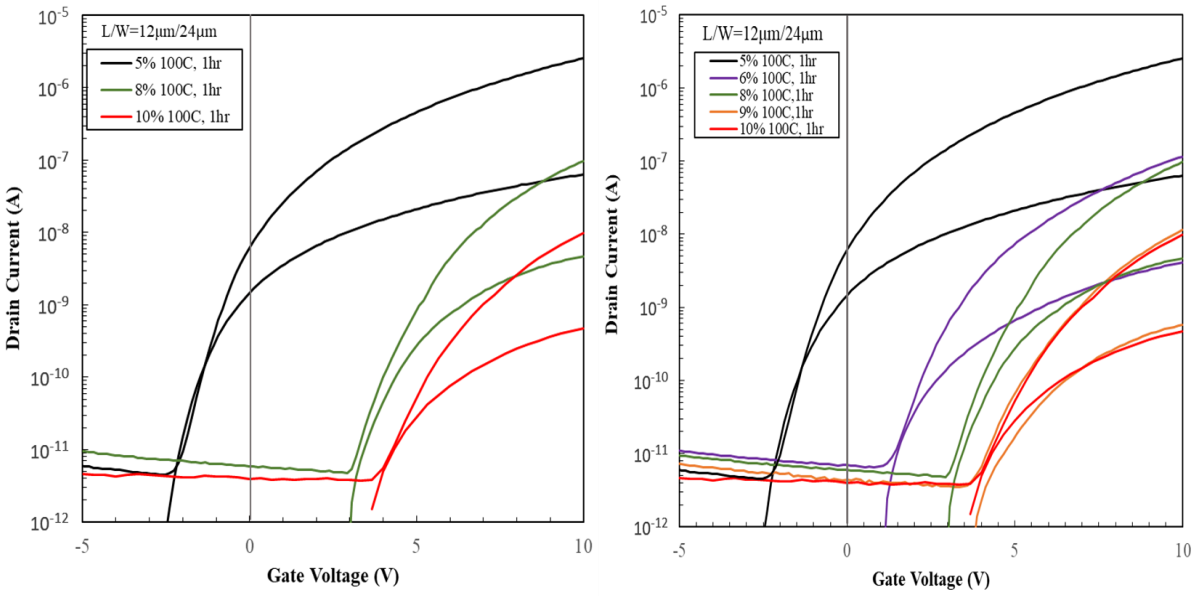

Figure 5.1: I_D-V_{GS} characterises(a) P_{O2} 8% acting as a midpoint between P_{O2} 5% and 10% (b) Significant right shift trend with increase in P_{O2} with reduced current levels when annealed at 100˚C, 1hour.

Figure 5.2(a) illustrates a comparison between devices annealed at 100°C for one hour at P_{O2} 5%, considering both Phase I and Phase II. Phase I device exhibits higher current drive with better mobility (8.77 cm²/Vs) compared to Phase II (7.47 cm²/Vs). Figure 5.2(b) illustrates the variation observed in the wafer with a P_{O2} of 5%. Notably, sample 5 of P_{O2} 5% closely resembles P_{O2} 6% after the 100°C anneal for an hour, indicating a non-uniformity in the film. In 5% P_{O2} device, it is observed that the same sample exhibits a significant difference in current drive by an order of magnitude. A complex mechanism appears to be at play, leading to a dramatic change in device characteristics. The observed change is more stable at higher P_{O2} levels, suggesting a potential connection to changes in film composition during the sputter process. Despite the IWO film deposition done in the same way under same sputter conditions, a marked performance difference is evident between the two phases.

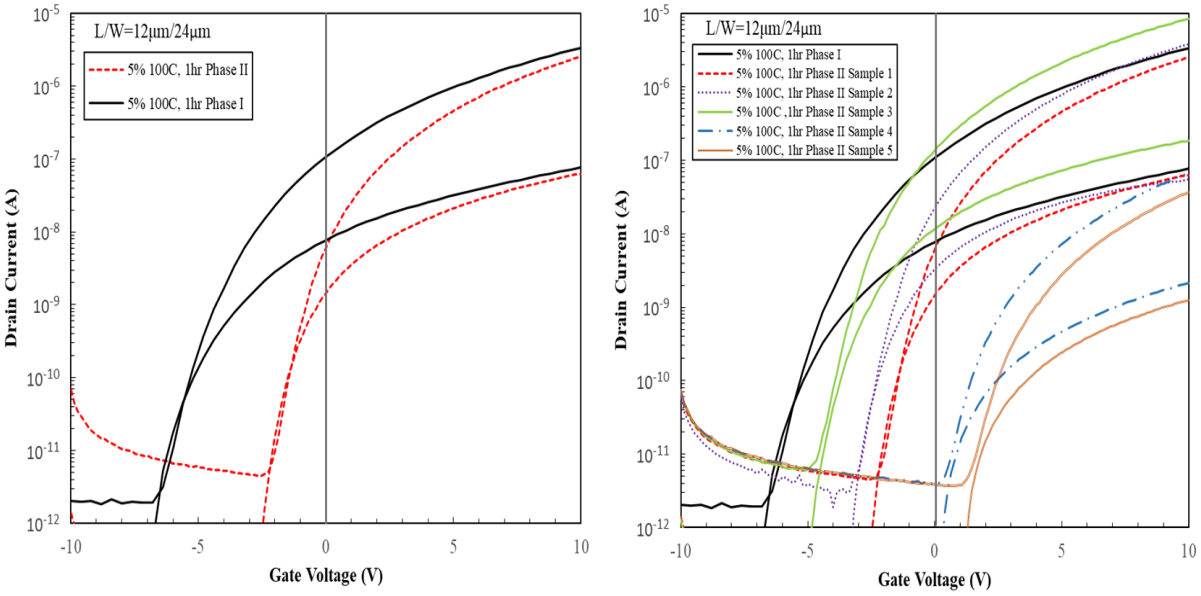

Figure 5.2 Comparison of I_D-V_{GS} characteristics at 5% P_{O2} (a) Phase I and Phase II (b) Non-uniformity among Phase II samples at 5% P_{O2}.

5.2. Heat Treatment #2: 200˚C, 1hour hotplate anneal in air ambient

During the 200°C annealing for one hour in Phase I, the I_D-V_{GS} curve displayed a significant left shift (approximately 30V) and pronounced distortion. Consequently, the annealing treatment was repeated to verify its stability for P_{O2} at 5% and 10%. The results indicate a similarity between the outcomes of P_{O2} at 5% in both Phase I and Phase II as shown in Figure 5.3(a). The device subjected to a 200˚C anneal exhibits significant degradation compared to the 100˚C anneal device. This degradation is evident through noticeable shifts, separation, and distortion, indicating the presence of oxygen trap states. A 200°C one-hour anneal was also conducted for the device with P_{O2} at 10%. Figure 5.3(b) compares the anneals for P_{O2} 5% and 10%, revealing that both devices are in depletion mode and left shifted. Following the annealing process, both devices demonstrated comparable performance, indicating that the annealing process dominated over the variations in oxygen partial pressure of these devices. The resulting transfer characteristics is not desirable, as both devices were observed to turn off beyond -30V, contributing to suboptimal device characteristics.

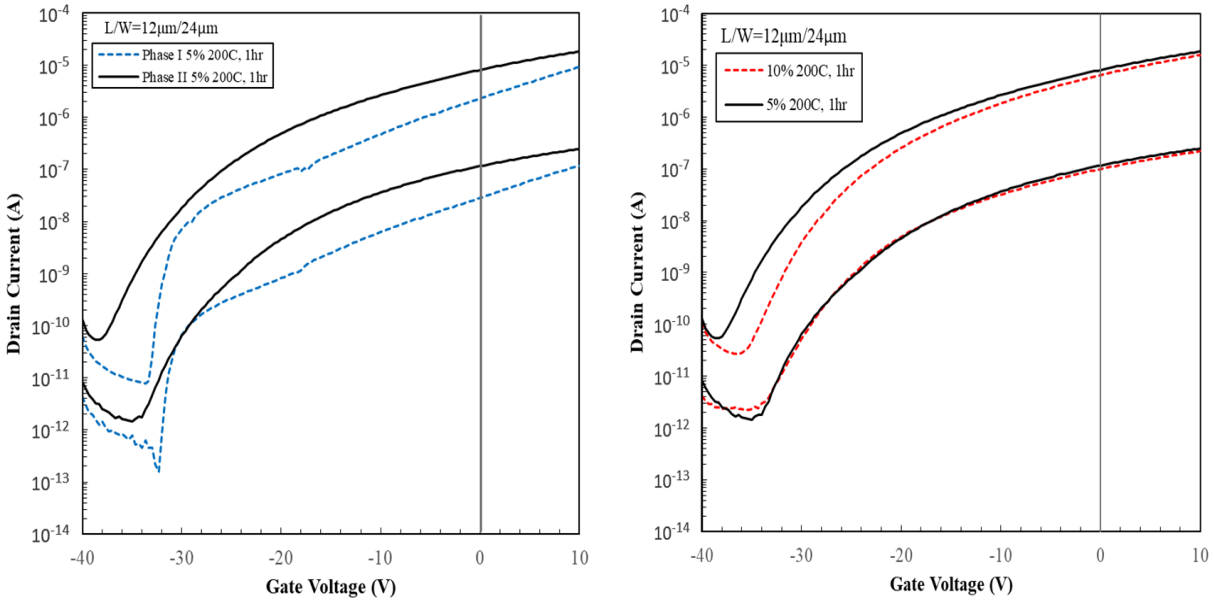

Figure 5.3: I_D-V_{GS} characterises at 200˚C, 1 hour anneal (a) Depletion mode operation of TFTs in both Phase I and Phase II, P_{O2} 5%. (b) Negligible effect of initial P_{O2} on the device performance after annealing.

5.3 Heat Treatment #3: 250˚C hotplate anneal in air ambient

In the subsequent sequential annealing, devices with P_{O2} levels of 5% and 10% underwent annealing at 250˚C for different durations of 1hr and 2hr for an hour on the hotplate in air ambient.

a) Effect of time

A series of sequential anneals at 250°C were conducted and tested after each hour (2 times) to evaluate the performance of the devices. This is based on the optimal outcome observed in Phase I for P_{O2} 2.5% at, 250˚C anneal for an hour. Figure 5.4(a) provides a comparative analysis of the 250°C anneals for P_{O2} at 5%. In the initial 250°C, 1-hour anneal, the V_{th} is around -10V; following the second anneal, V_{th} further right-shifts to approximately -6V.

Figure 5.4(b) illustrates a comparison of the 250°C anneals for P_{O2} at 10%. A device behavior similar to that of P_{O2} 5% at 250˚C anneal is observed. In the initial 250°C, 1-hour anneal, the V_{th} is approximately -11V; with the second anneal, V_{th} right-shifts to about -6V.

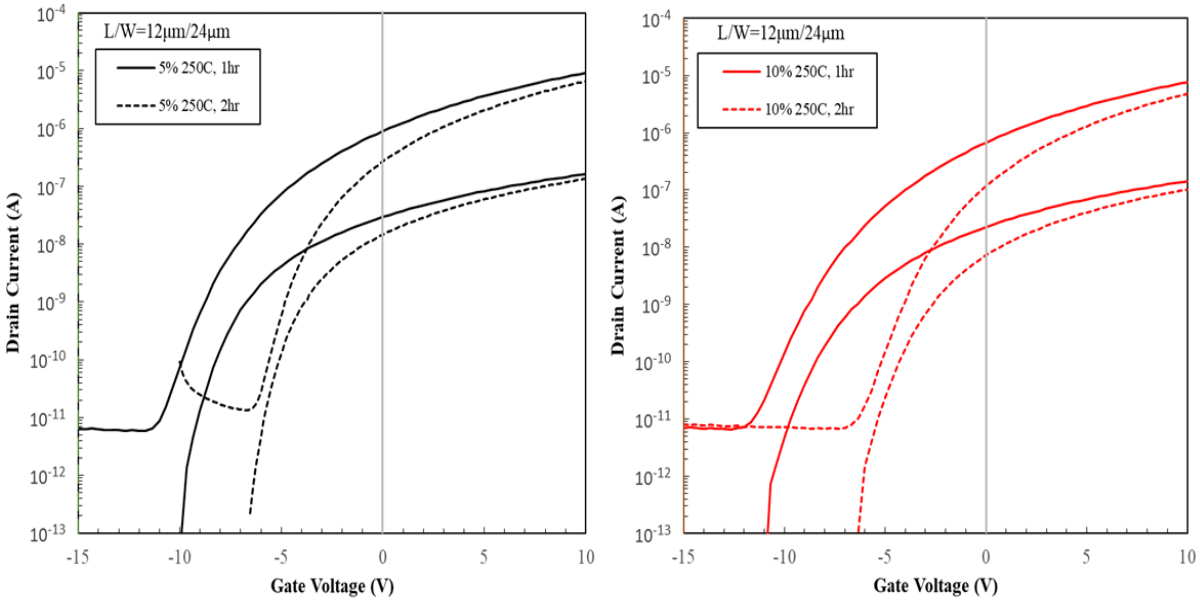

Figure 5.4: The hotplate anneal for P_{O2} 5% (Left) and 10%(Right) at 250˚C exhibits a device approaching enhancement mode of operation.

b) Effect of P_{O2}

In this section, the outcomes of the 250°C anneal are compared for devices with P_{O2} at 5% and 10%. Figure 5.5 presents a side-by-side comparison of device characteristics for P_{O2} at 5% and 10% following 1-hour and 2-hour anneals at 250°C. Notably, the 1-hour anneal at 250°C results in identical device characteristics for both P_{O2} scenarios. However, with the 2-hour anneal at 250°C, the device with P_{O2} at 10% exhibits a slightly more right-shifted behavior compared to P_{O2} at 5%, indicating a state of transition. The additional anneal time demonstrates consistency between the device characteristics of P_{O2} 5% and 10%, suggesting a weaker dependency between P_{O2} and anneal temperature at this higher temperature range. While the difference effect relatively small the trend always indicate that higher P_{O2} will support some additional right shift.

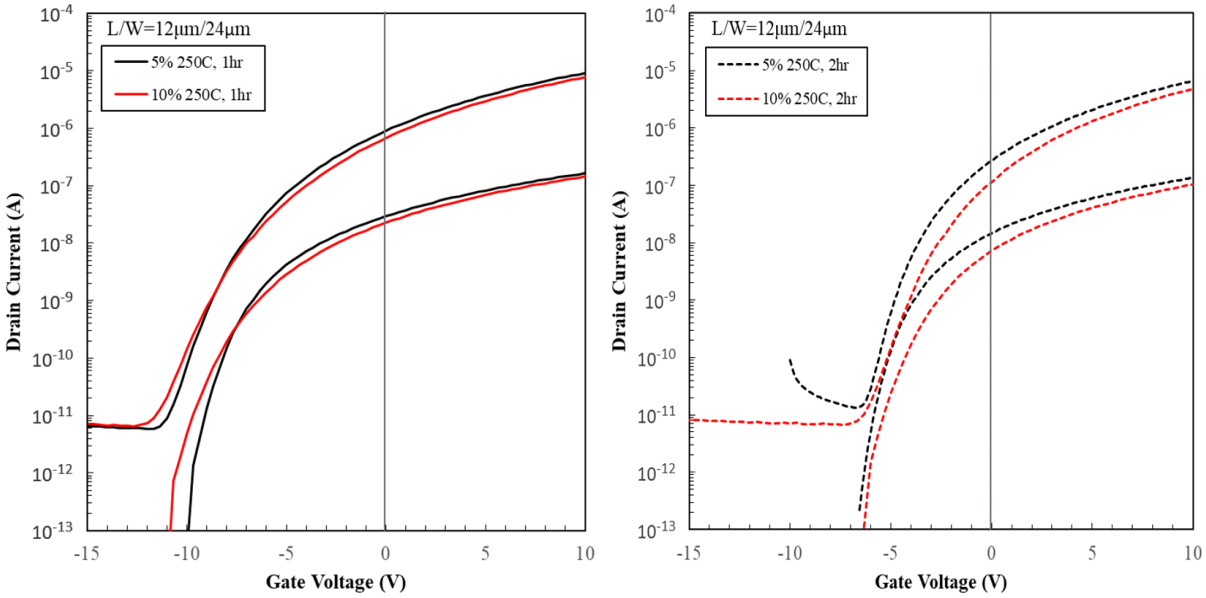

Figure 5.5: I_D-V_{GS} characteristics comparison after hotplate annealing at 250°C for 1 hour and 2 hours, showing comparable results at both P_{O2} 5% and 10%.

5.4 Heat Treatment #4: 275˚C, 1hour hotplate anneal in air ambient

The next step of sequential anneal involved the devices with P_{O2} 5% and 10% being subjected to a hotplate anneal at air ambient for 275˚C for an hour. There is a subtle right shift in the device characteristics of the P_{O2} at 10% compared to P_{O2} at 5% as seen in Figure 5.6. This observation indicates that the device with P_{O2} at 10% responds more favorably to annealing, resulting in an approximately 1V right shift towards enhancement mode operation.

When comparing the anneal at 275°C for 1 hour with the 250°C for 2 hours, P_{O2} at 5% exhibits nearly identical device characteristics, as depicted in Figure 5.6. While, for P_{O2} at 10%, there is an approximate 1V right shift, it is not particularly substantial. It is reasonable to assert that the anneal at 275°C for 1 hour on both P_{O2} 5% and 10% has minimal impact on the I_D-V_{GS} characteristics, as it does not have significant differences from the 250˚C anneal for 2 hours.

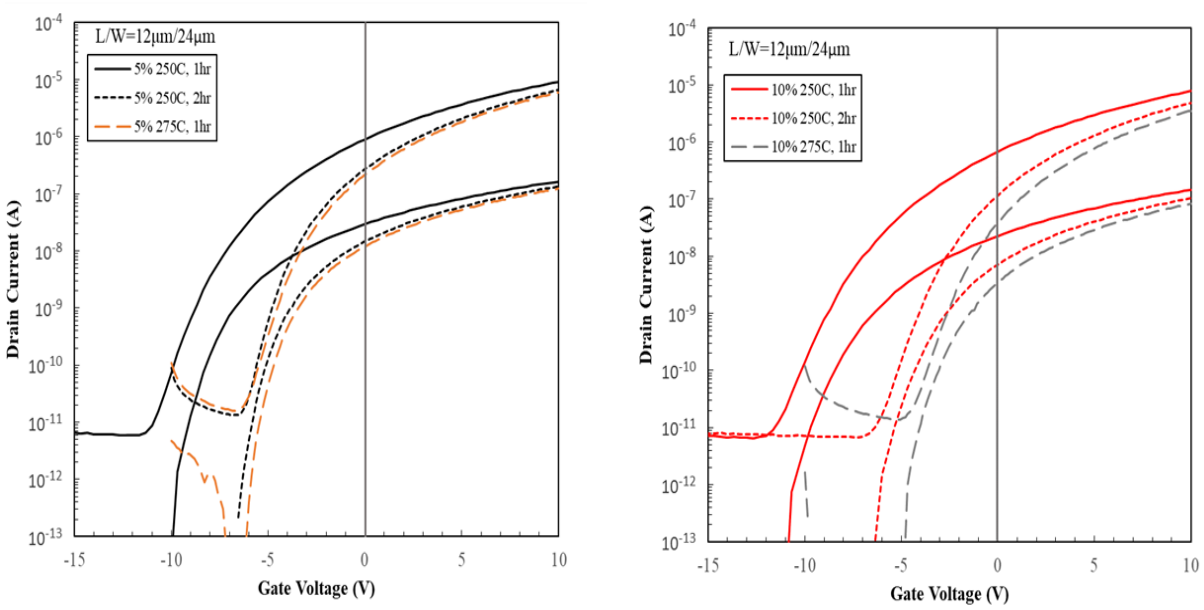

Figure 5.6: P_{O2} 10% shows the I_D-V_{GS} characterises moving right after consequent higher temperature anneal with a compromise in current level; showing the device approaching enhancement mode of operation.

In the next step of the anneal process, a 275°C hotplate anneal was performed for an hour on all P_{O2} levels. The results indicated that the I_D-V_{GS} characteristics of 6% and 7% closely resemble those of 5%, with almost no discernible difference. The device with P_{O2} at 8% acts as a midpoint between the characteristics of 5% and 10%. In Figure 5.7, a comparison of device characteristics for P_{O2} levels of 5%, 8% and 10% is presented. The devices are seen to still depend on the P_{O2} for the I_D-V_{GS} at 275˚C, which establishes that the anneal response is still dependant on P_{O2} of the devices under these conditions

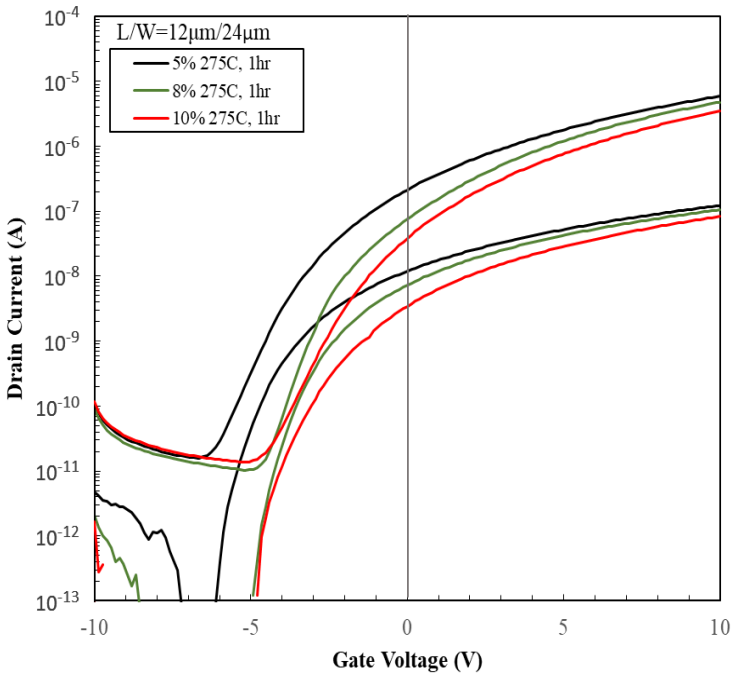

Figure 5.7: I_D-V_{GS} characterises in depletion mode, displayed a right ward shift with a compromise in current level after 275˚C, 1hr anneal.

5.5 Heat Treatment #5: *300˚C anneal*

The next stage of the experimental section focuses on understanding how a 300˚C anneal at different ambient impacts the IWO TFTs with different P_{O2} levels in the IWO film.

a) Hotplate Anneal at 300˚C, 2hours

In Figure 5.8, a comparative analysis of I_D-V_{GS} characteristics is presented for two IWO films with different P_{O2} at 5% and 10%, subjected to annealing at 300°C for two hours on a hotplate vs 275C,1 hour anneal. The device characteristics appear similar for both P_{O2} 5% and 10%, with the 10% P_{O2} device exhibiting a lower current level than the P_{O2} 5% device at 275C, 1hour anneal.

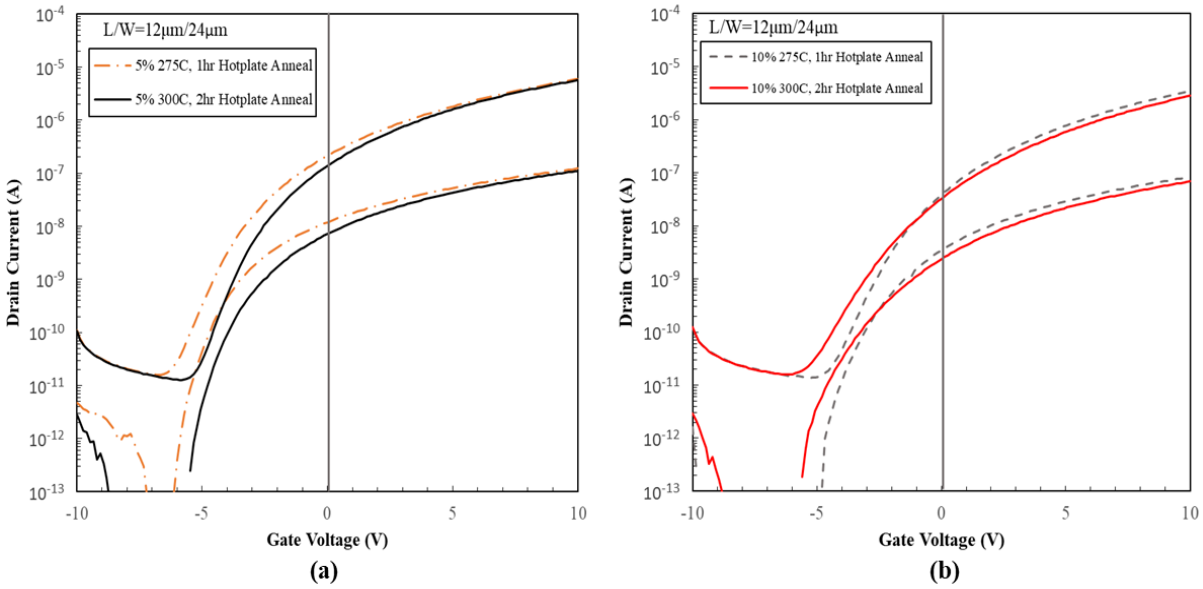

Figure 5.8: Comparative analysis of hotplate anneal at 275°C, 1 hour versus 300°C, 1 hour (a) Similar device operation observed at P_{O2} 5% after both anneals with a V_{th} shift of 1V

(b) Similar device characterization noted for P_{O2} 10%.

b) Furnace anneal at 300˚C, 30 minutes in oxygen ambient

Figure 5.9 shows a comparison between P_{O2} levels of 10% and 5% after furnace anneal in oxygen ambient at 300°C for a duration of 30 minutes. Post-annealing, both devices exhibited comparable performance, with subthreshold distortion. This indicates that the annealing process dominated the variations in oxygen partial pressure of these devices, however it is not a desirable transfer characteristics.

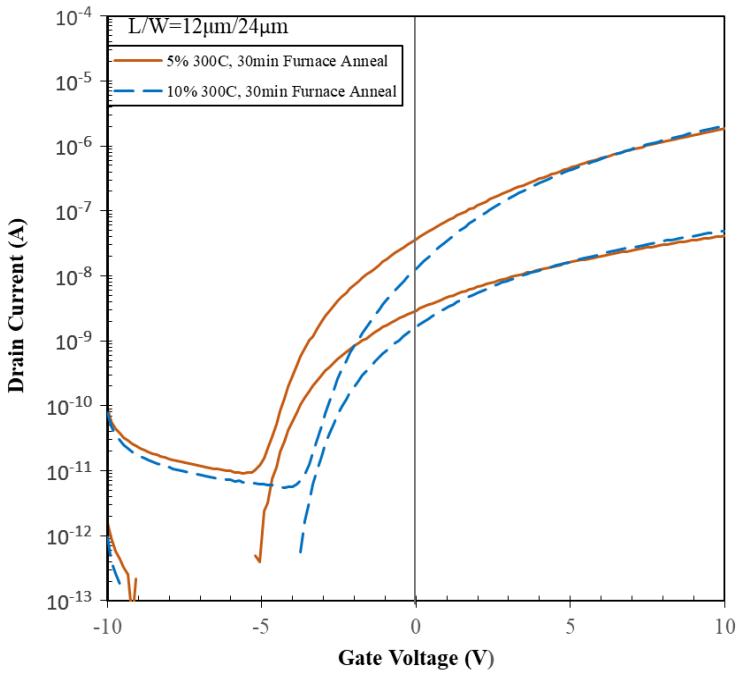

Figure 5.9: The furnace anneals in O_2 ambient overrode the variations in oxygen partial pressures of the devices.

c) Hotplate Anneal vs Furnace Anneal

In Figure 5.10(a), a comparison is drawn between hotplate anneals at 300°C for 2 hours and furnace anneal at 300°C for 30 minutes in an oxygen ambient for the P_{O2} 5% IWO TFT. Interestingly, the furnace anneal further reduces the current range for the P_{O2} 5% device, while the V_{th} remains consistent at around -5V. Figure 5.10(b) presents a comparison among hotplate anneals at 300C, 2-hour and a 300°C, 30-minute furnace anneal in an oxygen ambient for 10% P_{O2} IWO TFT. Following the furnace anneal, there is minimal difference in the I_D-V_{GS} characteristics between the 2-hour hotplate anneal and the furnace anneal, with the V_{th} being right shifted by about 1V

The impact of furnace annealing in an oxygen ambient appears more pronounced on devices with lower P_{O2}. When comparing the outcomes of furnace annealing for P_{O2} at 5% and 10%, it is evident that the current levels are low for both devices. However, the hotplate treatment favoured the device with P_{O2} at 5%, exhibiting better current levels.

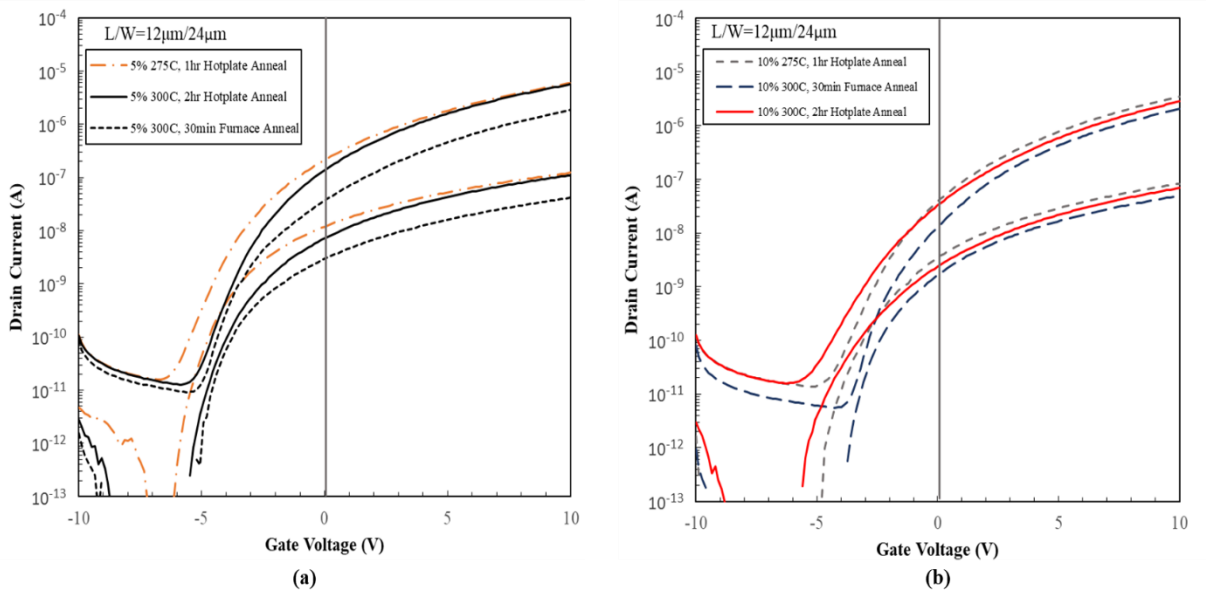

Figure 5.10 (a) Device operations for P_{O2} 5% remain similar after both hotplate and furnace anneals, with lower current levels observed after each anneal. (b) P_{O2} 10% demonstrates comparable device performance following both hotplate and furnace anneals

In the subsequent experimental phase, devices with P_{O2} levels of 6% to 9% underwent annealing in an oxygen furnace ambient at 300°C for a duration of 30 minutes. As illustrated in Figure 5.11, all the devices demonstrated comparable performance with low current drive; some device characterises overlapping better than the other, indicating the presence of some oxygen trap states. Devices exhibit subthreshold distortion and separation consistently across all P_{O2}, suggesting the presence of remaining defect states within the IWO film or its associated interfaces (gate dielectric and back channel). The annealing process dominated the variations in oxygen partial pressure of these devices; however, it is not a desirable transfer characteristics. The results of the furnace anneal are consistent throughout Phase I and Phase II.

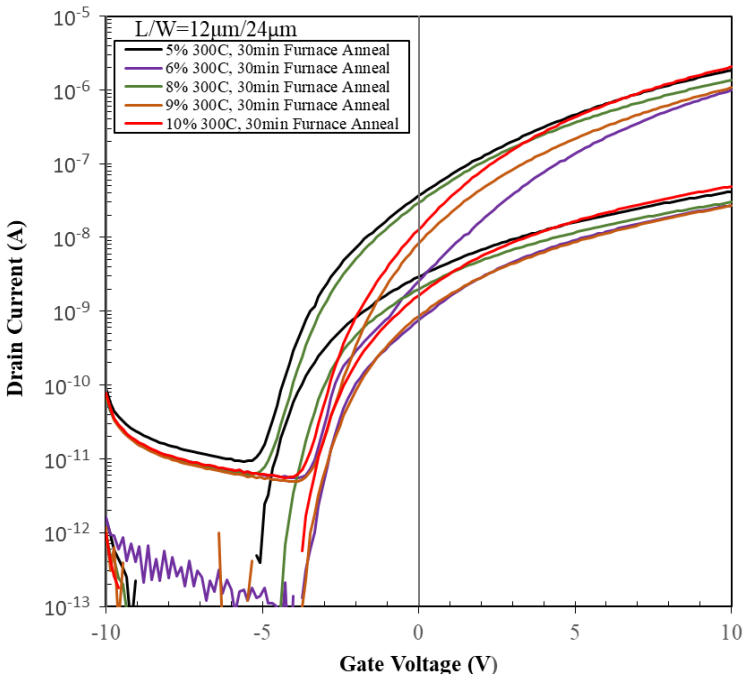

Figure 5.11: The furnace anneal in O_2 ambient overrode the variations in oxygen partial pressures of the devices for all the P_{O2}(5%- 10%)

5.6 Summary

The Phase II experimental investigation commenced with a low temperature anneal at 100°C for one hour. A peculiar observation emerged where the devices demonstrated a transient improvement which appears to be linked to the initial P_{O2} in the IWO film of the TFT. Notably, current levels exhibited degradation with increasing P_{O2}. The anneal at 100°C yielded inconsistent results, with some devices appearing more promising than others. A pronounced drop was observed between devices with P_{O2} at 8% and 9%, showing a significant decrease in current levels. Thus, it can be inferred that there is a significant reduction in donor-like defects, and the right shift is associated with lower current. In Phase II of P_{O2} 5% devices, notable inconsistencies were observed, revealing a bimodal behavior. Some devices exhibited a significant right shift, while others were notably positioned to the left of 0V.

Beyond the 100°C anneal, higher temperature anneals altered device behavior. The 200°C anneal caused a reversal of defect passivation resulting in significant left shift

(approximately -30V). The transfer characteristics of the devices annealed at 200°C resembled those of the un-annealed devices, possibly indicating a reconfigured defect state. The 250°C anneal re-established the donor state passivation and exhibited a continued right shift. Devices annealed at 275°C for 1 hour exhibited similar behavior to those annealed at 250°C, indicating stability.

At 300°C anneal, all devices exhibited similar behavior, maintaining a consistent threshold voltage, but experienced a loss of current. However, furnace anneals in an oxygen ambient led to the degradation of all devices, with a reduced current drive and subthreshold, with little correlation to the P_{O2}. While Phase II furnace anneal has better transfer characteristics without any distortion, the device's mobility encounters challenges in both phases of furnace anneals. The presence of numerous trap states at the back channel or gate oxide interface resulted in a shallow subthreshold slope and significant separation. Therefore, it can be concluded that the furnace annealing performed in an oxygen environment did not have a positive impact on the overall device performance.

Notably, with a P_{O2} of 10%, the device characteristics consistently right shifted after each annealing treatment, but with lower current levels. The lower density carriers at P_{O2} 10% seem insufficient to support the on-state current level, indicating a complex relationship between the annealing process and the initial oxygen partial pressure.

CHAPTER 6: CONCLUSIONS

IWO has been shown, in literature, to be a potential contender for future display applications due to its electrical characteristics and high electron mobility with lower operating voltage when compared to IGZO. The early phases of this study demonstrated good performance of IWO TFTs during low temperature anneals at higher P_{O2}, prompting an in-depth exploration into the influence of oxygen partial pressure, anneal temperature, ambient conditions, and duration on the IWO film TFTs.

The devices annealed at 100˚C in air ambient demonstrated towards enhancement mode operation but with reduced mobility, which appears linked to the initial P_{O2} in the IWO film. There is a significant reduction in donor-like defect and pronounced dependence on the initial P_{O2} of the devices. The anneal at 100°C yielded inconsistent results, with some devices appearing more promising than others. The devices after 100˚C anneal supports behavior closest to enhancement mode, but with a trade-off between V_T vs mobility and Imax.

The devices annealed at 200°C anneal in air ambient caused a reversal of defect passivation resulting in significant left shift (approximately -30V). The transfer characteristics of the devices annealed at 200°C resembled those of the un-annealed devices, possibly indicating a reconfigured defect state. The devices annealed at 250-275˚C in air ambient demonstrate minor dependence on the initial P_{O2} of the devices.

Figure 6.1(a) and (b) presents a comparison of furnace anneals at 100°C, 275°C, and 300°C for P_{O2} concentrations of 5% and 10%. In this experiment, the best parametric annealing condition for all P_{O2} scenarios is observed to be around 275°C, with varied sub-optimal amounts of improvement in device operation exhibited over the 250°C treatment. The donor state passivation is successfully re-established, with the interaction between P_{O2} and anneal temperature less pronounced than at 100˚C. While the O_2 furnace anneal at 300°C offers some

additional characteristic right-shift, there is an unfortunate drop in on-state current even when considering the higher threshold voltage; this is especially pronounced in the 5% P_{O2} sample.

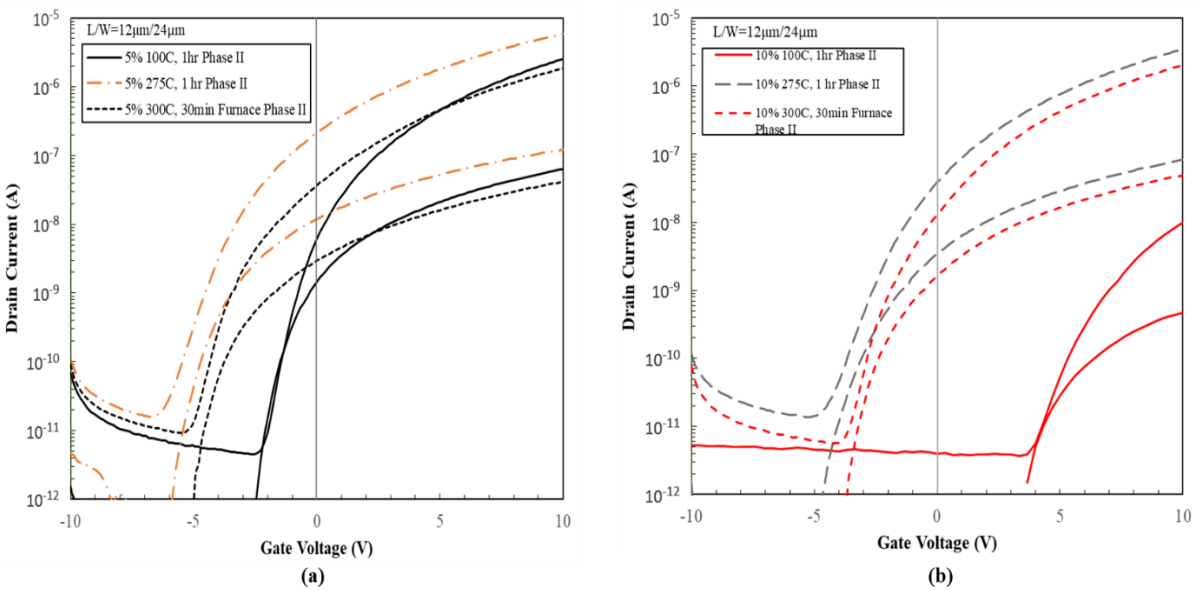

Figure 6.1: Comparison of anneals at 100°C, 275°C, and 300°C for P_{O2} of 5%(Left) and 10%(Right).

Table 4 compares the operating parameters of samples with P_{O2} at 5% and 10%, with anneal temperature at 100 °C and 275 °C. With the exception of the 10% P_{O2} annealed at 100 °C, mobility and current values listed have been extracted at $V_{GS} = V_T + 10V$ for an appropriate comparison.

P_{O2}, Temp	**V_T (V)**	**Mobility (cm^2/Vs)**	**SS (V/dec)**	**$I_{max(adj)}$ (Low drain) (A)**	**$I_{max(adj)}$ (High drain) (A)**
5%, 100˚C	-1.5	1.4	0.5	50nA	1.7u
10%,100˚C	6.5	0.06	~1.0	0.5nA*	10nA*
5%, 275˚C	-4.5	1.7	0.6	59nA	2.2u
10%, 275˚C	-3.0	1.5	0.9	48nA	1.6u

Table 4: Operating parameters of P_{O2} 5% and 10% at 100˚C and 275˚C anneal

* Imax value listed; V_T + 10V is beyond the measured V_{GS} range.

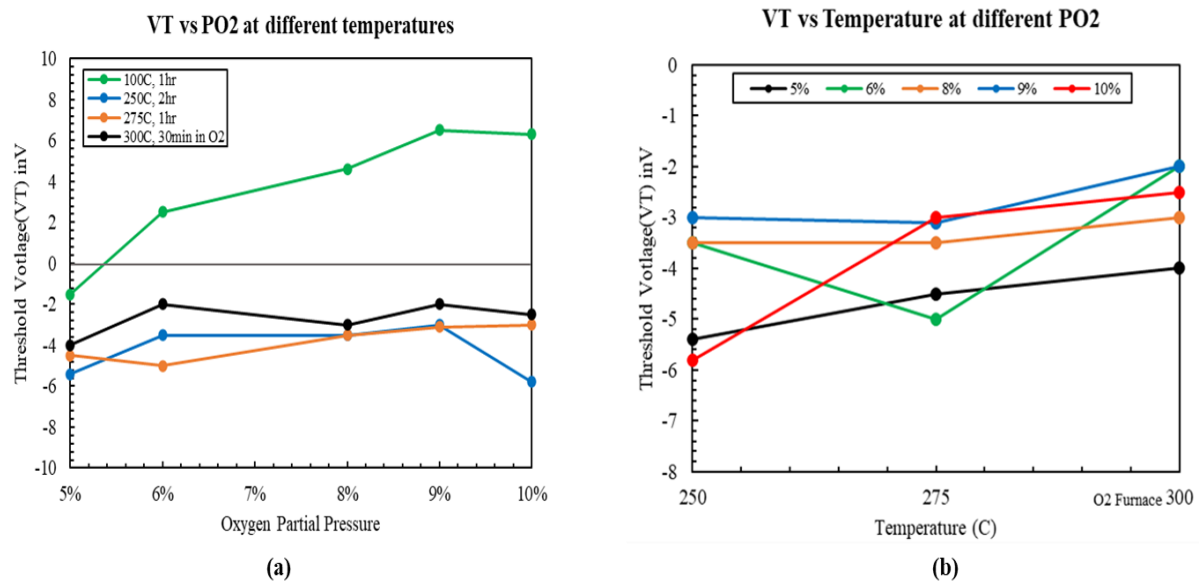

Figure 6.2: (a) Comparison at different anneal temperatures of V_T vs P_{O2} (b) Comparison at different P_{O2} of V_T vs temperatures

Figure 6.2 shows a comparison of threshold voltage over changes in P_{O2} and anneal temperature. Threshold voltage values exceed +6V on high P_{O2} devices annealed at 100˚C, however the associated mobility and current values are very low. The annealing process at 100 °C does not serve any practical purpose, but it demonstrates an interesting metastable condition. The V_T response of annealing at $T \geq 250$ °C appears somewhat random; however, in general the values continue to increase with increasing temperature and P_{O2}.

Figure 6.3 shows a current comparison of 5% and 10% P_{O2} samples annealed at $T \geq 250$ °C. Annealing at 275°C in air appears to exhibit a balanced, but not sufficient condition for both V_T and current drive over the oxygen partial pressure values investigated; however, the existence of remaining trap states suggests incomplete passivation. Furnace annealing in O_2 at 300 °C lead to degradation in device operation, which was more pronounced in the lower P_{O2} sample.

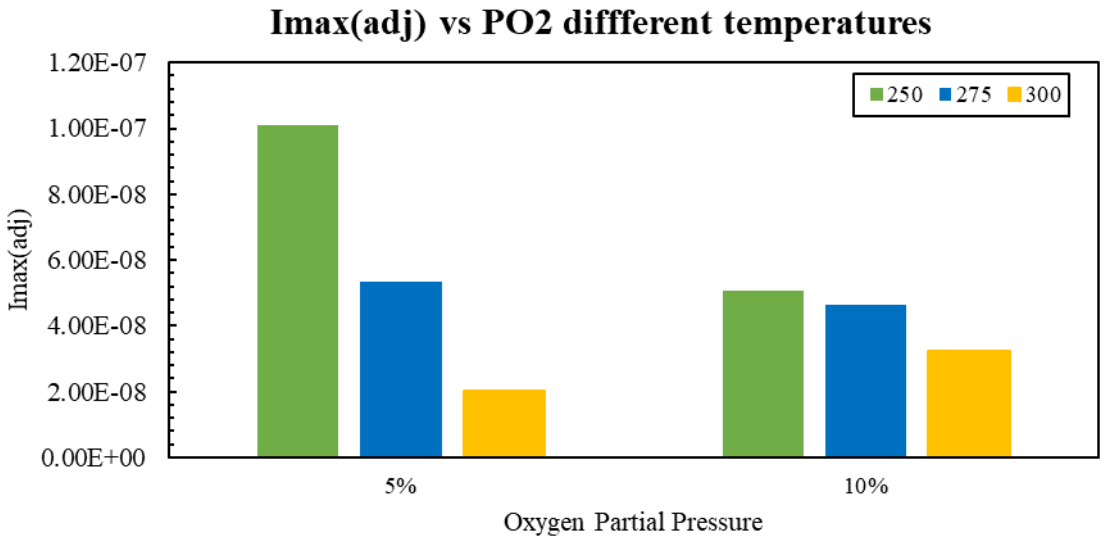

Figure 6.3: Comparison of $I_{max(adj)}$ vs P_{O2} for T ≥ 250 °C samples.

The various treatments examined in this experiment yielded TFT performance that would be considered unsatisfactory namely a carrier mobility of more than 20cm^2/Vs and enhancement mode operation (based on the criteria outlined in Chapter 2). The combined results from this experiment emphasize the sensitivity of the IWO film to compositional non-uniformity. The most favorable outcomes was observed at 10% P_{O2}, indicating the potential benefits of exploring higher oxygen partial pressures in future studies. The extended research can include variations in sputter process parameters such as target specifications, pressure, power, among others, for a more comprehensive understanding of the impact on device performance. In addition, a thinner IWO semiconductor film should help address the challenge of achieving electron depletion and support enhancement-mode operation, i.e. more positive threshold voltage.

REFERENCES

[1] Cristaldi, D.J., Pennisi, S., Pulvirenti, F. (2009). Passive LCDs and Their Addressing Techniques. In: Liquid Crystal Display Drivers. Springer, Dordrecht. https://doi-org.ezproxy.rit.edu/10.1007/978-90-481-2255-4_3

[2] "Liquid Crystal Display (LCD) Passive Matrix and Active Matrix Addressing," 2004

[3] Bardeen J. Brattain W. H. 1948 The transistor- A Semiconductor Triode. Physics Revision 74, 230 242.

[4] Weimer P. K. 1962 The TFT- A New Thin-Film Transistor. Proc. IEEE 50, 1462 1471.

[5] P. G. le Comber, W. E. Spear, and A. Ghaith, "Amorphous-silicon field-effect device and possible application," *Electronics Letters*, vol. 15, no. 6, p. 179, 1979, doi: 10.1049/el:19790126.

[6] A. J. Snell, K. D. Mackenzie, W. E. Spear, P. G. LeComber, and A. J. Hughes, "Application of amorphous silicon field effect transistors in addressable liquid crystal display panels," *Applied Physics*, vol. 24, no. 4, pp. 357–362, Apr. 1981, doi: 10.1007/BF00899734.

[7] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature*, vol. 432, no. November, pp. 488–492, 2004.

[8] J. G. Um, M. Mativenga, P. Migliorato, and J. Jang, "Defect generation in amorphous-indium-gallium-zinc-oxide thin-film transistors by positive bias stress at elevated temperature," Journal of Applied Physics, vol. 115, no. 13, 2014, doi: 10.1063/1.4870458.

[9] S. Lee, M. Mativenga, and J. Jang, "Removal of negative-bias-illumination-stress instability in amorphous-InGaZnO thin-film transistors by top-gate offset structure," IEEE Electron Device Letters, vol. 35, no. 9, pp. 930–932, 2014, doi: 10.1109/LED.2014.2333014.

[10] S. Jin, T. W. Kim, Y. G. Seol, M. Mativenga, and J. Jang, "Reduction of positive-bias-stress effects in bulk-accumulation amorphous-InGaZnO TFTs," IEEE Electron Device Letters, vol. 35, no. 5, pp. 560–562, 2014, doi: 10.1109/LED.2014.2311172

[11] K.-H. Lee, et al., "The effect of moisture on the photon-enhanced negative bias thermal instability in Ga–In–Zn–O thin film transistors," Applied Physics Letters, vol. 95, no. 23, p. 232106, Dec. 2009, doi: 10.1063/1.3272015.

[12] M. S. Kabir et al., “Channel-length dependent performance degradation of thermally stressed IGZO TFTs,” ECS Transactions, vol. 86, no. 11, pp. 125–133, 2018, doi: 10.1149/08611.0125ecst.

[13] T.-Y. Hsieh, T.-C. Chang, T.-C. Chen, and M.-Y. Tsai, “Review of Present Reliability Challenges in Amorphous In-Ga-Zn-O Thin Film Transistors,” ECS Journal of Solid-State Science and Technology, vol. 3, no. 9, pp. Q3058–Q3070, 2014, doi: 10.1149/2.013409jss

[14] T. Kamiya, K. Nomura, and H. Hosono, “Origins of High Mobility and Low Operation Voltage of Amorphous Oxide TFTs: Electronic Structure, Electron Transport, Defects and Doping,” Journal of Display Technology, vol. 5, no. 7, pp. 273–288, 2009, doi: 10.1109/JDT.2009.2034559.

[15] T. Mudgal, N. Walsh, N. Edwards, R. G. Manley, and K. D. Hirschman, “Interpretation of defect states in sputtered IGZO devices using i-v and c-v analysis," vol. 64, no. 10, pp. 93-100, Aug. 2014.

[16] J.-S. Yoo, S.-H. Jung, Y.-C. Kim, S.-C. Byun, J.-M. Kim, N.-B. Choi, S.-Y. Yoon, C.-D. Kim, Y.-K. Hwang, I.-J. Chung, et al., “Highly flexible am-oled display with integrated gate driver using amorphous silicon TFT on ultrathin metal foil," Journal of Display Technology, vol. 6, no. 11, pp. 565-570, 2010.

[17] Tiwari, N., Rajput, M., John, R. A., Kulkarni, M. R., Nguyen, A. C., & Mathews, N., “Indium tungsten oxide thin films for flexible high-performance transistors and neuromorphic electronics”, ACS Applied Materials and Interfaces, 10(36), 30506-30513. doi:10.1021/acsami.8b06956(2018).

[18] Park, J. S., Kim, K., Park, Y. G., Mo, Y. G., Kim, H. D., Jeong, J. K., “Novel ZrInZnO Thin-film Transistor with Excellent Stability”, Adv. Mater. 2009, 21, 329–333.

[19] Liu, P.T., Chou, Y.T., Teng L.F., “Environment-Dependent Metastability of Passivation-Free Indium Zinc Oxide Thin Film Transistor after Gate Bias Stress”, Applied Phys. Lett. 2009, 95, 233504–3.

[20] Fortunato, E., Barquinha, P., Martins. R., “Oxide Semiconductor Thin-film Transistors: A Review of Recent Advances”, Adv Mater. 2012, 24, 2945–2986.

[21] Genoe. J, Obata. K, Ameys. M, Myny. K, Ke. T. H, Nag. M, Steudel. S, Schols. S, Maas. J, Tripathi. Ashutosh, Steen. J.L P. J.V, Ellis. Tim, Gelinck. G. H, Heremans. P., “Integrated Line Driver for Digital Pulse-Width Modulation Driven AMOLED Displays on Flex”, IEEE J. Solid-State Circuits, 2015, 50, 282–290.

[22] K. Nomura, T. Kamiya, H. Ohta, T. Uruga, M. Hirano, and H. Hosono, “Local coordination structure and electronic structure of the large electron mobility amorphous oxide semiconductor In-Ga-Zn-O: Experiment and ab initio calculations,” Physical Review B, vol. 75, no. 3, Jan. 2007, doi: 10.1103/PhysRevB.75.035212.

[23] T. Kamiya, K. Nomura, and H. Hosono, “Origins of High Mobility and Low Operation Voltage of Amorphous Oxide TFTs: Electronic Structure, Electron Transport, Defects and Doping,” Journal of Display Technology, vol. 5, no. 7, Jul. 2009, doi: 10.1109/JDT.2009.2021582.

[24] M. F. A. M. Van Hest, M. S. Dabney, J. D. Perkins, D. S. Ginley, and M. P. Taylor, “Titanium-doped indium oxide: A high-mobility transparent conductor,” Applied Physics Letters, vol. 87, no. 3, pp. 10–13, 2005, doi: 10.1063/1.1995957.

[25] Z. Lu, F. Meng, Y. Cui, J. Shi, Z. Feng, and Z. Liu, “High quality of IWO films prepared at room temperature by reactive plasma deposition for photovoltaic devices,” Journal of Physics D: Applied Physics, vol. 46, no. 8, 2013, doi: 10.1088/0022-3727/46/7/075103.

[26] P. T. Liu, C. H. Chang, and C. J. Chang, “Reliability enhancement of high-mobility amorphous indium-tungsten oxide thin film transistor,” ECS Transactions, vol. 67, no. 1, pp. 9–16, 2015, doi: 10.1149/06701.0009ecst.

[27] Y. Huang, D. Li, J. Feng, G. Li, and Q. Zhang, “Transparent conductive tungsten-doped tin oxide thin films synthesized by sol-gel technique on quartz glass substrates,” *Journal of Sol-Gel Science and Technology*, vol. 54, no. 3, pp. 276‑281, 2010, doi: 10.1007/s10971-010-2182-0.

[28] Y. Meng *et al.*, “Molybdenum-doped indium oxide transparent conductive thin films,” *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, vol. 20, no. 1, pp. 288–290, 2002, doi: 10.1116/1.1421595.

[29] Y. Li, W. Wang, J. Zhang, and R. Wang, “Preparation and properties of tungsten-doped indium oxide thin films,” Rare Metals, vol. 31, no. 2, pp. 158–163, 2012, doi: 10.1007/s12598-012-0483-x.

[30] S. Aikawa, P. Darmawan, K. Yanagisawa, T. Nabatame, Y. Abe, and K. Tsukagoshi, “Thin-film transistors fabricated by low-temperature process based on Ga- and Zn-free amorphous oxide semiconductor,” *Applied Physics Letters*, vol. 102, no. 10, 2013, doi: 10.1063/1.4794903.

[31] D.Menzel and L.Korte, “ Evolution of Optical, Electrical, and Structural Properties of Indium Tungsten Oxide upon High Temperature Annealing,” *Physica Status Solidi (a)* , 217(18). https://doi.org/10.1002/pssa.202000165

[32] Z. Lu, F. Meng, Y. Cui, J. Shi, Z. Feng, and Z. Liu, “High quality of IWO films prepared at room temperature by reactive plasma deposition for photovoltaic devices,” Journal of Physics D: Applied Physics, vol. 46, no. 8, 2013, doi: 10.1088/0022-3727/46/7/075103.

[33] M. Qu, C. H. Chang, T. Meng, Q. Zhang, P. T. Liu, and H. P. D. Shieh, “Stability study of indium tungsten oxide thin-film transistors annealed under various ambient conditions,” Physica Status Solidi (A) Applications and Materials Science, vol. 214, no. 2, pp. 2–5, 2017, doi: 10.1002/pssa.201600465.

[34] M. Fakhri, H. Johann, P. Görrn, and T. Riedl, “Water as origin of hysteresis in zinc tin oxide thin-film transistors,” ACS Applied Materials and Interfaces, vol. 4, no. 9, pp. 4453–4456, 2012, doi: 10.1021/am301308y.

[35] J. Liu, D. B. Buchholz, J. W. Hennek, R. P. H. Chang, A. Facchetti, and T. J. Marks, “All-amorphous-oxide transparent, flexible thin-film transistors. Efficacy of bilayer gate dielectrics,” Journal of the American Chemical Society, vol. 132, no. 34, pp. 11934–11942, 2010, doi: 10.1021/ja9103155.